TE0320 Overview

The TE0320 is an industrial-grade FPGA micromodule integrating a leading-edge *Xilinx Spartan-3A DSP* FPGA, a USB 2.0 microcontroller, 32-bit wide 128 MByte DDR RAM, 4 MByte Flash memory for configuration and operation, and powerful switch-mode power supplies for all on-board voltages. A large number of configurable I/Os is provided via robust board-to-board (B2B) connectors.
All this on a tiny footprint, **smaller than a credit card**, at the most competitive price. Hardware and software development environment as well as reference designs are available at: www.trenz-electronic.de.

Xilinx ISE Device Support

- Xilinx Spartan-3A DSP 1800: ISE WebPACK (completely free)
- Xilinx Spartan-3A DSP 3400: ISE Design Suite (license needed)

Model	FPGA	Power Supply	Temperatur Range	ISE
TE0320-00-EV01	XC3SD1800A-4FGG676C	USB connector	Commercial	WebPACK
TE0320-00-EV02	XS3SD1800A-4FGG676C	B2B connector	Commercial	WebPACK
TE0320-00-EV02I	XC3SD1800A-4FGG676I	B2B connector	Industrial (the negative temperature range starts at - 25 °C)	WebPACK
TE0320-00-EV02B	XC3SD3400A-4FGG676C	B2B connector	Commercial	Design Suite
TE0320-00-EV02C	XS3SD1800A-4FGG676C	B2B connector	Commercial	WebPACK
TE0320-00-EV02IB	XC3SD3400A-4FGG676I	B2B connector	Industrial (the negative temperature range starts at - 25 °C)	Design Suite

legend

- comm. = commercial grade temperature
- ind. = industrial grade temperature

TE0320 Series Selection Chart

Module Options

- **FPGA options**
  Module can be ordered with Spartan-3A DSP XC3SD1800A or XC3SD3400A chip.
- **Flash options**
  Module can be ordered with 32, 64 or 128 Mbit SPI Flash chip.
- **Temperature grade options**
  Module can be ordered in commercial or in extended (from -25 C° to +85 C°) temperature grade.

Sample Applications

- Cryptographic hardware module
- Digital signal processing
- Embedded educational platform
- Embedded industrial OEM platform
- Embedded system design
- Emulation platforms
- FPGA graphics

Key Features

- Industrial-grade **Xilinx Spartan-3A DSP** FPGA module (1800 k gates or 3400 k gates)
- USB 2.0 (**Hi-Speed USB**) interface with a signalling bit rate of up to 480 Mbit/s
- 32-bit wide 1 Gbit **DDR SDRAM**
- FPGA configuration through:
- JTAG (B2B connector, pin header)

- Image processing
- IP (intellectual property) cores
- Low-power design
- Parallel processing
- Rapid prototyping
- Reconfigurable computing
- System-on-Chip (SoC) development

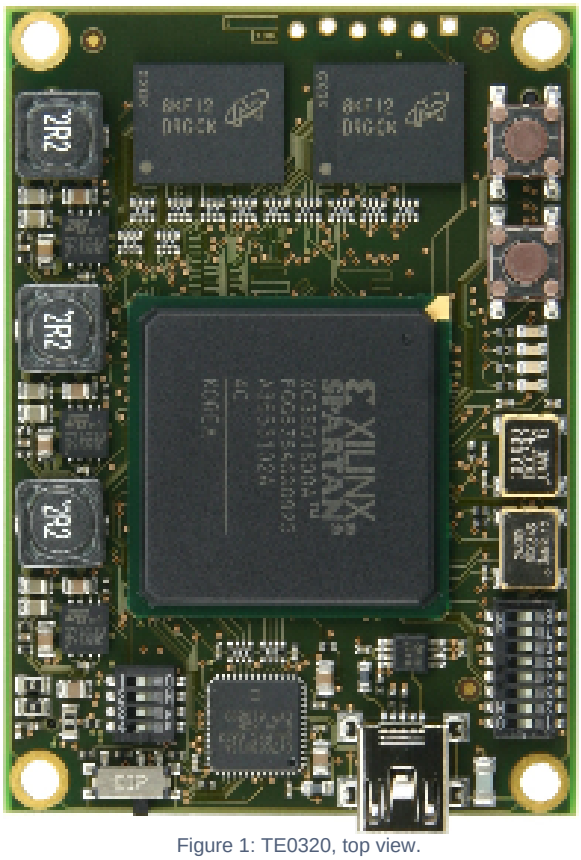


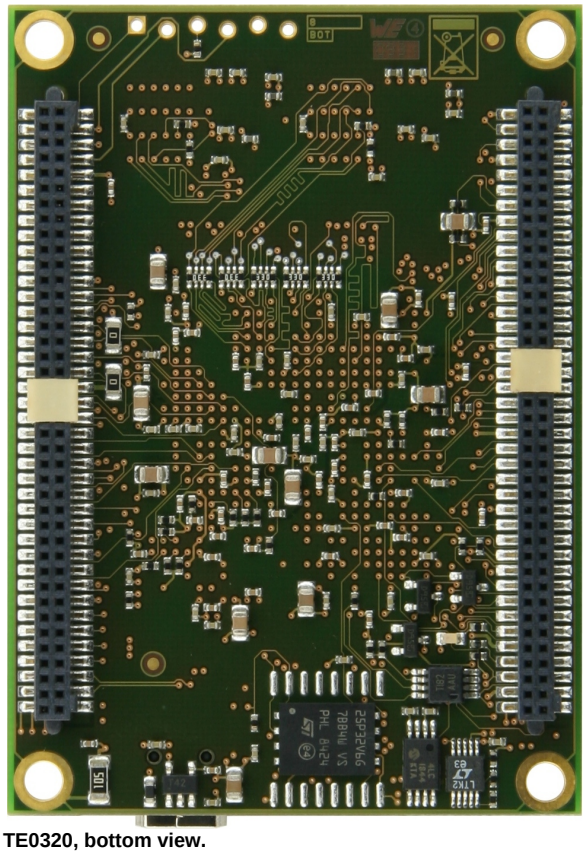
Figure 1: TE0320, top view.

TE0320, top view

- SPI Flash memory
- Large **SPI Flash** memory (for configuration and operation) accessible through:
- B2B connector (SPI direct)
- FPGA JTAG port (SPI indirect)
- USB bus (Firmware Upgrade Tool)
- On-board 100 MHz oscillator for high performance
- On-board 24 MHz oscillator available to user
- 3 on-board high-power, high-efficiency, switch-mode DC-DC converters capable of 3 A each
- Power supply range: 4.0 - 7.0 V
- Power supply via USB or B2B (carrier board)
- 4 LEDs, 2 push buttons, 8 DIP switches.
- Plug-on module with 2 female 1.27 mm pitch header connectors
- 109 FPGA I/O pins (+ 10 dual-purpose pins) available on B2B connectors
- Evenly spread supply pins for good signal integrity
- Assembly options for cost or performance optimization available on request

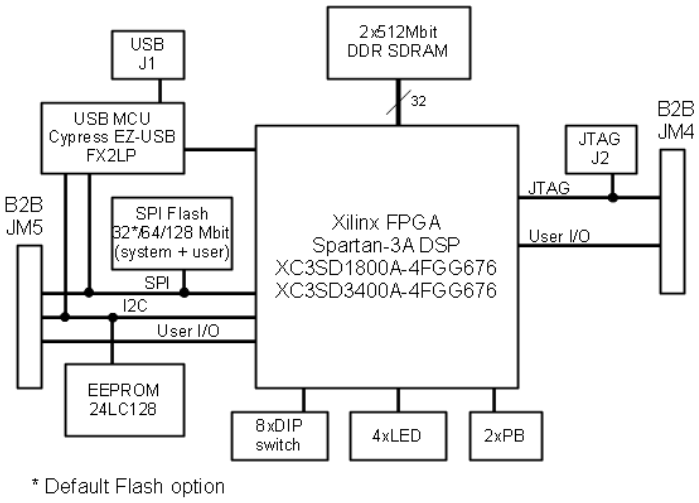
Specifications

- FPGA: Xilinx Spartan-3A DSP:
- XC3SD1800A-4FGG676C, XC3SD1800A-4FGG676I or
- XC3SD3400A-4FGG676C, XC3SD3400A-4FGG676I
- Cypress EZ-USB FX2LP™ USB FX2 microcontroller, high speed USB peripheral controller
- CY7C68013A-56LTXC (commercial grade) or
- CY7C68013A-56LTXI (industrial grade)
- Numonyx M25P32Default module configuration contain 32 MBit Flash / M25P64 / M25P128:low voltage, serial Flash memory with 75 MHz SPI bus interface
- 2 × 16-bit data-bus 512 Mbit DDR SDRAM (connected in parallel as a virtual 1 × 32-bit data-bus DDR SDRAM)
- Microchip Technology 24LC128I-ST128 kbit I2C CMOS serial EEPROM
- 3 × STMicroelectronics ST1S10:3 A, 900 kHz, monolithic synchronous step-down regulator 3 A for each power rail: 1.2 V, 2.5 V, 3.3 V
- Texas Instruments TPS370533DGN processor supervisory circuits with power-fail and watchdog
- 100 MHz oscillator (system + user)
- 24 MHz oscillator (system + user)
- 2 × CviLux CBC1-80-2-M110-2P1.27 mm (50 mil = .050") pitch 80-pin double row socket (female) header board-to-board (B2B) connectors with key and pegs
- 109 FPGA IO Pins routed to the B2B connector
- 6-pin JTAG header
- 1 × USB mini-B receptacle (device)
- 1 × LED (system)
- 4 × LED (user)
- 2 × push button (user)
- 4 × DIP switches (system)
- 1 × slide switch (system)
- 8 × DIP switch (user)



TE0320, bottom view.

Block Diagram



TE0320 block diagram