TE0715 Test Board

Table of contents

Overview

Zynq Design PS with Linux and simple frequency counter to measure MGT Reference CLK with Vivado HW-Manager.

Refer to http://trenz.org/te0715-info for the current online version of this manual and other available documentation.

Key Features

- Vitis/Vivado 2022.2
- PetaLinux
- SD
- EEPROM
- MAC from EEPROM
- USB
- I2C
- RTC
- FMeter
- Modified FSBL (some additional outputs and SI5338 reconfiguration)

Revision History

Date	Vivado	Project Built	Authors	Description
2023-07-05	2022.2	TE0715-test_board-vivado_2022.2-build_2_20230705115102.zip TE0715-test_board_noprebuilt-vivado_2022.2-build_2_20230705115102.zip	Waldemar Hanemann	• 2022.2 update
2023-05-06	2021.2.1	TE0715-test_board-vivado_2021.2-build_20_20230506205024.zip TE0715-test_board_noprebuilt-vivado_2021.2-build_20_20230506205024.zip	Manuela Strücker	• new Assembly variants
2022-02-09	2021.2	TE0715-test_board-vivado_2021.2-build_11_20220208131345.zip TE0715-test_board_noprebuilt-vivado_2021.2-build_11_20220208131345.zip	Manuela Strücker	• 2021.2 update

2021-12-16	2020.2	TE0715-test_board-vivado_2020.2-build_9_20211216124925.zip TE0715-test_board_noprebuilt-vivado_2020.2-build_9_20211216124901.zip	Manuela Strücker	• new Assembly variants
2021-06-16	2020.2	TE0715-test_board-vivado_2020.2-build_5_20210611100936.zip TE0715-test_board_noprebuilt-vivado_2020.2-build_5_20210611100742.zip	Manuela Strücker	• update mount function (from busybox to util-linux 2.34)
2021-05-31	2020.2	TE0715-test_board-vivado_2020.2-build_5_20210531083131.zip TE0715-test_board_noprebuilt-vivado_2020.2-build_5_20210531083148.zip	John Hartfiel/ Manuela Strücker	• bugfix TE0715_board_files.csv for TE0715-04-71I33-L ID
2021-04-27	2020.2	TE0715-test_board-vivado_2020.2-build_5_20210428094945.zip TE0715-test_board_noprebuilt-vivado_2020.2-build_5_20210428095209.zip	John Hartfiel/ Manuela Strücker	• update to vivado version 2020.2 • implemented boot.scr file for distro_boot
2020-06-10	2019.2	TE0715-test_board-vivado_2019.2-build_12_20200610070857.zip TE0715-test_board_noprebuilt-vivado_2019.2-build_12_20200610071014.zip	John Hartfiel	• bugfix usb reset • changes device tree for eeprom mac • new variants
2019-05-09	2018.3	TE0715-test_board-vivado_2018.3-build_05_20190509094447.zip TE0715-test_board_noprebuilt-vivado_2018.3-build_05_20190509094505.zip	John Hartfiel	• TE Script update • rework of the FSBLs • some additional Linux features • MAC from EEPROM
2018-10-01	2018.2	TE0715-test_board-vivado_2018.2-build_03_20181001131411.zip TE0715-test_board_noprebuilt-vivado_2018.2-build_03_20181001131421.zip	John Hartfiel	• Rework Board Part Files (PS) • small design changes • SI5338 reconfiguration default activated on FSBL • update linux startup app

2018-04-26	2017.4	TE0715-test_board-vivado_2017.4-build_07_20180426171530.zip TE0715-test_board_noprebuilt-vivado_2017.4-build_07_20180426171546.zip	John Hartfiel	• new assembly variant
2018-03-27	2017.4	te0715-test_board-vivado_2017.4-build_07_20180327223552.zip te0715-test_board_noprebuilt-vivado_2017.4-build_07_20180327223606.zip	John Hartfiel	• Board Part Bug fix with UART 1
2018-01-05	2017.4	te0715-test_board-vivado_2017.4-build_01_20180105195436.zip te0715-test_board_noprebuilt-vivado_2017.4-build_01_20180105195452.zip	John Hartfiel	• No Design changes • Add FSBL for Flash Programming
2017-11-10	2017.2	te0715-test_board-vivado_2017.2-build_05_20171110134232.zip te0715-test_board_noprebuilt-vivado_2017.2-build_05_20171110134247.zip	John Hartfiel	• New Web Link on Board Part Files • Add optional FSBL Code to reprogram SI5338
2017-10-19	2017.2	te0715-test_board-vivado_2017.2-build_04_20171019141808.zip te0715-test_board_noprebuilt-vivado_2017.2-build_04_20171019141825.zip	John Hartfiel	• changed Flash typ on TE0715_board_files.csv (older one is not supported on Vivado 2017.2)
2017-09-22	2017.2	te0715-test_board-vivado_2017.2-build_02_20170927143412.zip te0715-test_board_noprebuilt-vivado_2017.2-build_02_20170927143427.zip	John Hartfiel	• initial release

Design Revision History

Release Notes and Know Issues

Issues	Description	Workaround	To be fixed version

Wrong DDR Size on the preset files for Single core variants only	TE0715_12S_1C\1.1\preset.xml did not include DDR settings and board automation select wrong DDR size in this case.	open TE0715_12S_1C\1.1\preset.xml and add this parameter
		
		`<user_parameter name="CONFIG.PCW_UIPARAM_DDR_MEMORY_TYPE" value="DDR 3 (Low Voltage)" />`
		
		`<user_parameter name="CONFIG.PCW_UIPARAM_DDR_PARTNO" value="MT41J256M16 RE-125"/>`
			(will be done with 23.2 update)

QSPI Flash	Programming QSPI fails with Vivado 2021.2 and 2022.2	use Vivado 2020.2 or 2019.2 or older for programming	
Timing problems with Frequency counter	can be ignored	---	with 2018-10-01 update

Known Issues

Requirements

Software

Software	Version	Note
Vitis	2022.2	needed, Vivado is included into Vitis installation
PetaLinux	2022.2	needed
SI ClockBuilder Pro	---	optional

Software

Hardware

Basic description of TE Board Part Files is available on TE Board Part Files.

Complete List is available on "<project folder>\board_files*_board_files.csv"

Design supports following modules:

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMMC	Others	Notes
TE0715-02-15-1C	03_15_1c_1gb	REV02|REV01	1GB	32MB	NA	NA	NA
TE0715-02-15-1I	03_15_1i_1gb	REV02|REV01	1GB	32MB	NA	NA	NA
TE0715-02-15-1I1	03_15_1i_1gb	REV02|REV01	1GB	32MB	NA	NA	NA
TE0715-02-30-1C	03_30_1c_1gb	REV02|REV01	1GB	32MB	NA	NA	NA
TE0715-02-30-1I	03_30_1i_1gb	REV02|REV01	1GB	32MB	NA	NA	NA
TE0715-03-15-1I	03_15_1i_1gb	REV03	1GB	32MB	NA	NA	NA
TE0715-03-15-1I3	03_15_1i_1gb	REV03	1GB	32MB	NA	NA	NA
TE0715-03-15-2I	03_15_2i_1gb	REV03	1GB	32MB	NA	NA	NA
TE0715-03-30-1C	03_30_1c_1gb	REV03	1GB	32MB	NA	NA	NA
TE0715-03-30-1I	03_30_1i_1gb	REV03	1GB	32MB	NA	NA	NA
TE0715-03-30-1I3	03_30_1i_1gb	REV03	1GB	32MB	NA	NA	NA
TE0715-03-30-3E	03_30_3e_1gb	REV03|REV02|REV01	1GB	32MB	NA	NA	NA
TE0715-04-12S-1C	04_12s_1c_1gb	REV04	1GB	32MB	NA	NA	Low Power DDR
TE0715-04-15-1I	04_15_1i_1gb	REV04	1GB	32MB	NA	NA	Low Power DDR
TE0715-04-15-1I3	04_15_1i_1gb	REV04	1GB	32MB	NA	NA	Low Power DDR 2.5mm connector
TE0715-04-15-1IC	04_15_1i_1gb	REV04	1GB	32MB	NA	NA	Low Power DDR. 3M NOVEC coating
TE0715-04-15-2I*	04_15_2i_1gb	REV04	1GB	32MB	NA	NA	Low Power DDR
TE0715-04-21C33-A	04_12s_1c_1gb	REV04	1GB	32MB	NA	NA	Low Power DDR
TE0715-04-30-1C	04_30_1c_1gb	REV04	1GB	32MB	NA	NA	Low Power DDR
TE0715-04-30-1I	04_30_1i_1gb	REV04	1GB	32MB	NA	NA	Low Power DDR
TE0715-04-30-1I3	04_30_1i_1gb	REV04	1GB	32MB	NA	NA	Low Power DDR. 2.5mm connector
TE0715-04-30-1IA	04_30_1i_1gb	REV04	1GB	32MB	NA	NA	Low Power DDR. Micron Flash
TE0715-04-30-3E	04_30_3e_1gb	REV04	1GB	32MB	NA	NA	Low Power DDR
TE0715-04-51I33-A	04_15_1i_1gb	REV04	1GB	32MB	NA	NA	Low Power DDR
TE0715-04-51I33-AN	04_15_1i_1gb	REV04	1GB	32MB	NA	NA	Low Power DDR. 3M NOVEC coating

TE0715-04-51I33-L	04_15_1i_1gb	REV04	1GB	32MB	NA	NA	Low Power DDR 2.5mm connector
TE0715-04-52I33-A	04_15_2i_1gb	REV04	1GB	32MB	NA	NA	Low Power DDR
TE0715-04-71C33-A	04_30_1c_1gb	REV04	1GB	32MB	NA	NA	Low Power DDR
TE0715-04-71I33-A	04_30_1i_1gb	REV04	1GB	32MB	NA	NA	Low Power DDR
TE0715-04-71I33-L	04_30_1i_1gb	REV04	1GB	32MB	NA	NA	Low Power DDR. 2.5mm connector
TE0715-04-73E33-A	04_30_3e_1gb	REV04	1GB	32MB	NA	NA	Low Power DDR
TE0715-04-30-1IY	04_30_1i_1gb	REV04	1GB	32MB	NA	NA	Low Power DDR, without RTC
TE0715-04-51I33-AY	04_15_1i_1gb	REV04	1GB	32MB	NA	NA	Low Power DDR, without RTC
TE0715-04-52I33-AY	04_15_2i_1gb	REV04	1GB	32MB	NA	NA	Low Power DDR, without RTC
TE0715-04-71C33-AY	04_30_1c_1gb	REV04	1GB	32MB	NA	NA	Low Power DDR, without RTC
TE0715-04-71I33-AY	04_30_1i_1gb	REV04	1GB	32MB	NA	NA	Low Power DDR, without RTC
TE0715-04-71I33-LY	04_30_1i_1gb	REV04	1GB	32MB	NA	NA	Low Power DDR. 2.5mm connector, without RTC
TE0715-04-S003	04_30_1i_1gb	REV04	1GB	32MB	NA	NA	CAO: Low Power DDR
TE0715-05-51I33-AN	04_15_1i_1gb	REV05	1GB	32MB	NA	NA	Low Power DDR. 3M NOVEC coating
TE0715-05-71C33-A	04_30_1c_1gb	REV05	1GB	32MB	NA	NA	Low Power DDR
TE0715-04-S015	04_30_1i_1gb	REV04	1GB	32MB	NA	NA	CAO and Low Power DDR
TE0715-05-52I33-A	04_15_2i_1gb	REV05	1GB	32MB	NA	NA	Low Power DDR
TE0715-05-21C33-A	04_12s_1c_1gb	REV05	1GB	32MB	NA	NA	Low Power DDR
TE0715-05-51I33-A	04_15_1i_1gb	REV05	1GB	32MB	NA	NA	Low Power DDR
TE0715-05-71I33-A	04_30_1i_1gb	REV05	1GB	32MB	NA	NA	Low Power DDR
TE0715-05-71I33-L	04_30_1i_1gb	REV05	1GB	32MB	NA	NA	Low Power DDR. 2.5mm connector
TE0715-05-S002C1	04_15_2i_1gb	REV05	1GB	32MB	NA	NA	Low Power DDR
TE0715-05-51I33-L	04_15_1i_1gb	REV05	1GB	32MB	NA	NA	Low Power DDR 2.5mm connector
TE0715-05-73E33-A	04_30_3e_1gb	REV05	1GB	32MB	NA	NA	Low Power DDR
TE0715-05-S003C1	04_15_2i_1gb	REV05	1GB	32MB	NA	NA	CAO:Low Power DDR

*used as reference

Hardware Modules

Design supports following carriers:

Carrier Model	Notes
TE0701	
TE0703*	
TE0705	
TE0706	
TEBA0841-02	

*used as reference

Hardware Carrier

Additional HW Requirements:

Additional Hardware	Notes
USB Cable for JTAG/UART	Check Carrier Board and Programmer for correct type
XMOD Programmer	Carrier Board dependent, only if carrier has no own FTDI

Additional Hardware

Content

For general structure and usage of the reference design, see Project Delivery - AMD devices

Design Sources

Type	Location	Notes
Vivado	<project folder>\block_design <project folder>\constraints <project folder>\ip_lib <project folder>\board_files	Vivado Project will be generated by TE Scripts
Vitis	<project folder>\sw_lib	Additional Software Template for Vitis and apps_list.csv with settings automatically for Vitis app generation
PetaLinux	<project folder>\os\petalinux	PetaLinux template with current configuration

Design sources

Additional Sources

Type	Location	Notes
SI5338	<project folder>\misc\Si5338	SI5338 Project with current PLL Configuration
init.sh	<project folder>\misc\sd\	Additional Initialization Script for Linux (working from sd card only)

Additional design sources

Prebuilt

File	File-Extension	Description
BIF-File	*.bif	File with description to generate Bin-File
BIN-File	*.bin	Flash Configuration File with Boot-Image (Zynq-FPGAs)
BIT-File	*.bit	FPGA (PL Part) Configuration File
Boot Script-File	*.scr	Distro Boot Script file
DebugProbes-File	*.ltx	Definition File for Vivado/Vivado Labtools Debugging Interface
Diverse Reports	---	Report files in different formats
Device Tree	*.dts	Device tree (2 possible, one for u-boot and one for linux)
Hardware-Platform-Description-File	*.xsa	Exported Vivado hardware description file for Vitis and PetaLinux
LabTools Project-File	*.lpr	Vivado Labtools Project File
OS-Image	*.ub	Image with Linux Kernel (On Petalinux optional with Devicetree and RAM-Disk)
Software-Application-File	*.elf	Software Application for Zynq or MicroBlaze Processor Systems

Prebuilt files (only on ZIP with prebult content)

Download

Reference Design is only usable with the specified Vivado/Vitis/PetaLinux version. Do never use different Versions of AMD Software for the same Project.

Reference Design is available on:

- TE0715 "Test Board" Reference Design

Design Flow

Reference Design is available with and without prebuilt files. It's recommended to use TE prebuilt files for first launch.

Trenz Electronic provides a tcl based built environment based on AMD Design Flow.

See also:

- AMD Development Tools#AMDSoftware-BasicUserGuides
- Vivado Projects - TE Reference Design
- Project Delivery.

The Trenz Electronic FPGA Reference Designs are TCL-script based project. Command files for execution will be generated with "_create_win_setup.cmd" on Windows OS and "_create_linux_setup.sh" on Linux OS.

TE Scripts are only needed to generate the vivado project, all other additional steps are optional and can also executed by AMD Vivado/Vitis GUI. For currently Scripts limitations on Win and Linux OS see: Project Delivery Currently limitations of functionality

Caution! Win OS has a 260 character limit for path lengths which can affect the Vivado tools. To avoid this issue, use Virtual Drive or the shortest possible names and directory locations for the reference design (for example "x:\<project folder>")

1. Run _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell:

_create_win_setup.cmd/_create_linux_setup.sh

```
-----------------------Set design paths---------------------------
-- Run Design with: _create_win_setup
-- Use Design Path: <absolute project path>
------------------------------------------------------------------
-----------------------TE Reference
Design--------------------------
------------------------------------------------------------------
-- (0)  Module selection guide, project creation...prebuilt export...
-- (1)  Create minimum setup of CMD-Files and exit Batch
-- (2)  Create maximum setup of CMD-Files and exit Batch
-- (3)  (internal only) Dev
-- (4)  (internal only) Prod
-- (c)  Go to CMD-File Generation (Manual setup)
-- (d)  Go to Documentation (Web Documentation)
-- (g)  Install Board Files from AMD Board Store (beta)
-- (a)  Start  design with unsupported Vivado Version (beta)
-- (x)  Exit Batch (nothing is done!)
----
Select (ex.:'0' for module selection guide):
```

2. Press 0 and enter to start "Module Selection Guide"
3. Create project and follow instructions of the product selection guide, settings file will be configured automatically during this process.
    - optional for manual changes: Select correct device and AMD install path on "design_basic_settings.cmd" and create Vivado project with "vivado_create_project_guimode.cmd"

> ⚠ Note: Select correct one, see also Vivado Board Part Flow

4. Create hardware description file (.xsa file) for PetaLinux project and export to prebuilt folder

run on Vivado TCL (Script generates design and export files into "<project folder>\prebuilt\hardware\<short name>")

```
TE::hw_build_design -export_prebuilt
```

> ⓘ Using Vivado GUI is the same, except file export to prebuilt folder.

5. Create and configure your PetaLinux project with exported .xsa-file, see PetaLinux KICKstart
   - use TE Template from "<project folder>\os\petalinux"
   - use exported .xsa file from "<project folder>\prebuilt\hardware\<short name>" . **Note:** HW Export from Vivado GUI creates another path as default workspace.
   - The build images are located in the "<plnx-proj-root>/images/linux" directory
6. Configure the **boot.scr** file as needed, see Distro Boot with Boot.scr
7. Copy PetaLinux build image files to prebuilt folder
   - copy **u-boot.elf**, **u-boot.dtb, system.dtb**, **image.ub** and **boot.scr** from "<plnx-proj-root>/images/linux" to prebuilt folder

> ⓘ "<project folder>\prebuilt\os\petalinux\<ddr size>" or "<project folder>\prebuilt\os\petalinux\<short name>"

8. Generate Programming Files with Vitis

run on Vivado TCL (Script generates applications and bootable files, which are defined in "test_board\sw_lib\apps_list.csv")

```
TE::sw_run_vitis -all
TE::sw_run_vitis (optional; Start Vitis from Vivado GUI or start with TE Scripts on Vivado TCL)
```

> ⚠ TCL scripts generate also platform project, this must be done manually in case GUI is used. See Vitis

Launch

Programming

> ⚠ Check Module and Carrier TRMs for proper HW configuration before you try any design.
>
> Reference Design is also available with prebuilt files. It's recommended to use TE prebuilt files for first launch.

TE0715-0x-30-xx only: HP IO Banks max power supply voltage is 1.8V.

AMD documentation for programming and debugging: Vivado/Vitis/SDSoC-Xilinx Software Programming and Debugging

Get prebuilt boot binaries

1. Run _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell
2. Press 0 and enter to start "Module Selection Guide"
    a. Select assembly version
    b. Validate selection
    c. Select Create and open delivery binary folder

Note: Folder "<project folder>_binaries_<Article Name>" with subfolder "boot_<app name>" for different applications will be generated

QSPI-Boot mode

Optional for **Boot.bin** on QSPI Flash and **image.ub** and **boot.scr** on **SD** or **USB**.

1. Connect **JTAG** and power on carrier with module
2. Open Vivado Project with "vivado_open_existing_project_guimode.cmd" or if not created, create with "vivado_create_project_guimode.cmd"

run on Vivado TCL (Script programs BOOT.bin on QSPI flash)

```
TE::pr_program_flash -swapp u-boot
TE::pr_program_flash -swapp hello_te0715 (optional)
```

3. Copy **image.ub** and **boot.scr** on **SD** or **USB**
    - use files from "<project folder>_binaries_<Article Name>\boot_linux" from generated binary folder,see: Get prebuilt boot binaries
    - or use prebuilt file location, see "<project folder>\prebuilt\file_location.txt"
4. Set Boot Mode to **QSPI-Boot** and insert **SD** or **USB**.
    - Depends on Carrier, see carrier TRM.

SD-Boot mode

1. Copy **image.ub, boot.scr** and **Boot.bin** on **SD**
    - use files from "<project folder>_binaries_<Article Name>\boot_linux" from generated binary folder,see: Get prebuilt boot binaries
    - or use prebuilt file location, see "<project folder>\prebuilt\file_location.txt"
    - optional: use startup script **init.sh** for **SD**
2. Set Boot Mode to SD-Boot.
    - Depends on Carrier, see carrier TRM.
3. Insert SD-Card in SD-Slot.

JTAG

Not used on this Example.

Usage

1. Prepare HW like described on section Programming

2. Connect UART USB (most cases same as JTAG)
3. Select SD Card as Boot Mode (or QSPI - depending on step 1)

> Note: See TRM of the Carrier, which is used.

> Starting with Petalinux version 2020.1, the industry standard "Distro-Boot" boot flow for U-Boot was introduced, which significantly expands the possibilities of the boot process and has the primary goal of making booting much more standardised and predictable.
> The boot options described above describe the common boot processes for this hardware; other boot options are possible.
> For more information see Distro Boot with Boot.scr

4. Power On PCB

   1. Zynq Boot ROM loads FSBL from SD/QSPI into OCM,

   2. FSBL init PS, programs PL using the bitstream and loads U-boot from SD into DDR,

   3. U-boot loads Linux (**image.ub**) from SD/QSPI/... into DDR

Linux

1. Open Serial Console (e.g. putty)
   - Speed: 115200
   - select COM Port

   > Win OS, see device manager, Linux OS see dmesg | grep tty (UART is *USB1)

2. Linux Console:

   > Note: Wait until Linux boot finished

3. You can use Linux shell now.

```
i2cdetect -y -r 0        (check I2C 1 Bus)
dmesg | grep rtc       (RTC check)
udhcpc                                (ETH0 check)
lsusb                               (USB check)
```

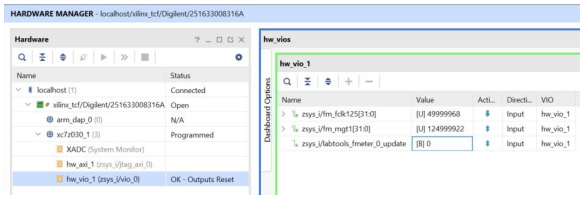
4. Option Features
   - Webserver to get access to Zynq
     - insert IP on web browser to start web interface
   - init.sh scripts
     - add init.sh script on SD, content will be load automatically on startup (template included in "<project folder>\misc\SD")

Vivado HW Manager

Open Vivado HW-Manager and add VIO signal to dashboard (*.ltx located on prebuilt folder).

- Monitoring:
  - Si5338 CLKs:
    - Set radix from VIO signals to unsigned integer. Note: Frequency Counter is inaccurate and displayed unit is Hz

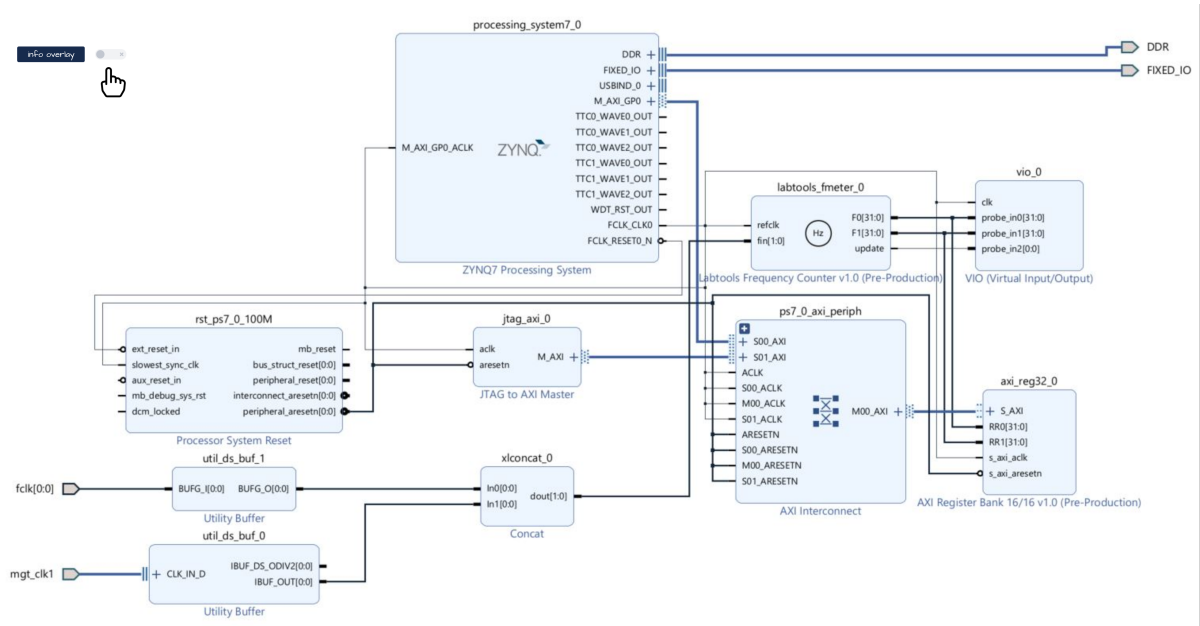
- MGT CLK is configured to 125MHz by default, FCLK is not configured by default (optionally possible over FSBL 50MHz on delivered configuration, see FSBL description).



Vivado Hardware Manager

System Design - Vivado

Block Design



PS Interfaces

Activated interfaces:

Type	Note
DDR	---

QSPI	MIO
I2C1	MIO
UART0	MIO
GPIO	MIO
ETH, USB Rst	MIO
SD0	MIO
USB0	MIO
ETH0	MIO
TTC0..1	EMIO
SWDT	EMIO

PS Interfaces

Constraints

Basic module constraints

_i_bitgen_common.xdc

```
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property CONFIG_VOLTAGE 3.3 [current_design]
set_property CFGBVS VCCO [current_design]

set_property BITSTREAM.CONFIG.USR_ACCESS TIMESTAMP [current_design]
```

_i_unused_io.xdc

```
set_property BITSTREAM.CONFIG.UNUSEDPIN PULLNONE [current_design]
```

Design specific constraints

_i_io.xdc

```
set_property PACKAGE_PIN K2 [get_ports {fclk[0]}]
set_property IOSTANDARD LVCMOS18 [get_ports {fclk[0]}]
set_property CLOCK_DEDICATED_ROUTE FALSE [get_nets fclk_IBUF[0]]
```

_i_timing.xdc

```
# for fmeter only
set_false_path -from [get_clocks clk_fpga_0] -to [get_clocks
mgt_clk1_clk_p]
set_false_path -from [get_clocks mgt_clk1_clk_p] -to [get_clocks
clk_fpga_0]
```

Software Design - Vitis

For Vitis project creation, follow instructions from:

Vitis

Application

Template location: "<project folder>\sw_lib\sw_apps\"

fsbl

TE modified 2022.2 FSBL

General:

- Modified Files: main.c, fsbl_hooks.h/.c (search for 'TE Mod' on source code)
- Add Files: te_fsbl_hooks.h/.c (for hooks and board)
- General Changes:
    - Display FSBL Banner and Device ID

Module Specific:

- Add Files: all TE Files start with te_*
    - SI5338 Configuration

fsbl_flash

TE modified 2022.2 FSBL

General:

- Modified Files: main.c
- General Changes:
    - Display FSBL Banner
    - Set FSBL Boot Mode to JTAG
    - Disable Memory initialisation

hello_te0715

Hello TE0715 is a AMD Hello World example as endless loop instead of one console output.

u-boot

U-Boot.elf is generated with PetaLinux. Vitis is used to generate Boot.bin.

Software Design - PetaLinux

For PetaLinux installation and project creation, follow instructions from:

- PetaLinux KICKstart

Config

Start with **petalinux-config** or **petalinux-config --get-hw-description**

Changes:

- CONFIG_SUBSYSTEM_ETHERNET_PS7_ETHERNET_0_MAC=""

U-Boot

Start with **petalinux-config -c u-boot**

Changes:

- CONFIG_QSPI_BOOT=y
- CONFIG_SD_BOOT=y
- CONFIG_ENV_IS_NOWHERE=y
- CONFIG_ENV_OVERWRITE=y (used to overwrite environment parameter)
- CONFIG_ENV_IS_IN_FAT=y (needed to boot from SD card)
- CONFIG_ENV_IS_IN_SPI_FLASH=y (needed to boot from QSPI flash)
- # CONFIG_ENV_IS_IN_NAND is not set
- CONFIG_BOOT_SCRIPT_OFFSET=0x1920000 (Calculate the start address of partition 3 "bootscr" in the QSPI flash. To do this, add the sizes of partitions 0, 1 and 2 together)
- CONFIG_ZYNQ_MAC_IN_EEPROM=y
- CONFIG_ZYNQ_GEM_I2C_MAC_OFFSET=0xFA
- CONFIG_SYS_I2C_EEPROM_ADDR=0x50

Device Tree (system-user.dtsi in device-tree and uboot-device-tree)

```
/include/ "system-conf.dtsi"
/ {
  chosen {
    xlnx,eeprom = &eeprom;
  };
};

/*------------------- default --------------------*/

/*------------------ QSPI PHY --------------------*/
&qspi {
    #address-cells = <1>;
    #size-cells = <0>;
    status = "okay";
flash0: flash@0 {
        spi-rx-bus-width = <4>;
        spi-tx-bus-width = <4>;
        compatible = "jedec,spi-nor";
        reg = <0x0>;
        #address-cells = <1>;
        #size-cells = <1>;
    };
```

```
};



/*---------------------- ETH PHY ------------------*/
&gem0 {

    status = "okay";
        ethernet_phy0: ethernet-phy@0 {
        compatible = "marvell,88e1510";
        device_type = "ethernet-phy";
                reg = <0>;
    };
};


/*---------------------- USB PHY -----------------*/
/{
    usb_phy0: usb_phy@0 {
        compatible = "ulpi-phy";
        //compatible = "usb-nop-xceiv";
        #phy-cells = <0>;
        reg = <0xe0002000 0x1000>;
        view-port = <0x0170>;
        drv-vbus;
    };
};

&usb0 {
    dr_mode = "host";
    //dr_mode = "peripheral";
    usb-phy = <&usb_phy0>;
};

/*---------------------- I2C ---------------------*/
// i2c PLL: 0x70, i2c eeprom: 0x50

&i2c1 {
  rtc@6F {                      // Real Time Clock
       compatible = "isl12022";
       reg = <0x6F>;
   };

  eeprom: eeprom@50 {           //MAC EEPROM
    compatible = "atmel,24c08";
    reg = <0x50>;
  };
};
```

FSBL patch

Must be add manually --> work in progress

Kernel

Start with **petalinux-config -c kernel**

Changes:

- CONFIG_RTC_DRV_ISL12022=y

Rootfs

Start with **petalinux-config -c rootfs**

Changes:

- CONFIG_i2c-tools=y
- CONFIG_busybox-httpd=y (for web server app)
- CONFIG_usbutils=y
- CONFIG_util-linux-umount=y (uses mount/umount function from util-linux instead of busybox)
- CONFIG_util-linux-mount=y
- CONFIG_auto-login=y

Applications

See "<project folder>\os\petalinux\project-spec\meta-user\recipes-apps\"

startup

Script App to load init.sh from SD Card if available.

webfwu

Webserver application suitable for Zynq access. Need busybox-httpd

Additional Software

SI5338

File location "<project folder>\misc\Si5338\Si5338-*.slabtimeproj"

General documentation how you work with this project will be available on Si5338

Appx. A: Change History and Legal Notices

Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

Date	Document Revision	Authors	Description

Error rendering macro 'page-info'

Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page]

Error rendering macro 'page-info'

Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page]

Error rendering macro 'page-info'

Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page]

- Add Note for Single Core Variants to the Issue List

due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.

due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.

due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.

atlassian . confluence.core. ContentEntityObject]	atlassian . confluence.core. ContentEntityObject]	atlassian . confluence.core. ContentEntityObject]	
2024-05-13	v.43	Manuela Strücker	• Release 2022.2
2023-05-08	v.41	Manuela Strücker	• new Assembly variants
2022-02-09	v.40	Manuela Strücker	• Release 2021.2
2021-12-16	v.39	Manuela Strücker	• new Assembly variants
2021-06-16	v.38	Manuela Strücker	• changed mount /umount function in PetaLinux
2021-05-31	v.37	John Hartfiel	• Design update (bugfix csv file)
2021-05-04	v.36	Manuela Strücker	• Release 2020.2 • added boot.scr for distro boot
2020-06-10	v.33	John Hartfiel	• Release 2019.2
2019-05-09	v.32	John Hartfiel	• Release 2018.3 • FSBL Rework • Script rework • some optional features
2018-10-01	v.31	John Hartfiel	• Release 2018.2 • Redesign Board Part Files • New activate SI5338 example over FSBL • small Design changes • Update Documentation Style

2019-04-06	v.30	John Hartfiel	• New assembly variant
2018-03-27	v.29	John Hartfiel	• Bugfix Board Part Files
2018-02-13	v.28	John Hartfiel	• Release 2017.4
2017-11-10	v.22	John Hartfiel	• Design Update with new options • Add Si5338 section • Update FSBL section
2017-10-19	v.21	John Hartfiel	• Download Update
2017-10-19	v.20	John Hartfiel	• Document style update
2017-10-06	v.18	John Hartfiel	• Text correction • Update Launch section • Supported PCBs
2017-10-02	v.14	John Hartfiel	• Document update on Prebuilt section
2017-09-28	v.13	John Hartfiel	• Initial Release 2017.2
--	all	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.	--

proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.

		Conflue nceUser , class java. lang. String, class com. atlassian . confluen ce.core. Content EntityOb ject] [interfac e com. atlassian .user. User, class java. lang. String, class com. atlassian . confluen ce.core. Content EntityOb ject]	

Document change history.

Legal Notices

Data Privacy

Please also note our data protection declaration at https://www.trenz-electronic.de/en/Data-protection-Privacy

Document Warranty

The material contained in this document is provided “as is” and is subject to being changed at any time without notice. Trenz Electronic does not warrant the accuracy and completeness of the materials in this document. Further, to the maximum extent permitted by applicable law, Trenz Electronic disclaims all warranties, either express or implied, with regard to this document and any information contained herein, including but not limited to the implied warranties of merchantability, fitness for a particular purpose or non infringement of intellectual property. Trenz Electronic shall not be liable for errors or for incidental or consequential damages in connection with the furnishing, use, or performance of this document or of any information contained herein.

Limitation of Liability

In no event will Trenz Electronic, its suppliers, or other third parties mentioned in this document be liable for any damages whatsoever (including, without limitation, those resulting from lost profits, lost data or business interruption) arising out of the use, inability to use, or the results of use of this document, any documents linked to this document, or the materials or information contained at any or all such documents. If your use of the materials or information from this document results in the need for servicing, repair or correction of equipment or data, you assume all costs thereof.

Copyright Notice

Technology Licenses

The hardware / firmware / software described in this document are furnished under a license and may be used /modified / copied only in accordance with the terms of such license.

Environmental Protection

To confront directly with the responsibility toward the environment, the global community and eventually also oneself. Such a resolution should be integral part not only of everybody's life. Also enterprises shall be conscious of their social responsibility and contribute to the preservation of our common living space. That is why Trenz Electronic invests in the protection of our Environment.

REACH, RoHS and WEEE

REACH

Trenz Electronic is a manufacturer and a distributor of electronic products. It is therefore a so called downstream user in the sense of REACH. The products we supply to you are solely non-chemical products (goods). Moreover and under normal and reasonably foreseeable circumstances of application, the goods supplied to you shall not release any substance. For that, Trenz Electronic is obliged to neither register nor to provide safety data sheet. According to present knowledge and to best of our knowledge, no SVHC (Substances of Very High Concern) on the Candidate List are contained in our products. Furthermore, we will immediately and unsolicited inform our customers in compliance with REACH - Article 33 if any substance present in our goods (above a concentration of 0,1 % weight by weight) will be classified as SVHC by the European Chemicals Agency (ECHA).

RoHS

Trenz Electronic GmbH herewith declares that all its products are developed, manufactured and distributed RoHS compliant.

WEEE

Information for users within the European Union in accordance with Directive 2002/96/EC of the European Parliament and of the Council of 27 January 2003 on waste electrical and electronic equipment (WEEE).

Users of electrical and electronic equipment in private households are required not to dispose of waste electrical and electronic equipment as unsorted municipal waste and to collect such waste electrical and electronic equipment separately. By the 13 August 2005, Member States shall have ensured that systems are set up allowing final holders and distributors to return waste electrical and electronic equipment at least free of charge. Member States shall ensure the availability and accessibility of the necessary collection facilities. Separate collection is the precondition to ensure specific treatment and recycling of waste electrical and electronic equipment and is necessary to achieve the chosen level of protection of human health and the environment in the European Union. Consumers have to actively contribute to the success of such collection and the return of waste electrical and electronic equipment. Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.

Trenz Electronic is registered under WEEE-Reg.-Nr. DE97922676.

Error rendering macro 'page-info'

Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]