TEI0006 Test Board

Table of contents

Overview

- 1 Overview
  - 1.1 Key Features
  - 1.2 Revision History
  - 1.3 Supported Boards and Variants
  - 1.4 Requirements
    - 1.4.1 Software
    - 1.4.2 Hardware
  - 1.5 Content
    - 1.5.1 Design Sources
    - 1.5.2 Prebuilt
    - 1.5.3 Download
- 2 Design Flow
- 3 Launch
  - 3.1 Programming
    - 3.1.1 Get prebuilt boot binaries
    - 3.1.2 QSPI
    - 3.1.3 JTAG
  - 3.2 Usage
    - 3.2.1 UART
- 4 System Design - Vivado
  - 4.1 Block Design
- 5 Software Design - SDK
  - 5.1 Application
    - 5.1.1 hello_tei0006
    - 5.1.2 simple_socket_server
    - 5.1.3 Debug
- 6 Appx. A: Change History and Legal Notices
  - 6.1 Document Change History
  - 6.2 Legal Notices
  - 6.3 Data Privacy
  - 6.4 Document Warranty
  - 6.5 Limitation of Liability
  - 6.6 Copyright Notice
  - 6.7 Technology Licenses
  - 6.8 Environmental Protection
  - 6.9 REACH, RoHS and WEEE
- 7 Table of contents

Quartus Design with NIOS V/m and software example "simple_socket_server" and "hello_tei0006".

Refer to http://trm.tebedev.io/tei0006 for the current online version of this manual and other available documentation.

Key Features

- Quartus 22.4 Pro
- NIOS V/m
- UART
- ETH
- QSPI flash memory
- DDR3 memory
- User LED

Revision History

Date	Quartus	Project Built	Authors	Description
2024-01-09	22.4 Pro	TEI0006-test_board-quartus_22.4.0-20240109135625.zip TEI0006-test_board_noprebuilt-quartus_22.4.0-20240109135551.zip	Thomas Dück	• Fixed bugs in TE scripts
2023-12-04	22.4 Pro	TEI0006-test_board_noprebuilt-quartus_22.4.0-20231204134534.zip TEI0006-test_board-quartus_22.4.0-20231204134455.zip	Thomas Dück	• update to Quartus Prime Pro 22.4 • TE scripts update • new assembly variants
2023-04-13	20.4 Pro	TEI0006-test_board_noprebuilt-quartus_20.4.0-20230411171022.zip TEI0006-test_board-quartus_20.4.0-20230411171231.zip	Thomas Dück	• change "Serial Flash Controller II" IP Core to "QUAD SPI Controller II" IP Core • bugfix offset value of hex file

2021-06-15	20.4 Pro	TEI0006-test_board_noprebuilt-quartus_20.4.0-20210615142627.zip TEI0006-test_board-quartus_20.4.0-20210615142455.zip	Thomas Dück	• update to Quartus Prime Pro 20.4 • TE scripts update • new assembly variants
2020-10-19	19.4 Pro	TEI0006-test_board_noprebuilt-quartus_19.4.0-20201019101920.zip TEI0006-test_board-quartus_19.4.0-20201019101840.zip	Thomas Dück	• script update • bugfixes
2020-05-13	19.4 Pro	TEI0006-test_board_noprebuilt-quartus_19.4.0-20200513124953.zip TEI0006-test_board-quartus_19.4.0-20200513125247.zip	Thomas Dück	• TE scripts update
2020-03-09	19.4 Pro	TEI0006-test_board-quartus_19.4-20200309134933.zip TEI0006-test_board_noprebuilt-quartus_19.4-20200309135555.zip	Thomas Dück	• initial release

Design Revision History

Release Notes and Know Issues

Issues	Description	Workaround	To be fixed version
No known issues	---	---	---

Known Issues

Requirements

Software

Software	Version	Note
Quartus Prime Pro	22.4	Nios V/m license is needed. For more information see: Intel Nios V Processors
Ashling RiscFree IDE for Intel FPGAs	22.4	needed

Software

Hardware

Complete List is available on <project folder>/board_files/*_devices.csv

Design supports following modules:

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	Others	Notes
TEI0006-03-220-5I*	220_5I_2GB	REV03|REV02|REV01	2GB	128MB	--	--
TEI0006-03-APC13-R	APC13R	REV03	128MB	128MB	--	without ETH PHY
TEI0006-03-ANC13-R	ANC13R	REV03	128MB	128MB	--	without ETH PHY
TEI0006-03-ALC13-R	ALC13R	REV03	128MB	128MB	--	without ETH PHY
TEI0006-03-ALC13	ALC13	REV03	128MB	128MB	--	--
TEI0006-04-ALC13A	ALC13	REV04	128MB	128MB	--	--
TEI0006-04-ALE13A	ALE13	REV04	128MB	128MB	--	--
TEI0006-04-ANE13A	ANE13	REV04	128MB	128MB	--	--
TEI0006-04-APE23A	APE23	REV04	2GB	128MB	--	--
TEI0006-04-API23A	API23	REV04	2GB	128MB	--	--
TEI0006-04-S004	API23R	REV04	2GB	128MB	--	without ETH PHY
TEI0006-04-S005	APE23	REV04	2GB	128MB	--	--
TEI0006-04-S006	BPI23	REV04	2GB	128MB	--	--
TEI0006-04-S007	APE23R	REV04	2GB	128MB	--	without ETH PHY

*used as reference

Hardware Modules

Design supports following carriers:

Carrier Model	Notes
TEIB0006*	

*used as reference

Hardware Carrier

Additional HW Requirements:

Additional Hardware	Notes
USB cable for JTAG/UART	Check Carrier Board and Programmer for correct type
RJ45 ethernet cable	connect carrier board to network

Additional Hardware

Content

For general structure and of the reference design, see Project Delivery - Intel devices

Design Sources

Type	Location	Notes
Quartus	<project folder>/source_files /quartus <project folder>/source_files /<Board Part Short Name> /quartus	Quartus project will be generated by TE Scripts optional, source files for specific assembly variants
Software	<project folder>/source_files /software	Additional software will be generated by TE Scripts

Design sources

Prebuilt

File	File-Extension	Description
SOPC Information File	*.sopcinfo	File with description of the .qsys file to create software for the target hardware
SRAM Object File	*.sof	Ram configuration file
JTAG indirect configuration file	*.jic	Flash configuration file
Diverse Reports	---	Report files in different formats
Software-Application-File	*.elf	Software application for NIOS II processor system

Prebuilt files (only on ZIP with prebult content)

Download

Reference Design is only usable with the specified Quartus version. Do never use different versions of Quartus software for the same project.

Reference Design is available on:

- TEI0006 "Test Board" Reference Design

Design Flow

⚠ Reference Design is available with and without prebuilt files. It's recommended to use TE prebuilt files for first launch.

Trenz Electronic provides a tcl based built environment based on Quartus Design Flow.

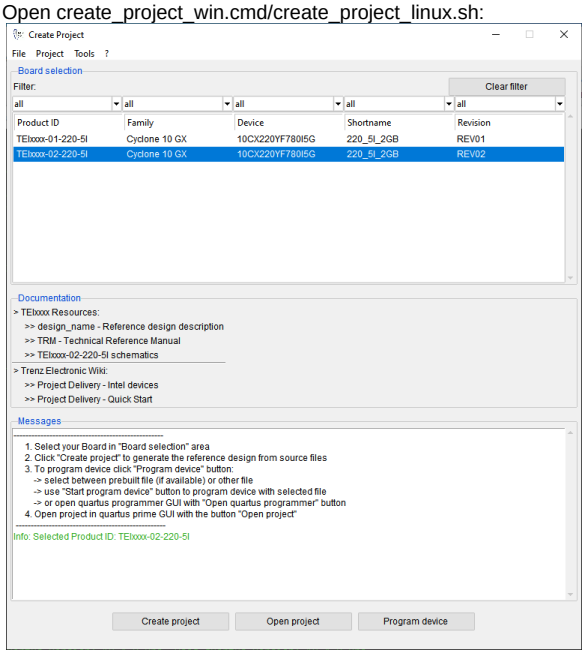
See also:

- Project Delivery - Intel devices

The Trenz Electronic FPGA Reference Designs are TCL-script based projects. To create a project, open a project or program a device execute "create_project_win.cmd" on Windows OS and "create_project_linux.sh" on Linux OS.

TE Scripts are only needed to generate the quartus project, all other additional steps are optional and can also executed by Intel Quartus/SDK GUI. For currently Scripts limitations on Win and Linux OS see: Project Delivery - Intel devices Currently limitations of functionality

1. Open create_project_win.cmd/create_project_linux.sh:



'Create Project' GUI example

2. Select Board in "Board selection"
3. Click on "Create project" button to create project
    a. (optional for manual changes) Select correct quartus installation path in "<project folder>/settings/design_basic_settings.tcl"

Launch

Programming

Check Module and Carrier TRMs for proper HW configuration before you try any design.

Reference Design is also available with prebuilt files. It's recommended to use TE prebuilt files for first launch.

Get prebuilt boot binaries

1. Run create_project_win.cmd/create_project_linux.sh
2. Select a Module in 'Board selection'
3. Click on the 'Export prebuilt files' button

a. Folder <*project folder*>/_binaries_<*Article Name*> with subfolder *boot_linux* will be generated and opened

QSPI

1. Connect JTAG and power on carrier with module
2. Open create_project_win.cmd/create_project_linux.sh
3. Select correct board in "Board selection"
4. Click on "Program device" button
    a. if prebuilt files are available: select "Program prebuilt file"
    b. using own generated programming file: select "Program other file" and click on "Browse ..." to open own generated programming file
    c. (optional) click on "Open programmer GUI" to program device with Quartus programmer GUI
5. Click on "Start program device" button

JTAG

Not used on this Example.

Usage

1. Prepare HW like described on section Programming
2. Connect UART USB (most cases same as JTAG)
3. Connect your board to the network
4. Power on PCB

UART

1. Open Serial Console (e.g. PuTTY)
    a. select COM Port

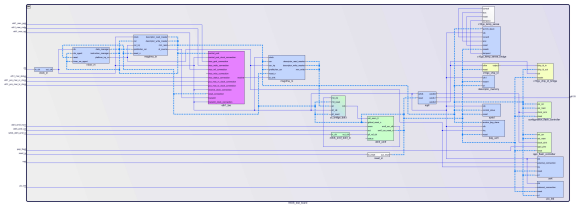
    > Win OS: see device manager
    >
    > Linux OS: see ls -l dev/serial/by-id (UART is *USB1)

    b. Speed: 115200
2. Press reset button
3. Console output depends on used Software project, see Software Design - SDK#Application

System Design - Quartus

Block Design

The block design may differ depending on the assembly variant.



Block Design - NIOS_test_board.qsys

Block Design - Platform Designer

Software Design - SDK

Application

Used software project depends on board assembly variant. Template location: <project folder> /source_files/software/

hello_tei0006

Hello TEI0006 is a Hello World example as endless loop instead of one console output.

simple_socket_server

Software example "Simple Socket Server" from eclipse (modified source files for TEI0006 board).

- If DHCP Server is not available:
    1. Open software project in sdk gui (e.g. Ashling RiscFree IDE for Intel FPGAs 22.4) and set in the main.c file the varaibles:
        - .use_dhcp = !DEF_TRUE
        - .ipv4_addr_str = <your static IP address>
        - .ipv4_gateway_str =<your gateway>
    2. Rebuild the software project and download the *.elf file to the device.
    3. Open the command shell and enter "telnet <ip_address> 80" to connect to the simple socket server

Appx. A: Change History and Legal Notices

Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

Date	Document Revision	Authors	Description
Error rendering macro 'page-info' Ambiguous method overload	**Error rendering macro 'page-info'** Ambiguous method overload	**Error rendering macro 'page-info'** Ambiguous method overload	• update to Quartus Prime Pro 22.4 • new assembly variants

ing for method jdk.proxy24.$Proxy3572#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interfac

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. confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	. confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	. confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	
2023-04-13	v.12	Thomas Dück	• Design files update

2021-07-26	v.10	Thomas Dück	• update to Quartus Prime Pro 20.4 • new assembly variants • document style update • script update
2020-10-19	v.6	Thomas Dück	• script update • bugfixes
2020-05-13	v.5	Thomas Dück	• Design files update
2020-03-18	v.4	Thomas Dück	• initial release 19.4
--	all	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy24.$Proxy3572#hasContentLevelPermission. Cannot resolve which method to	--

invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.

		Content EntityOb ject] [interfac e com. atlassian .user. User, class java. lang. String, class com. atlassian . confluen ce.core. Content EntityOb ject]	

Document change history

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Error rendering macro 'page-info'

Ambiguous method overloading for method jdk.proxy244.$Proxy3572#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]