Arduino with VIRTEX-7



Why should anyone want to run Arduino code on Virtex-7 ever you may ask? Let's look the prices first: as of current listing XC7VX330T-2FFG1157C costs 3204 USD or 2366 EUR.

On my desk there is a PCB board that did come from our Vapor Phase oven yesterday. On the board there is a LED. This LED blinks, it says hello, I am alive. There is a chip on the board, and on that it reads: XC7VX330T-2FFG1157C

Lets look closer how the LED was made to Blink. Why it makes sense I tell another day.

Step 1: Hardware Design



I have dropped Xilinx Microblaze MCS onto the Block design. all the Interface ports to the real hardware (clock, reset and LED) are connected automatically using Vivado Board Part Interface flow. So for making this hardware design, there is nothing to look in any documents, just select the Board to work with, and go. All constraints are managed by Vivado. We can now just run generate bitstream.



Design is implemented, we go to software design flow now.

Step 2: From Hardware to Software

As soon as Vivado has generate the output products and bitstream we can move from Hardware design to Software. In Vivado Export and Launch SDK. We create new BSP and select Arduino System Library to be included.

Board Support Package Settings				X
Board Support Package Settings Control various settings of your Board Suppo	ort Package.			
 Overview standalone arduino drivers design_1_microblaze_mcs_0_0 	standalone_bsp_0 OS Type: standalo OS Version: 4.1 ▼ Hardware Specificatio Processor: Check the box next th Name ♥ arduino	ne bn: B:\hw\2014. design_1_mi to the libraries yn Version 1.0 2.1 2.1 4.0 4.0 2.0	Standalone is a simple, low-level software layer. It provides acc caches, interrupts and exceptions as well as the basic features of input and output, profiling, abort and exit. 2\project_4\project_4.sdk\design_1_microblaze_mcs_0_0_hw_plat croblaze_mcs_0_0 bu want included in your Board Support Package.You can config Description Arduino System Library IwIP TCP/IP Stack library: IwIP v1.4.0, Xilinx adapter v Generic Fat File System Library Xilinx In-system and Serial Flash Library Xilinx Memory File System	ress to basic processor features such as of a hosted environment, such as standard atform_0\system.xml gure the library in the navigator on the left.
	xilskey	2.0	Xilinx Secure Key Library	
?				OK Cancel

Now we are ready to write some Arduino Code! A LED Blinky would do for now.

K C/C++ - Arduino_Virtex7/src/Arduino_Virtex7.cpp - Xilinx	DK	
<u>File Edit Source Refactor N</u> avigate Se <u>a</u> rch <u>R</u> un <u>F</u>	roject <u>X</u> ilinx Tools <u>W</u> indow <u>H</u> elp	
¹ ▼ 및 № ▲ ≫ ▼ % ▼ ⋒ @ ▼ 8 ▼ ∮ ▼ ∛ ▼ や ◆ ▼ → ▼	° • ° • ∲ • 0 • 4 • 8 ≥ # ⊠ ■ 6 ≥ / 2	〕 🗐 🍸 🕆 Debug 🕞 C/C++)
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4	🖹 Problems 🔕 Tasks 📮 Console 🔲 Properties 🕴 🥒 Terminal 1 📗 SDK Log	📴 🎝 🖾 🔁 🗖 🗖
📥 Target Connections 🕱 🛛 🔹 🖉 🗖 🗖	Property Value	
Local [default]		
	< III	
	Writable Smart Insert 19:1	

Done, we select debug-as and start in Debugger. LED Blinks!

Flash Programming

How about Programming the Arduino code into the Flash memory so that it starts when FPGA loads? First we have to tell Vivado what Software file we want to use, so we associate the proper ELF File.

🚴 Associate ELF File					
Associate an ELF file with a processor instance	(Address Map). ELF files are available after running generate on your embedded design sources.				
ELF File Associations					
Processors/Address Maps	Associated ELF File				
⊡· 🔂 Design Sources					
microblaze_mcs_0/U0/microblaze_I	Arduino_Virtex7.elf				
🗄 🛅 Simulation Sources					
		-			
	OK Cancel				

Now we tell Vivado what Flash Memory is used on our board:

🚴 Add Configura	ation Memory Device								x
Choose a	configuration memory part. This	s can be changed la	ater.						
Device: 🛞 xc7vx	:330t_0								
Manufacturer	Micron	*			Туре	spi		-	-
Density (Mb)	All	-			Width	All		-	
			Reset All	Filters					
-Select Configuratio	on Memory Part								
Search: Q.									0
Name		Part	Manufacturer	Alias	Family	Туре	Density (Mb)	Width	
🥦 n25q256-1.8v-s	spi-x1_x2_x4	n25q256-1.8v	Micron		n25q	spi	256	x1_x2_x4	
🌾 n25q128-1.8v-s	spi-x1_x2_x4	n25q128-1.8v	Micron		n25q	spi	128	x1_x2_x4	
🌼 mt25ql512-spi-x	x1_x2_x4	mt25ql512	Micron		mt25qu	spi	512	x1_x2_x4	
🌼 mt25qu512-spi-	x1_x2_x4	mt25qu512	Micron		mt25qu	spi	512	x1_x2_x4	
							ОК	Canc	:el

And ready we are to write the Flash memory. Almost.. there is one step still required that currently is not available from the menus. So single line of TCL code should be executed.



So the BIT file is converted to MCS and ready for flashing!

🚴 Program Configuration Memory Device						
Select a configuration file and	Select a configuration file and set programming options.					
Memory Device:						
Configuration file:	B:/hw/2014.2/project_4/Virtex7-Arduino-Blinky.mcs					
State of non-config mem IO pins:	Pull-none 💌					
Program Operations						
Address Range: Configuration F	ile Only 🔻					
🔽 Erase						
Blank Check						
Program						
Verify						
	~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~					
	OK Cancel					

Click OK to Program..



#### And ready we are. Now lets try power cycle - power off, power on.. and LED Blinks again.

### Xilinx Virtex-7 has configured itself with Arduino Code and Says "Blink..Blink" to all of us.

And what did I miss in the process? I forgot to set the bitstream options, so it did take painfully long (About 1 minute to load the bitstream!) to start after cold restart. So here some screenshots of the property settings:

Configuration Setup         Configuration Rate (MHz)         Enable external configuration dock and set divide value         DISABLE ▼         Configuration Voltage         1.8 ▼         Configuration Bank Voltage Selection         GPU ▼         BPI Configuration         Ist Read cyde         I ▼         Page Size (bytes)         I ▼         Synchronous Mode         DISABLE ▼         Synchronous Mode         DISABLE ▼         Spit Configuration         Enable SPI 32-bit address style         Bus width         4 ▼         Enable the FPGA to use a failing edge dock for SPI data capture         NO ▼         HultiBoot Settings         Load a failback bitstream when a configuration attempt fails         DISABLE ▼         Specify the internal value of the RS[1:0] settings in the Warm Boot Start Address         Specify the internal value of the RS[1:0] settings in the Warm Boot Start Address         DONE PIN       PLLLP         Watchdog Timer value in Configuration mode         Configuration PIN Settings during User Mode         Cdk Pin       PLLLP         NO Pin       PLLLIP         NO Pin       PLLLIP	Configuration			
Configuration Rate (MHz)       66 \u2207         Enable external configuration dock and set divide value [DISABLE \u2207         Configuration Voltage       1.8 \u2207         Configuration Bank Voltage Selection       GMD \u2207         PPT Configuration       Ist Read cycle         Ist Read cycle       1 \u2207         Page Size (bytes)       1 \u2207         Synchronous Mode       DISABLE \u2207         SPT Configuration       Ist Read cycle         Ist Read cycle       1 \u2207         Synchronous Mode       DISABLE \u2207         SPT Configuration       Ist Read cycle         Ist Read cycle       N \u2207         Bus width       4 \u2207         Bus width       4 \u2207         HultiBoot Settings       Ist Configuration is a configuration attempt fails         Ist ring address for the next configuration is a MultiBoot setup       Ist Robue         Specify the internal value of the RS[1:0] settings in the Warm Boot Start Address       ISt Robue         Specify the internal value of the RS[1:0] settings in the Warm Boot Start Address       ISt Robue         Watchdog Timer value in Configuration mode       INTOPIN         Watchdog Timer value in Configuration mode       INTOPIN         NDNE Pin       PULLUP \u2207         ND Pin <th></th> <th></th> <th></th> <th></th>				
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INIT PinPULLUPM0 PinPULLUPM1 PinPULLUPM2 PinPULLUPPROGRAM PinPULLUPTCK PinPULLUPTDI PinPULLUPTDO PinPULLUP	DONE Pin	PULLUP 👻		
M0 Pin     PULLUP       M1 Pin     PULLUP       M2 Pin     PULLUP       PROGRAM Pin     PULLUP       TCK Pin     PULLUP       TDI Pin     PULLUP       TDO Pin     PULLUP	INIT Pin	PULLUP 👻		
M1 Pin     PULLUP       M2 Pin     PULLUP       PROGRAM Pin     PULLUP       TCK Pin     PULLUP       TDI Pin     PULLUP       TDO Pin     PULLUP	M0 Pin	PULLUP 🔻		
M2 Pin     PULLUP       PROGRAM Pin     PULLUP       TCK Pin     PULLUP       TDI Pin     PULLUP       TDO Pin     PULLUP	M1 Pin	PULLUP 👻		
PROGRAM Pin     PULLUP       TCK Pin     PULLUP       TDI Pin     PULLUP       TDO Pin     PULLUP	M2 Pin	PULLUP 👻		
TCK Pin     PULLUP       TDI Pin     PULLUP       TDO Pin     PULLUP	PROGRAM Pin	PULLUP 👻		
TDI Pin     PULLUP       TDO Pin     PULLUP	TCK Pin	PULLUP 🔻		
TDO Pin PULLUP 🔻	TDI Pin	PULLUP 👻		
	TDO Pin	PULLUP 🔻		

	Misc Settings		
	Digitally Controlled Impedance (DCI) circuit match frequency	ASREQUIRED 🔻	-
		OK Undo All	lelp

🚴 Edit Device Properties		×
Q- General Configuration Configuration Modes Startup Encryption Readback	General         Bitstream Properties         Enable Bitstream Compression         Enable Quic Redundancy Checking (CRC)         Enable debugging of Serial mode Bitstream         Disable communication to the Boundary Scan (BSCAN) block via JTAG         Enable JTAG Connection to XADC         Enable Single Erame Cyclic Redundancy Checking (CRC)         Enable Single Erame Cyclic Redundancy Checking (CRC)         Enable Enhanced Linearity for XADC	TRUE   ENABLE  NO  NO  ENABLE  NO  COFF
	Enable <u>X</u> ADC Power Down	DISABLE 🔻
		OK Undo All Help

A small hint: those properties are not always accessible, so if you can not find them, just run the flow and open implemented design.