TEBF0818 CPLD

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Overview

Firmware for PCB-Master CPLD with designator U17. Use first CPLD Device in Chain: LCMX02-1200HC.

Firmware for PCB-Slave CPLD with designator U39. Use second CPLD Device in Chain: LCMX02-1200HC.

There are 3 different Firmware variants available:

1. (Default): SCM_xA_default.jed/SCS_xA_default.jed
2. (optional): SCM_xB_powerdown_disabled.jed/SCS_xB_powerdown_disabled.jed - Power down Sequencing is disabled (See Note Power Management).
3. (optional): SCM_xC_msdboot_disabled.jed/SCS_xC_msdboot_disabled.jed - CD Pin of MicroSD will not influence boot Mode (mircoSD can be used as Filesystem and system Boots from QSPI)

Feature Summary

- Power Management (Slave CPLD)
- Reset Management (both)
- CPLD JTAG (both)
- FMC JTAG / PJTAG (Master CPLD)
- FMC VADJ Power (Master CPLD)
- Boot Mode (Slave CPLD)
- PCIe (Slave CPLD)
- SD (both)
- UART SoC (Slave CPLD)
- UART (Debug) (Master CPLD)
- CAN (Master CPLD)
- USB (Master CPLD)
- DisplayPort (Master CPLD)
- SFP (Master CPLD)
- I2C (Master CPLD)
- LEDs (both)
- RGPIO (both)

Firmware Revision and supported PCB Revision

See Document Change History

Product Specification

Port Description

Name / opt. VHD Name	Direction	Pin	Bank Power	Description	CPLD
C_T1		24	3V3SB	/ currently_not_used	U17
C_T2		26	3V3SB	/ currently_not_used	U17
C_T3		25	3V3SB	/ currently_not_used	U17
C_TCK	in	131	3V3SB	JTAG J28 (XMOD2) / FMC JTAG	U17
C_TDI	in	136	3V3SB	JTAG J28 (XMOD2) / FMC JTAG	U17
C_TDO1 / C_TDO	out	137	3V3SB	JTAG J28 (XMOD2) / FMC JTAG	U17
C_TMS	in	130	3V3SB	JTAG J28 (XMOD2) / FMC JTAG	U17
CAN_FAULT		106	3V3SB	CAN	U17
CAN_RX	in	107	3V3SB	CAN	U17
CAN_S	out	105	3V3SB	CAN	U17
CAN_TX	out	104	3V3SB	CAN	U17
CLK_125MHz / PHY_CLK	in	70	1.8V	/ currently_not_used	U17
CON_NTRST / JTAG_TRST	in	117	3V3SB	JTAG, Connector J30	U17
CON_RTCK / JTAG_RTCK	out	125	3V3SB	JTAG, Connector J30	U17
CON_sRST / JTAG_SRST	in	127	3V3SB	JTAG, Connector J30	U17
CON_TCK / JTAG_TCK	in	122	3V3SB	JTAG, Connector J30	U17
CON_TDI / JTAG_TDI	in	119	3V3SB	JTAG, Connector J30	U17
CON_TDO / JTAG_TDO	out	126	3V3SB	JTAG, Connector J30	U17
CON_TMS / JTAG_TMS	in	121	3V3SB	JTAG, Connector J30	U17

DIR_T1		23	3V3SB	/ currently_not_used	U17
DIR_T2		28	3V3SB	/ currently_not_used	U17
DIR_T3		27	3V3SB	/ currently_not_used	U17
DP_AUX_DE / DP_DE	out	92	3V3SB	Display Port	U17
DP_AUX_RX / DP_RX	in	91	3V3SB	Display Port	U17
DP_AUX_TX / DP_TX	out	93	3V3SB	Display Port	U17
DP_EN	out	77	3V3SB	Display Port	U17
DP_TX_HPD / DP_HPD	in	94	3V3SB	Display Port	U17
ETH_RST	out	62	1.8V	ETH Reset	U17
EX_IO1		112	3V3SB	/ currently_not_used	U17
EX_IO2		113	3V3SB	/ currently_not_used	U17
EX_IO3		114	3V3SB	/ currently_not_used	U17
EX_IO4		115	3V3SB	/ currently_not_used	U17
F2_EN	out	19	3V3SB	FAN2	U17
F2PWM	out	20	3V3SB	FAN2	U17
F2SENSE	in	21	3V3SB	FAN2	U17
FMC_CLK_DIR / FMC_CLKDIR	in	73	3V3SB	FMC	U17
FMC_TCK	out	95	3V3SB	FMC	U17
FMC_TDI	out	96	3V3SB	FMC	U17
FMC_TDO	in	97	3V3SB	FMC	U17
FMC_TMS	out	98	3V3SB	FMC	U17
FMC_VID0	out	139	3V3SB	FMC	U17
FMC_VID1	out	140	3V3SB	FMC	U17
FMC_VID2	out	141	3V3SB	FMC	U17
GND		84	3V3SB	REV03 unconnected / currently_not_used	U17
HDIO_SC10 / SC10	out	60	1.8V	FPGA / DP_RX or 'Z'	U17
HDIO_SC11 / SC11	in	59	1.8V	FPGA / DP_DE	U17
HDIO_SC12 / SC12	out	58	1.8V	FPGA / DP_HPD	U17
HDIO_SC13 / SC13	out	57	1.8V	FPGA / RGPIO TX	U17
HDIO_SC14 / SC14	in	56	1.8V	FPGA / RGPIO RX	U17
HDIO_SC15 / SC15	in	55	1.8V	FPGA / RGPIO CLK	U17
HDIO_SC16 / SC16	in	54	1.8V	FPGA / CAN_S	U17
HDIO_SC17 / SC17	in	52	1.8V	FPGA / XMOD LED	U17
HDIO_SC18 / SC18	in	68	1.8V	FPGA / CAN_TX	U17
HDIO_SC19 / SC19	out	69	1.8V	FPGA / CAN_RX	U17
I2C_RST	out	61	1.8V	I2C	U17
JTAGENB		120	3V3SB	external Pin for CPLD Firmware Update	U17
LED_1A / JLED1	out	109	3V3SB	USB3.0 LED Jellow	U17
LED_2A / JLED2A	out	111	3V3SB	USB3.0 LED Green/Orange	U17
LED_2B / JLED2B	out	110	3V3SB	USB3.0 LED Green/Orange	U17

MIO26	out	41	1.8V	MIO / PJTAG	U17
MIO27	out	40	1.8V	MIO / PJTAG	U17
MIO28	in	39	1.8V	MIO / PJTAG	U17
MIO29	out	38	1.8V	MIO / PJTAG	U17
OCLK_EN / OSC_EN	out	74	3V3SB	Programmable Oscillator U45	U17
PHY_CONFIG	out	65	1.8V	ETH PHY	U17
PHY_LED0	in	67	1.8V	ETH PHY	U17
PHY_LED1	in	86	3V3SB	ETH PHY	U17
PHY_LED2	in	85	3V3SB	ETH PHY	U17
SC_CLK0 / CLK0	in	76	3V3SB	/ currently_not_used	U17
SC_CLK1 / CLK1	in	75	3V3SB	/ currently_not_used	U17
SC_IO0 / X0	out	50	1.8V	MTS dummy	U17
SC_IO1 / X1	in	49	1.8V	internal cpld RGPIO CLK	U17
SC_IO2 / X2	out	48	1.8V	internal cpld RGPIO TX	U17
SC_IO3 / X3	in	47	1.8V	internal cpld RGPIO RX	U17
SC_IO4 / X4	out	45	1.8V	SD WP to slave cpld	U17
SC_IO5 / X5	in	44	1.8V	STM dummy	U17
SC_IO6 / X6	out	43	1.8V	/ currently_not_used	U17
SC_IO7 / X7	out	42	1.8V	/ currently_not_used	U17
SC_IO8 / X8	in	22	3V3SB	internal cpld RGPIO available(1.8V on)	U17
SC_SCL / SCL	in	14	3V3SB	I2C Mux U27 / currently_not_used	U17
SC_SDA / SDA	in	13	3V3SB	I2C Mux U27 / currently_not_used	U17
SC2_SW3 / SW3	in	6	3V3SB	DIP-Switch S5-3	U17
SC2_SW4 / SW4	in	5	3V3SB	DIP-Switch S5-4	U17
SD_WP	in	100	3V3SB	MMC SD WP	U17
SFP_LED1 / SFP_LED0	out	81	3V3SB	SFP	U17
SFP_LED2 / SFP_LED1	out	82	3V3SB	SFP	U17
SFP_LED3 / SFP_LED2	out	78	3V3SB	SFP	U17
SFP_LED4 / SFP_LED3	out	83	3V3SB	SFP	U17
SFP1_LOS		32	3V3SB	SFP / currently_not_used	U17
SFP1_TX_DIS	out	33	3V3SB	SFP	U17
SFP2_LOS		35	3V3SB	SFP / currently_not_used	U17
SFP2_TX_DIS	out	34	3V3SB	SFP	U17
STAT_LED0 / LED0	out	99	3V3SB	LED D4 Green	U17
STAT_LED1 / LED1	out	128	3V3SB	LED D1 Red	U17
USB0_RST / USB_TRST		71	1.8V	USB (U9) PHY Reset	U17
USBH_LED_G3		11	3V3SB	USB Hub (U4) / currently_not_used	U17
USBH_LED_G4		12	3V3SB	USB Hub (U4) / currently_not_used	U17
USBH_LED_SS1		9	3V3SB	USB Hub (U4) / currently_not_used	U17
USBH_LED_SS2		133	3V3SB	USB Hub (U4) / currently_not_used	U17

USBH_LED_SS3		132	3V3SB	USB Hub (U4) / currently_not_used	U17
USBH_LED_SS4		138	3V3SB	USB Hub (U4) / currently_not_used	U17
USBH_MODE0	out	142	3V3SB	USB Hub (U4)	U17
USBH_MODE1	out	143	3V3SB	USB Hub (U4)	U17
USBH_RST	out	10	3V3SB	USB Hub (U4)	U17
XMOD1_A / XMOD_TXD	out	3	3V3SB	J28 (XMOD 2 UART)	U17
XMOD1_B / XMOD_RXD	in	2	3V3SB	J28 (XMOD 2 UART)	U17
XMOD1_E / XMOD_E	out	4	3V3SB	J28 (XMOD 2 LED)	U17
XMOD1_G / XMOD_G	out	1	3V3SB	J28 (XMOD 2 Button)	U17
1.8V_EN / EN_1V8	out	106	3V3SB	Enable 1.8V Power	U39
5V_EN / EN_5V	out	115	3V3SB	Enable 5V Power, can be permanently enabled by S4-4	U39
C_TCK		131	3V3SB	JTAG J28 (XMOD2) / currently_not_used	U39
C_TDO	out	137	3V3SB	JTAG J28 (XMOD2)	U39
C_TDO1 / C_TDI	in	136	3V3SB	JTAG J28 (XMOD2)	U39
C_TMS		130	3V3SB	JTAG J28 (XMOD2) / currently_not_used	U39
CLK_A / AUD_CLK	out	1	1.8V	AUDIO U3 CLK	U39
CLK_CPLD / MEMS_CLKIN	in	128	3V3SB	U25 24,576MHz	U39
DONE	in	67	1.8V	PS Done	U39
EN_DDR	out	86	3V3SB	Enable Module DDR Power	U39
EN_FMC / FMC_EN	out	104	3V3SB	FMC	U39
EN_FPD	out	81	3V3SB	Enable Module PS FPD Power	U39
EN_GT_L	out	77	3V3SB	Enable Module GT Power	U39
EN_GT_R	out	93	3V3SB	Enable Module GT Power	U39
EN_LPD	out	84	3V3SB	Enable Module PS LPD Power	U39
EN_PL	out	95	3V3SB	Enable Module PL Power	U39
EN_PLL_PWR	out	78	3V3SB	Enable Module SI5345 Power	U39
EN_PSGT / EN_PSGTR	out	75	3V3SB	Enable Module PS GT Power	U39
ERR_OUT / ERROR	in	70	1.8V	Module PS Error Out / Status	U39
ERR_STATUS / ERR_STAT	in	69	1.8V	Module PS Error Status	U39
F1PWM	out	121	3V3SB	FAN1	U39
F1SENSE	in	125	3V3SB	FAN1	U39
FAN_FMC_EN / FMC_FAN_EN		132	3V3SB	FMC FAN	U39
FMC_PG_C2M	out	141	3V3SB	FMC PG	U39
HD_LED_N / HDLED_N	out	112	3V3SB	J10 HD LED	U39
HD_LED_P / HDLED_P	out	110	3V3SB	J10 HD LED	U39
HDIO_SC0 / SC0	in	32	1.8V	FPGA IO / forward to HD_LED_P / HDLED_P	U39
HDIO_SC1 / SC1	in	33	1.8V	/ currently_not_used	U39
HDIO_SC2 / SC2	in	34	1.8V	/ currently_not_used	U39
HDIO_SC3		35	1.8V	/ currently_not_used	U39
HDIO_SC4		25	1.8V	/ currently_not_used	U39

HDIO_SC5 / SC5	out	26	1.8V	FPGA IO / RGPIO	U39
HDIO_SC6 / SC6	in	27	1.8V	FPGA IO / RGPIO CLK	U39
HDIO_SC7 / SC7	in	28	1.8V	.FPGA IO / RGPIO	U39
I2C_SCL / SCL	in	50	1.8V	I2C / currently_not_used	U39
I2C_SDA / SDA	in	52	1.8V	I2C / currently_not_used	U39
INIT_B / INIT	in	68	1.8V	Module PS Init_B	U39
JTAGENB		120	3V3SB	external Pin for CPLD Firmware Update	U39
LP_GOOD / PG_LPD	in	83	3V3SB	Module LP Power Good	U39
MIO24		38	1.8V	MIO / currently_not_used	U39
MIO25		39	1.8V	MIO / currently_not_used	U39
MIO30	in	48	1.8V	MIO / USB Reset	U39
MIO31	in	49	1.8V	MIO / PCIe Reset	U39
MIO32		40	1.8V	MIO / currently_not_used	U39
MIO33		41	1.8V	MIO / currently_not_used	U39
MIO34		42	1.8V	MIO / currently_not_used	U39
MIO35		43	1.8V	MIO / currently_not_used	U39
MIO36		44	1.8V	MIO / currently_not_used	U39
MIO37		45	1.8V	MIO / currently_not_used	U39
MIO40	in	54	1.8V	MIO	U39
MIO41		55	1.8V	MIO / currently_not_used	U39
MIO42	out	60	1.8V	MIO	U39
MIO43	in	61	1.8V	MIO	U39
MIO44		47	1.8V	MIO	U39
MOD_EN	out	119	3V3SB	Enable Main Module Power 3.3V	U39
MODE0	out	6	1.8V	Module Boot Mode	U39
MODE1	out	9	1.8V	Module Boot Mode	U39
MODE2	out	10	1.8V	Module Boot Mode	U39
MODE3	out	11	1.8V	Module Boot Mode	U39
MR / MRESETn	out	92	3V3SB	Module PS Power Reset	U39
PCI_SFP_EN	out	76	3V3SB	SFP	U39
PER_EN	out	117	3V3SB	Enable 3.3V power	U39
PERST / PERSTn	out	139	3V3SB	PCIE Resetn	U39
PG_DDR	in	91	3V3SB	Module Power Good	U39
PG_FPD	in	85	3V3SB	Module Power Good	U39
PG_GT_L	in	96	3V3SB	Module Power Good	U39
PG_GT_R	in	94	3V3SB	Module Power Good	U39
PG_PL	in	82	3V3SB	Module Power Good	U39
PG_PLL_1V8 / PG_PLL	in	73	3V3SB	Module Power Good	U39
PG_PSGT	in	74	3V3SB	Module Power Good	U39
PLL_LOLn / PLL_LOL	in	58	1.8V	Module PLL / currently_not_used	U39

PLL_RST / PLL_RSTn	out	56	1.8V	Module PLL Reset	U39
PLL_SEL0	out	57	1.8V	Module PLL	U39
PLL_SEL1	out	59	1.8V	Module PLL	U39
POK_1V8	in	107	3V3SB	Carrier Power Good	U39
POK_FMC	in	99	3V3SB	FMC Power Good	U39
PROG_B	OUT	71	1.8V	Module PS_PROG_B	U39
PSON	out	105	3V3SB	ATX J20 PS_ON_N	U39
PWR_BTN	in	113	3V3SB	Power Button S1 or J10	U39
PWRLED_N / LED_N	out	111	3V3SB	J10 PWR	U39
PWRLED_P / LED_P	out	109	3V3SB	J10 PWR	U39
PWROK	in	100	3V3SB	ATX J20 PWROK	U39
RST_BTN	in	114	3V3SB	Reset Button S2 or J10	U39
S_1		127	3V3SB	BEEPER / currently_not_used	U39
SC_IO0 / X0	in	12	1.8V	MTS dummy	U39
SC_IO1 / X1	out	13	1.8V	internal cpld RGPIO CLK	U39
SC_IO2 / X2	in	14	1.8V	internal cpld RGPIO RX	U39
SC_IO3 / X3	out	20	1.8V	internal cpld RGPIO TX	U39
SC_IO4 / X4	in	21	1.8V	MMC SD WP from master	U39
SC_IO5 / X5	out	22	1.8V	STM dummy	U39
SC_IO6 / X6	in	23	1.8V	/ currently_not_used	U39
SC_IO7 / X7	in	24	1.8V	/ currently_not_used	U39
SC_IO8 / X8	out	126	3V3SB	internal cpld RGPIO available(1.8V on)	U39
SC2_SW1 / SW1	in	133	3V3SB	S5-1 / Boot Mode Selection	U39
SC2_SW2 / SW2	in	138	3V3SB	S5-2 / Boot Mode Selection	U39
SD_A_EN	out	140	3V3SB	Micro SD	U39
SD_B_EN	out	122	3V3SB	MMC SD	U39
SD_CD / SD_CD_OUT	out	65	1.8V	SD Card detect to FPGA	U39
SD_CD_B	in	143	3V3SB	MMC SD CD	U39
SD_CD_S	in	142	3V3SB	Micro SD CD	U39
SEL_SD / SD_SEL	out	62	1.8V	SD select (Mirco or MMC)	U39
SRST_B / SRSTn	out	19	1.8V	Module PS_SRST_B	U39
STAT_LED2 / LED2	out	98	3V3SB	LED D6 Green	U39
STAT_LED3 / LED3	out	97	3V3SB	LED D7 Red	U39
XMOD2_A / XMOD_TXD	out	5	1.8V	J12 (XMOD 1 UART)	U39
XMOD2_B / XMOD_RXD	in	4	1.8V	J12 (XMOD 1 UART)	U39
XMOD2_E / XMOD_LED	out	3	1.8V	J12 (XMOD 1 LED)	U39
XMOD2_G / XMOD_BTN	in	2	1.8V	J12 (XMOD 1 Button)	U39

Functional Description

JTAG

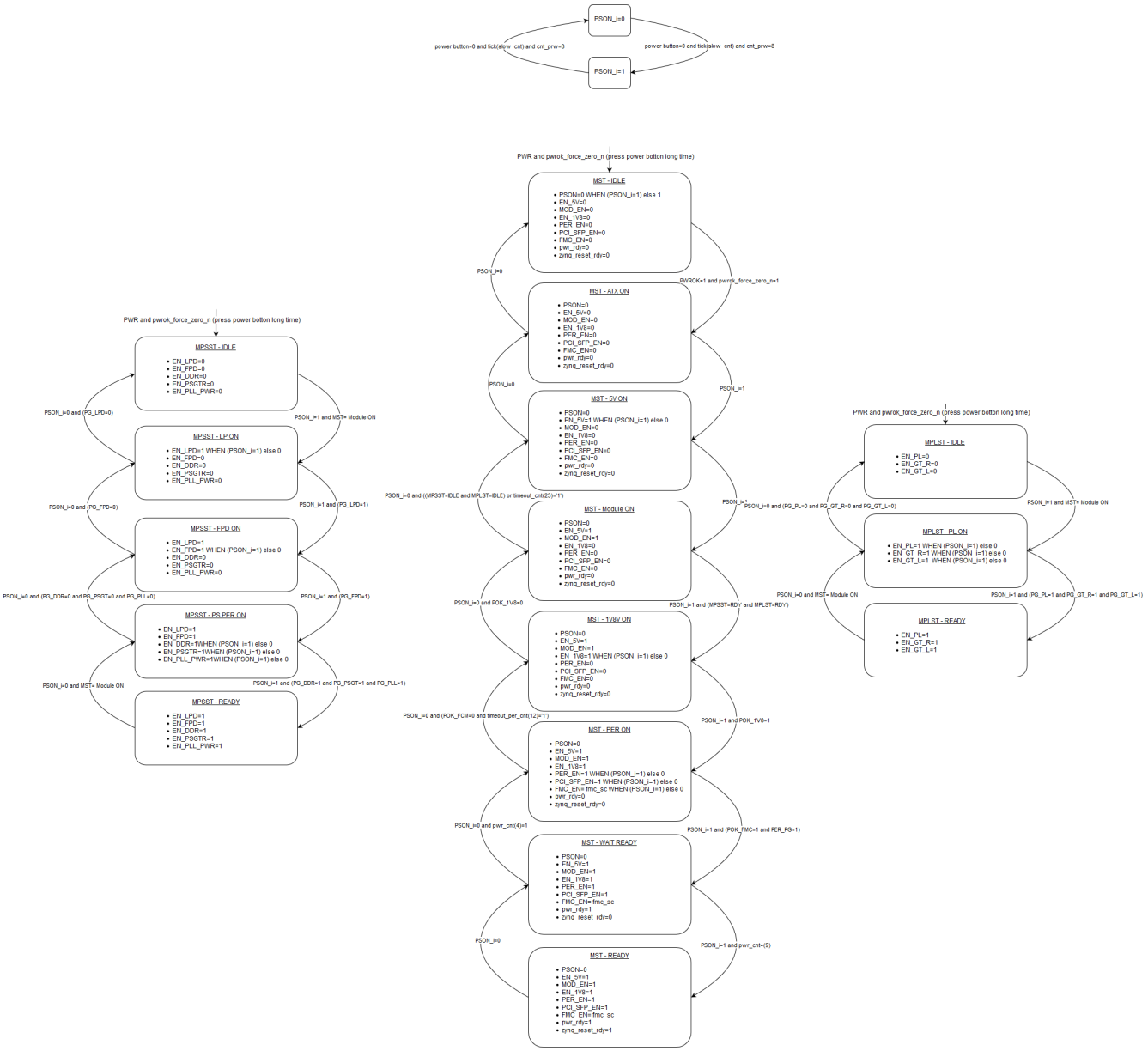
JTAGENB set carrier board CPLD into the chain for firmware update. For Update set DIP S4-3 to ON.

Power

FMC VADJ is handled on master CPLD.

DIP	Positon	Description
S5-4	ON	1.8V
S5-4	OFF	1.2V

Power on and off sequencing is done with slave CPLD.



Power On/OFF Sequencing

Note: Power downs sequencing above can be disabled with second optional CPLD Firmware:

1. Configure Firmware version SCM_07B_powerdown_disabled.jed/SCS_07B_powerdown_disabled.jed
2. Add Jumper to J10-6 and J10-8 instead of Enclousure Button
3. Module will be powered and boot on with Main power supply.

Reset

Power, Zynq reset and PCIe is handle on Slave CPLD

USB, I2C Reset is handled on Master CPLD

Type	controlled by
PCie	Power On Reset_N(pwr_rdy), MIO31
USB(PHY+HUB)	Power On Reset_N(pwr_rdy), MIO30
Modul PLL	Power On Reset_N(pwr_rdy)
PS_POR_B	Reset Button (hold long time ~3s), zynq_reset_ready
PS_SRST_B	Reset Button (hold short time ~1s), zynq_reset_ready
FMC_FAN_EN	Power On Reset_N(pwr_rdy)
I2C_RST	Power On Reset_N(pwr_rdy)
ETH_RST	Power On Reset_N(pwr_rdy)

JTAG

CPLD JTAG only needed for CPLD Firmware update.

FMC and CPLD JTAG is accessable over XMOD2(J28).

S4-3	
ON	CPLD Access on both CPLD
OFF	FMC JTAG Access

PJTAG on connector J17 is routed over Master CPLD to MIO26..29.

Signal	Connection
JTAG_TCK	MIO26
JTAG_RTCK	JTAG_TCK
JTAG_TDI	MIO27
JTAG_TDO	MIO28
JTAG_TMS	MIO29
JTAG_SRST	not usedconnected only to FPGA RGPIO
JTAG_TRST	not used, connected only to FPGA RGPIO

Boot Mode

Boot Mode is handled on Slave CPLD.

S5-1	S5-2	Description
ON	ON	Default, boot from SD/microSD or SPI Flash if no SD is detected
OFF	ON	Boot from eMMC
ON	OFF	Boot mode PJTAG0

OFF	OFF	Boot mode main JTAG

Note: There is a second CPLD Variant available, where microSD will not change the boot mode.

1. Configure Firmware version SCM_07C_msdboot_disabled.jed/SCS_07C_msdboot_disabled.jed
2. Boot mode will be still QSPI,when microSD is insered.

PCIe

PCIe is handled on Slave CPLD.

Signal	Connection
PERSTn	Power On reset and MIO31

SD

SD is mainly handled on Slave CPLD

SD Signal	Description
SD_SEL	CD Pin form microSD selects the SD Card, microSD has higher priority
CD (MIO45)	mircoSD and SD Card detect
WP(MIO44)	0 when miroSD is used else SD card detect (forrward over Master CPLD)

UART SoC

SoC(ZynqMP) is accessible over XMOD1(J12) and connected to ZynqMP over Slave CPLD

Signal	Description
XMOD_TXD	ZynqMP TX(MIO43), when PWR Ready else 1
XMOD_RXD	to ZynqMP RX(MIO42), when PWR Ready else 1

UART (Debug)

Simple Firmware Debug UART is accessible over XMOD2(28) over Master CPLD

Firmware Versions and some statistics can be displayed over second XMOD:

- Included since CPLD Firmware Update to REV07
- UART Speed is 115200
- Press XMOD Button to see output, otherwise RX/TX are loop backed

Signal	Description
XMOD_TXD	Debug output, when XMOD Button is pressed else RX loopback
XMOD_RXD	Debug input(currently no function), when XMOD Button is pressed else TX loopback

CAN

CAN is handled mainly on Master CPLD

Signal	Description
CAN_TX	SC18(FPGA LOC depends on module)
CAN_RX	SC19(FPGA LOC depends on module)
CAN_S	SC16(FPGA LOC depends on module)
CAN_FAULT	Monitoring over RGPIO only

USB

USB Reset is handled mainly on Master CPLD

Signal	Description
USB_RST	Power On Reset and MIO30 (over slave CPLD)
USBH_RST	Power On Reset and MIO30 (over slave CPLD)
USBH_MODE0	const 1
USBH_MODE1	const 1

DisplayPort

DisplayPort is handled on Master CPLD

Signal	Description
DP_EN	not Power On Reset
DP_RX	to SC10 when SC11 is 0 else Z
DP_TX	SX10
DP_DE	SC11
DP_HPD	SC12

SFP

ETH Reset is handled on Master CPLD

Signal	Description
SFP1_TX_DIS	const 0 (Enabled)
SFP2_TX_DIS	const 0 (Enabled)

I2C

I2C MUX is handled on Master CPLD

Signal	Description
I2C_RST	Power On Reset

ETH

ETH Reset is handled on Master CPLD

Signal	Description
ETH_RST	Power On Reset
PHY_CONFIG	const 1

FAN

ETH Reset is handled on Master CPLD

Signal	Description
FAN1	• EN: enabled with power • PWM: const 1
FAN2	• PWM: const 1 • EN: const 1

FMC FAN	• EN enabled with power
	• PWM: via "LM96163CISD/NOPB"
	  ◦ CPLD includes simple I2C master which set fan speed to 0x03 after power on.
	  ◦ User can controll FAN via SoC Modul:
	  ▪ I2C Bus:15 (U27-5 SC_SDA/SDL)
	  ▪ I2C device Address: 0x4C
	  ▪ Example full speed via Starterkit Reference design :i2cset -y -r 15 0x4c 0x4c 0x3F

LEDs

LEDs are handled on both CPLDs.

They used different Blink Sequence to indicate all state:

******** (slow blinking)	~0,7 Hz	continuous blinking, like SFP LEDs or Enclosure HD LED when board is powered down
******** (fast blinking)	~5,8 Hz	continuous blinking, like D6 LED or Enclosure Power LED when board is powered down
*****ooo	~0,7 Hz, duty cycle 5/8	5 times fast blink with a break
****oooo	~0,7 Hz, duty cycle 4/8	4 times fast blink with a break
***ooooo	~0,7 Hz, duty cycle 3/8	3 times fast blink with a break
**oooooo	~0,7 Hz, duty cycle 2/8	2 times fast blink with a break
*ooooooo	~0,7 Hz, duty cycle 1/8	1 times fast blink with a break
ON	---	LED ON
OFF	---	LED OFF

<table>
<tr><th>Designator</th><th>Color</th><th>Usage</th><th>Description</th></tr>
<tr><td>D7</td><td>Red</td><td>status</td><td>
<table>
<tr><th>Priority</th><th>Description</th><th>Blink sequencing</th></tr>
<tr><td>1</td><td>PS POR Reset pressed long time (or whole system is powered off)</td><td>ON</td></tr>
<tr><td>2</td><td>PS Soft Reset pressed short time</td><td>OFF</td></tr>
<tr><td>3</td><td>SD Boot</td><td>*ooooooo</td></tr>
<tr><td>4</td><td>QSPI Boot</td><td>**oooooo</td></tr>
<tr><td>5</td><td>eMMC Boot</td><td>***ooooo</td></tr>
<tr><td>6</td><td>PJTAG Boot</td><td>****oooo</td></tr>
<tr><td>7</td><td>JTAG Boot</td><td>*****ooo</td></tr>
<tr><td>8</td><td>Error</td><td>******** (fast blinking)</td></tr>
</table>
</td></tr>
<tr><td>D6</td><td>Green</td><td>status</td><td>
<table>
<tr><th>Priority</th><th>Description</th><th>Blink sequencing</th></tr>
<tr><td>1</td><td>Power OFF</td><td>******** (fast blinking)</td></tr>
<tr><td>2</td><td>PG_LPD low</td><td>*****ooo</td></tr>
<tr><td>3</td><td>PG_FPD low</td><td>****oooo</td></tr>
<tr><td>4</td><td>PG_PL low</td><td>***ooooo</td></tr>
<tr><td>5</td><td>PG_DDR low or PG_PSGT low or PG_PLL low or PG_GT_L low or PG_GT_R low</td><td>**oooooo</td></tr>
<tr><td>6</td><td>POK_1V8 low or POK_FMC low or perihpery_pg low or (Main Power State Machine Ready and FMC Sanity check low)</td><td>*ooooooo</td></tr>
<tr><td>7</td><td>Main Power State Machine Ready</td><td>OFF</td></tr>
<tr><td>8</td><td>ERROR some power failed, see XMOD LEDs</td><td>ON</td></tr>
</table>
</td></tr>
<tr><td>J10 Power LED</td><td>Blue (symbol light bulb)</td><td>status /user</td><td>
<table>
<tr><th>Priority</th><th>Description</th><th>Blink sequencing</th></tr>
<tr><td>1</td><td>power button pressed long time forced power down</td><td>******** (fast blinking)</td></tr>
<tr><td>2</td><td>Main Power State Machine Idle and Power of State is off</td><td>******** (slow blinking)</td></tr>
<tr><td>3</td><td>power button pressed short time power to power on/off</td><td>*****ooo</td></tr>
<tr><td>4</td><td>PS reset button pressed long time</td><td>****oooo</td></tr>
<tr><td>5</td><td>PS reset button pressed short time</td><td>***ooooo</td></tr>
<tr><td>6</td><td>power down sequencing is running</td><td>**oooooo</td></tr>
<tr><td>7</td><td>whole system hold into reset</td><td>*ooooooo</td></tr>
<tr><td>8</td><td>MIO40</td><td>User Defined</td></tr>
</table>
</td></tr>
</table>

<table>
<tr>
<td>J10 HD LED</td>
<td>Red (symbol drive)</td>
<td>status /user</td>
<td>
<table>
<tr><th>Priority</th><th>Description</th><th>Blink sequencing</th></tr>
<tr><td>1</td><td>PS Init is low</td><td>******** (fast blinking)</td></tr>
<tr><td>2</td><td>PS Error High</td><td>*****ooo</td></tr>
<tr><td>3</td><td>PS Error Status High</td><td>****oooo</td></tr>
<tr><td>4</td><td>SOC Done low</td><td>***ooooo</td></tr>
<tr><td>5</td><td>SC0</td><td>User Defined</td></tr>
</table>
</td>
</tr>
<tr>
<td>XMOD1 D4</td>
<td>Red</td>
<td>status</td>
<td>
<table>
<tr><th>Priority</th><th>XMOD Button</th><th>Description</th><th>Blink sequencing</th></tr>
<tr><td>1</td><td>Pressed</td><td>power button pressed long time forced power down</td><td>******** (fast blinking)</td></tr>
<tr><td>2</td><td>Pressed</td><td>Main Power State Machine Idle and Power of State is power down
sequencing</td><td>*****ooo</td></tr>
<tr><td>3</td><td>Pressed</td><td>PS reset button pressed</td><td>****oooo</td></tr>
<tr><td>4</td><td>Pressed</td><td>Power button pressed short time power on/off</td><td>***ooooo</td></tr>
<tr><td>5</td><td>Pressed</td><td>Power of State is power down sequencing</td><td>**oooooo</td></tr>
<tr><td>6</td><td>Pressed</td><td>System hold into reset</td><td>*ooooooo</td></tr>
<tr><td>7</td><td>Pressed</td><td>PS Init low</td><td>ON</td></tr>
<tr><td>1</td><td>Unpressed</td><td>Problem with other CPLD, FMC is disabled</td><td>******** (fast blinking)</td></tr>
<tr><td>2</td><td>Unpressed</td><td>Main Power State Machine Wait Ready ON/OFF</td><td>*****ooo</td></tr>
<tr><td>3</td><td>Unpressed</td><td>Main Power State Machine 3.3V and VADJ ON/OFF</td><td>****oooo</td></tr>
<tr><td>4</td><td>Unpressed</td><td>power not ready (power reset)</td><td>**oooooo</td></tr>
<tr><td>5</td><td>Unpressed</td><td>zynq reset</td><td>*ooooooo</td></tr>
<tr><td>7</td><td>Unpressed</td><td>PS Init low</td><td>ON</td></tr>
<tr><td>x</td><td>Pressed /Unpressed</td><td>all fine</td><td>OFF</td></tr>
</table>
</td>
</tr>
<tr>
<td>XMOD2 D4</td>
<td>Red</td>
<td>status /user</td>
<td>
<table>
<tr><th>Priority</th><th>Description</th><th>Blink sequencing</th></tr>
<tr><td>1</td><td>Power On Reset</td><td>******** (slow blinking)</td></tr>
<tr><td>2</td><td>PS Init low</td><td>******** (fast blinking)</td></tr>
<tr><td>3</td><td>SC17</td><td>User Defined</td></tr>
</table>
</td>
</tr>
<tr>
<td>SFP D1</td>
<td>Red</td>
<td>status /user</td>
<td>
<table>
<tr><th>Priority</th><th>Description</th><th>Blink sequencing</th></tr>
<tr><td>1</td><td>Power On Reset</td><td>******** (slow blinking)</td></tr>
<tr><td>2</td><td>PS Init low</td><td>******** (fast blinking)</td></tr>
<tr><td>3</td><td>RGPIO(0), when RGPIO Enabled over FPGA</td><td>User Defined</td></tr>
<tr><td>4</td><td>--</td><td>OFF</td></tr>
</table>
</td>
</tr>
<tr>
<td>SFP D8</td>
<td>Green</td>
<td>status /user</td>
<td>
<table>
<tr><th>Priority</th><th>Description</th><th>Blink sequencing</th></tr>
<tr><td>1</td><td>Power On Reset</td><td>******** (slow blinking)</td></tr>
<tr><td>2</td><td>PS Init low</td><td>******** (fast blinking)</td></tr>
<tr><td>3</td><td>RGPIO(1), when RGPIO Enabled over FPGA</td><td>User Defined</td></tr>
<tr><td>4</td><td>--</td><td>OFF</td></tr>
</table>
</td>
</tr>
</table>

<table>
<tr><td>D17 - USB HUB LED (Suspend)</td><td>Green</td><td>status</td><td>ON, no USB connected, OFF, USB connected</td></tr>
<tr><td>SFP D9</td><td>Red</td><td>status /user</td><td>
<table>
<tr><th>Priority</th><th>Description</th><th>Blink sequencing</th></tr>
<tr><td>1</td><td>Power On Reset</td><td>******** (slow blinking)</td></tr>
<tr><td>2</td><td>PS Init low</td><td>******** (fast blinking)</td></tr>
<tr><td>3</td><td>RGPIO(2), when RGPIO Enabled over FPGA</td><td>User Defined</td></tr>
<tr><td>4</td><td>--</td><td>OFF</td></tr>
</table>
</td></tr>
<tr><td>SFP D10</td><td>Green</td><td>status /user</td><td>
<table>
<tr><th>Priority</th><th>Description</th><th>Blink sequencing</th></tr>
<tr><td>1</td><td>Power On Reset</td><td>******** (slow blinking)</td></tr>
<tr><td>2</td><td>PS Init low</td><td>******** (fast blinking)</td></tr>
<tr><td>3</td><td>RGPIO(3), when RGPIO Enabled over FPGA</td><td>User Defined</td></tr>
<tr><td>4</td><td>--</td><td>OFF</td></tr>
</table>
</td></tr>
<tr><td>ETH J7</td><td>Yellow</td><td>status</td><td>
<table>
<tr><th>Priority</th><th>Description</th><th>Blink sequencing</th></tr>
<tr><td>1</td><td>Power On Reset</td><td>******** (slow blinking)</td></tr>
<tr><td>2</td><td>PS Init low</td><td>******** (fast blinking)</td></tr>
<tr><td>3</td><td>ETH PHY LED</td><td>(not PHY_LED0)</td></tr>
</table>
</td></tr>
<tr><td>ETH J7</td><td>Green/Orange</td><td>status</td><td>
<table>
<tr><th>Priority</th><th>Description</th><th>Blink sequencing</th></tr>
<tr><td>1</td><td>Power On Reset</td><td>******** (slow blinking)</td></tr>
<tr><td>2</td><td>PS Init low</td><td>******** (fast blinking)</td></tr>
<tr><td>3</td><td>ETH PHY LED</td><td>(PHY_LED1)</td></tr>
</table>
</td></tr>
<tr><td>D4</td><td>Green</td><td>status /user</td><td>
<table>
<tr><th>Priority</th><th>Description</th><th>Blink sequencing</th></tr>
<tr><td>1</td><td>1.8V disabled, inter CPLD RGPIO is disabled</td><td>******** (fast blinking)</td></tr>
<tr><td>2</td><td>1.8V enabled, inter CPLD RGPIO is disabled</td><td>*****ooo</td></tr>
<tr><td>3</td><td>Power On Reset</td><td>****oooo</td></tr>
<tr><td>4</td><td>USB Reset</td><td>***ooooo</td></tr>
<tr><td>5</td><td>RGPIO(4), when RGPIO Enabled over FPGA</td><td>User Defined</td></tr>
<tr><td>6</td><td>all fine</td><td>*ooooooo</td></tr>
</table>
</td></tr>
<tr><td>D5</td><td>Red</td><td>status /user</td><td>
<table>
<tr><th>Priority</th><th>Description</th><th>Blink sequencing</th></tr>
<tr><td>1</td><td>1.8V disabled, inter CPLD RGPIO is disabled</td><td>******** (fast blinking)</td></tr>
<tr><td>2</td><td>1.8V enabled, inter CPLD RGPIO is disabled</td><td>*****ooo</td></tr>
<tr><td>3</td><td>Power On Reset</td><td>****oooo</td></tr>
<tr><td>4</td><td>PCie Reset</td><td>***ooooo</td></tr>
<tr><td>5</td><td>RGPIO(4), when RGPIO Enabled over FPGA</td><td>User Defined</td></tr>
<tr><td>6</td><td>all fine</td><td>*ooooooo</td></tr>
</table>
</td></tr>
</table>

RGPIO

There are 3 RGPIO interfaces, one InterCPLD RGPIO, and one from every CPLD to SoC.

InterCPLD RGPIO handles:

Signal	Description
Reset Button (SW)	for monitoring only
PS POR	for monitoring only
PS ERR Stat	for monitoring only
PS ERR	for monitoring only
PS Init	for monitoring only
PCIe Reset	for monitoring only
USB Reset	for USB Reset and monitoring
Power On Reset	for Power On Reset and monitoring
inter FPGA	Data from Slave RGPIO to Master RGPIO (for test only)

Master CPLD-SoC RGPIO (accesseble via SoC):

Signal	Description
FPGA Read (23)	JTAG_SRST
FPGA Read (22)	JTAG_TRST
FPGA Read (21)	FMC_CLKDIR
FPGA Read (20)	SD_WP
FPGA Read (19)	unused 0
FPGA Read (18)	SW4
FPGA Read (17)	SW3
FPGA Read (16)	XMOD_G
FPGA Read (15 dt 13)	PHY LEDs
FPGA Read (12)	CAN_FAULT
FPGA Read (11 dt 8)	current RGPIO Mux

FPGA Read (7 dt 0)	Data depends on MUX: 0 Data(7dt0) from Slave CPLD-SoC RGPIO 1 POR Statistic 2 PS RST Statistic 3 PS POR Statistic 4 PS Init Statistic 5 PS ERR Statistic 6 PS ERR Stat Statistic 7 PCie RST Statistic 8 USB RST Statistic
FPGA Write (23 dt 12)	unused
FPGA Write (11 dt 8)	RGPIO Mux, see FPGA Read (7 dt 0) , when RGIO active
FPGA Write (7 dt 6)	unused
FPGA Write (5 dt 0)	Diverse LED controll(see LED description) , when RGIO active

Slave CPLD-SoC RGPIO (accesseble via SoC):

Signal	Description
FPGA Read (23)	PLL_LOL
FPGA Read (22)	PG_PLL
FPGA Read (21)	PG_PL
FPGA Read (20)	PWROK and pwrok_force_zero_n
FPGA Read (19)	fmc_sanity_check
FPGA Read (18)	POK_FMC
FPGA Read (17)	PG_GT_R
FPGA Read (16)	PG_GT_L
FPGA Read (15)	PG_PSGT
FPGA Read (14)	PG_FPD
FPGA Read (13)	PG_DDR
FPGA Read (12)	PG_LPD
FPGA Read (11 dt 8)	current Boot Mode
FPGA Read (7)	ERR_STAT
FPGA Read (6)	ERROR
FPGA Read (5)	SD_CD_B
FPGA Read (4)	SD_CD_S
FPGA Read (3)	unused const 1

FPGA Read (2)	XMOD_BTN
FPGA Read (1)	SW2
FPGA Read (0)	SW1
FPGA Write (23 dt 8)	unused
FPGA Write (7dt 0)	Readable over Master CPLD-SoC RGPIO, when RGIO active

Appx. A: Change History and Legal Notices

Revision Changes

Master	Slave
CPLD REV02 to REV01 • add enable FAN2(F2*) with const 1 PWM • add I2C Master and FMC FAN activation(only slow speed, customer can control via FPGA and I2C)	CPLD REV02 to REV01 • DISABLE_ATX_PWROK default 0
CPLD REV01 to TEBF0808 version(Copy from TEBF0808 SCB0808 REV07(dev)) • disable DP-HPD pullup • changed CPLD string name • counter deep for status register (otherwhise new version of lattice mapping tool has problems)	CPLD REV01 to TEBF0808 version(Copy from TEBF0808 SCB0808 REV07(dev)) • Add Parameter to disable PWOK usage(for 12V only usage, CPLD can't detect which power supply is used on PCB REV01 and POWK will be forced to low, in case ATX is not connected) • PSON inverted

Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

Date	Document Revision	CPLD Firmware Revision	Supported PCB Revision	Authors	Description
		REV02	REV02	**Error rendering macro 'page-info'** Ambiguous method overloading for method	• Update new content • REV02 finished (Firmware released on 2023-06-14, SC-PGM-TEBF0818-02_SCBF0818-02_20230614.zip)

Error rendering macro 'page-info' Ambiguous method overloading for method jdk.proxy244.$Proxy3572#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy244.$Proxy3572#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]			jdk.proxy244.$Proxy3572#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	

				[interface com. atlassian. user.User, class java. lang. String, class com. atlassian. confluence. core. ContentEnt ityObject]	
2021-09-21	v.2	REV01	REV01*		• Initial release (copy from TEBF0808 CPLD Firmware REV07) • REV01 finished (Firmware released on 2021-09-21) • *special Firmware for TEBF0818-01 only
	All			**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk. proxy244.$ Proxy3572	

#hasConte
ntLevelPer
mission.
Cannot
resolve
which
method to
invoke for
[null, class
java.lang.
String,
class com.
atlassian.
confluence.
pages.
Page] due
to
overlapping
prototypes
between:
[interface
com.
atlassian.
confluence.
user.
Confluence
User,
class java.
lang.
String,
class com.
atlassian.
confluence.
core.
ContentEnt
ityObject]
[interface
com.
atlassian.

				user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	

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Error rendering macro 'page-info'

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