TEBF0818 Getting Started

TEBF0818 with TE081x

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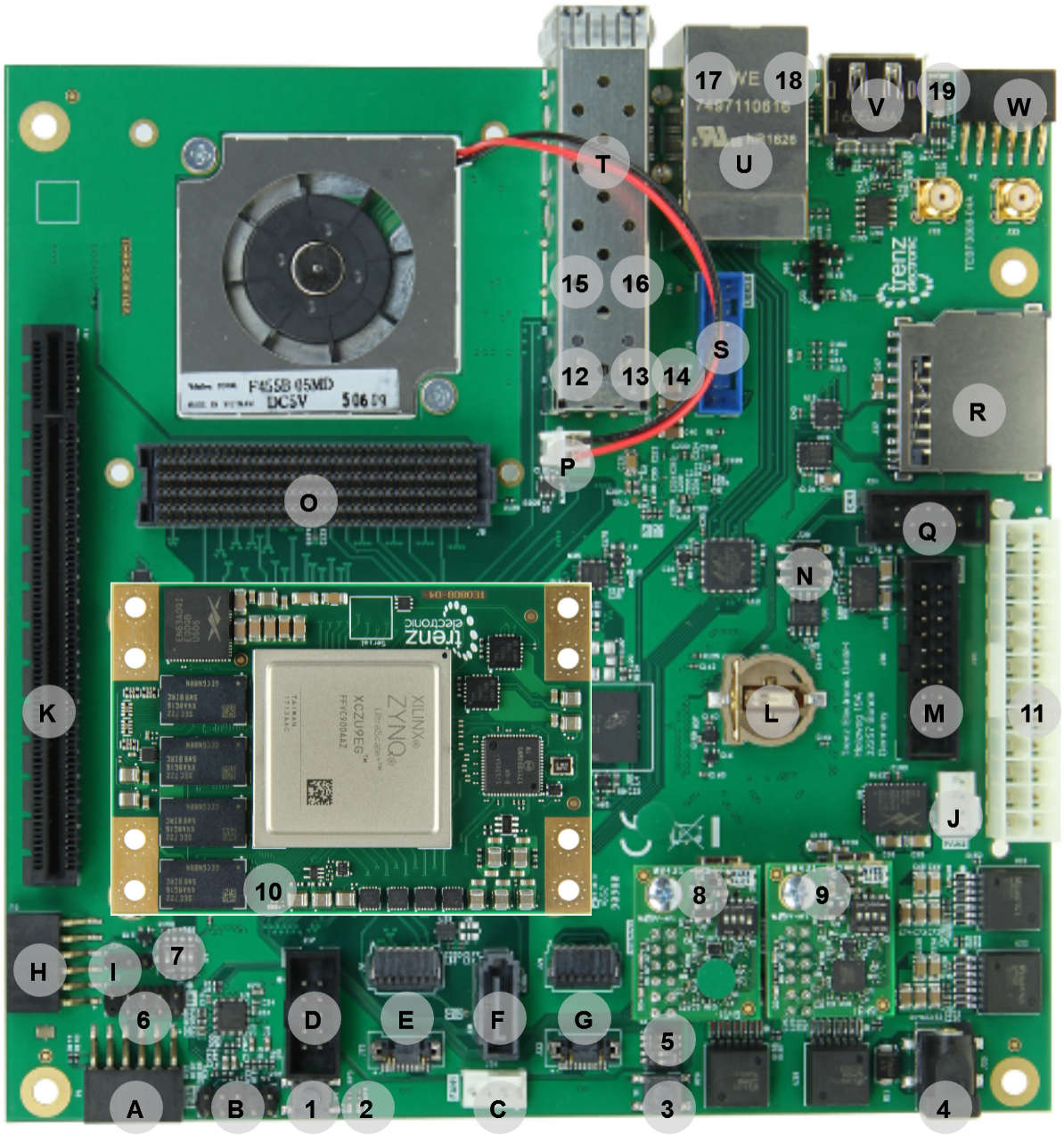
Overview

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Basic instructions to work with TEBF0818 and TE0818,TE0817 or TE0813.

> Functionality of buttons, DIP switches, LEDs depends on CPLD Firmware. Following description is only for newest firmware version, which is available on the download area

TEBF0818 with TE0818



Board Overview

Number	Note		Letter	Note

1	S2- Reset Button		A	P1 - PMOD 3.3V I2C Bus
2	D7 - LED D7 Red (Usage: status) || D6 - LED Green (Usage: status)		B	J9 - Audio Enclosure
3	S1 - Power Button		C	J26 - FAN1 12V
4	J25 - Power Jack J25, 2.1mm (optional 12V power input)		D	J17 - I2C (for optional module PLL access)
5	S5 - DIP Switch for Boot Mode and FMCVADJ		E	J6/15 - Firefly - GTH
6	J10 - Enclosure Pin header(Reset and Power Button, HD LED (Usage: status/user) and Power LED (Usage: status/user))		F	J31 - SATA
7	S4 - DIP Switch for CPLD access and power control		G	J21/22 - Firefly - loopback only
8	J12 - XMOD with green dot for Module JTAG and UART, XMOD LED D4 Red used for status information		H	P3 - PMOD 3.3V I2C Bus
9	J28 - XMOD for CPLD,FMC JTAG and Firmware ID over UART (need CPLD Firmware 7 or newer) , XMOD LED D4 Red used for status information		I	J34 - I2C Firefly
10	FPGA Done LED (location varies slightly on different module series)		J	J35 - FAN2 12V
11	J20 - ATX Power Connector (Main 12V and 5V Power supply), recommended power supply connector		K	J11 - PCIe (1x)
12	D1 - SFP LED Red (Usage: status/user)		L	B1 - Battery holder CR1220
13	D8 - SFP LED Green (Usage: status/user)		M	J30 - PJTAG
14	D17 - USB HUB LED Green (Suspend)		N	J29 - CAN (same as J24)
15	D9 - SFP LED Red (Usage: status/user)		O	J5 - FMC HPC
16	D10 - SFP LED Green (Usage: status/user)		P	J19 - FAN3 5V
17	J7 - ETH LED Yellow (Usage: status)		Q	J24 - CAN (same as J29)
18	J7 - ETH LED Green/Orange (Usage: status)		R	J27 - SD

19	D4 - LED Green (Usage: status/user) || D5 - LED Red (Usage: status /user)		S	J8 - USB 3.0 (2x) Enclosure
---	---		T	J14 - SFP (2x)
---	---		U	J7 - USB 3.0 (2x), ETH (1x)
---	---		V	J13 - Displayp ort (1x)
---	---		W	P2 - PMOD 3.3V FPG IOs
---	---		W(b)	Bottom side: J16 - microSD

Power supply

Label	Designator	Power	Description
Overview - 11	J20	12V and 5V	**Recommended** power supply unit is PC power supply unit: • DIP S4-4 can be switched OFF with this power supply configuration (CPLD firmware depended)
Overview - 4	J25	12V	Optional single 12V power supply: • DIP S4-4 must be switched ON with this power supply

Current depends manly on design and cooling solution. Use Xilinx Power Estimator and/or Your Vivado Project to estimate min current. Minimum of 3A are recommanded for basic functionality.

DIP-Switches and Push Buttons

Overview 7	Default	Description
S4-1	OFF	SoC PUDC, ON (low - internal FPGA pull ups enabled), OFF (high - internal FPGA pull ups disabled)
S4-2	OFF	N.C.
S4-3	OFF	JTAGEN ON (CPLD access), OFF (FMC access)
S4-4	ON	Enable on board 5V permanently

DIP Switches S4

Overview 5	Default	Description
S5-1	ON	

S5-2	ON	• ON(1), ON(2) - Default, boot from SD/microSD or SPI Flash if no SD is detected • OFF(1), ON(2) - Boot from eMMC • ON(1), OFF(2) - Boot mode PJTAG0 • OFF(1), OFF(2) - Boot mode main JTAG
S5-3	OFF	User Input to SoC over RGPIO interface
S5-4	OFF	VADJ OFF(1.2V), ON(1.8V)

DIP Switches S5 (CPLD Firmware depended)

Overview 1;3	Default	Description
S2	High	Negative Reset Button, alternative Enclosure over J10-7/J10-5 • Press appr. 1sec for PS Soft Reset (PS_SRST_B)* • Press appr 3 sec for PS POR Reset
S1	High	Negative Power Button, alternative Enclosure over J10-6/J10-8 • Press appr. 1sec for power on/off • Press appr 3 sec force power of without power down sequencing

*Note: PS_SRST_B ignores mode pins and do not reset all registers, see UG1085 table 38-1

Buttons (CPLD Firmware depended)

LEDs

LEDs used different Blink Sequence to indicate all state:

Blink Sequence	Frequence	Note
******** (slow blinking)	~0,7 Hz	continuous blinking, like SFP LEDs or Enclosure HD LED when board is powered down
******** (fast blinking)	~5,8 Hz	continuous blinking, like D6 LED or Enclosure Power LED when board is powered down
*****ooo	~0,7 Hz, duty cycle 5/8	5 times fast blink with a break
****oooo	~0,7 Hz, duty cycle 4/8	4 times fast blink with a break
***ooooo	~0,7 Hz, duty cycle 3/8	3 times fast blink with a break
**oooooo	~0,7 Hz, duty cycle 2/8	2 times fast blink with a break
*ooooooo	~0,7 Hz, duty cycle 1/8	1 times fast blink with a break
ON	---	LED ON
OFF	---	LED OFF

LED Sequencing (CPLD Firmware depended)

<table>
<tr><th>Label</th><th>Designator</th><th>Color</th><th>Usage</th><th>Description</th></tr>
<tr><td>Overview - 2</td><td>D7</td><td>Red</td><td>status</td><td>
<table>
<tr><th>Priority</th><th>Description</th><th>Blink sequencing</th></tr>
<tr><td>1</td><td>PS POR Reset pressed long time (or whole system is powered off)</td><td>ON</td></tr>
<tr><td>2</td><td>PS Soft Reset pressed short time</td><td>OFF</td></tr>
<tr><td>3</td><td>SD Boot</td><td>*ooooooo</td></tr>
<tr><td>4</td><td>QSPI Boot</td><td>**oooooo</td></tr>
<tr><td>5</td><td>eMMC Boot</td><td>***ooooo</td></tr>
<tr><td>6</td><td>PJTAG Boot</td><td>****oooo</td></tr>
<tr><td>7</td><td>JTAG Boot</td><td>*****ooo</td></tr>
<tr><td>8</td><td>Error</td><td>******** (fast blinking)</td></tr>
</table>
</td></tr>
<tr><td>Overview - 2</td><td>D6</td><td>Green</td><td>status</td><td>
<table>
<tr><th>Priority</th><th>Description</th><th>Blink sequencing</th></tr>
<tr><td>1</td><td>Power OFF</td><td>******** (fast blinking)</td></tr>
<tr><td>2</td><td>PG_LPD low</td><td>*****ooo</td></tr>
<tr><td>3</td><td>PG_FPD low</td><td>****oooo</td></tr>
<tr><td>4</td><td>PG_PL low</td><td>***ooooo</td></tr>
<tr><td>5</td><td>PG_DDR low or PG_PSGT low or PG_PLL low or PG_GT_L low or PG_GT_R low</td><td>**oooooo</td></tr>
<tr><td>6</td><td>POK_1V8 low or POK_FMC low or perihpery_pg low or (Main Power State Machine Ready and FMC Sanity check low)</td><td>*ooooooo</td></tr>
<tr><td>7</td><td>Main Power State Machine Ready</td><td>OFF</td></tr>
<tr><td>8</td><td>ERROR some power failed, see XMOD LEDs</td><td>ON</td></tr>
</table>
</td></tr>
<tr><td>Overview - 6</td><td>J10 Power LED</td><td>Blue (symbol light bulb)</td><td>status /user</td><td>
<table>
<tr><th>Priority</th><th>Description</th><th>Blink sequencing</th></tr>
<tr><td>1</td><td>power button pressed long time forced power down</td><td>******** (fast blinking)</td></tr>
<tr><td>2</td><td>Main Power State Machine Idle and Power of State is off</td><td>******** (slow blinking)</td></tr>
<tr><td>3</td><td>power button pressed short time power to power on/off</td><td>*****ooo</td></tr>
<tr><td>4</td><td>PS reset button pressed long time</td><td>****oooo</td></tr>
<tr><td>5</td><td>PS reset button pressed short time</td><td>***ooooo</td></tr>
<tr><td>6</td><td>power down sequencing is running</td><td>**oooooo</td></tr>
<tr><td>7</td><td>whole system hold into reset</td><td>*ooooooo</td></tr>
<tr><td>8</td><td>MIO40</td><td>User Defined</td></tr>
</table>
</td></tr>
</table>

<table>
<tr>
<td>Overview - 6</td>
<td>J10 HD LED</td>
<td>Red (symbol drive)</td>
<td>status /user</td>
<td>
<table>
<tr><th>Priority</th><th>Description</th><th>Blink sequencing</th></tr>
<tr><td>1</td><td>PS Init is low</td><td>******** (fast blinking)</td></tr>
<tr><td>2</td><td>PS Error High</td><td>*****ooo</td></tr>
<tr><td>3</td><td>PS Error Status High</td><td>****oooo</td></tr>
<tr><td>4</td><td>SOC Done low</td><td>***ooooo</td></tr>
<tr><td>5</td><td>SC0</td><td>User Defined</td></tr>
</table>
</td>
</tr>
<tr>
<td>Overview - 8</td>
<td>XMOD1 D4</td>
<td>Red</td>
<td>status</td>
<td>
<table>
<tr><th>Priority</th><th>XMOD Button</th><th>Description</th><th>Blink sequencing</th></tr>
<tr><td>1</td><td>Pressed</td><td>power button pressed long time forced power down</td><td>******** (fast blinking)</td></tr>
<tr><td>2</td><td>Pressed</td><td>Main Power State Machine Idle and Power of State is power down sequencing</td><td>*****ooo</td></tr>
<tr><td>3</td><td>Pressed</td><td>PS reset button pressed</td><td>****oooo</td></tr>
<tr><td>4</td><td>Pressed</td><td>Power button pressed short time power on/off</td><td>***ooooo</td></tr>
<tr><td>5</td><td>Pressed</td><td>Power of State is power down sequencing</td><td>**oooooo</td></tr>
<tr><td>6</td><td>Pressed</td><td>System hold into reset</td><td>*ooooooo</td></tr>
<tr><td>7</td><td>Pressed</td><td>PS Init low</td><td>ON</td></tr>
<tr><td>1</td><td>Unpressed</td><td>Problem with other CPLD, FMC is disabled</td><td>******** (fast blinking)</td></tr>
<tr><td>2</td><td>Unpressed</td><td>Main Power State Machine Wait Ready ON/OFF</td><td>*****ooo</td></tr>
<tr><td>3</td><td>Unpressed</td><td>Main Power State Machine 3.3V and VADJ ON/OFF</td><td>****oooo</td></tr>
<tr><td>4</td><td>Unpressed</td><td>power not ready (power reset)</td><td>**oooooo</td></tr>
<tr><td>5</td><td>Unpressed</td><td>zynq reset</td><td>*ooooooo</td></tr>
<tr><td>7</td><td>Unpressed</td><td>PS Init low</td><td>ON</td></tr>
<tr><td>x</td><td>Pressed /Unpressed</td><td>all fine</td><td>OFF</td></tr>
</table>
</td>
</tr>
<tr>
<td>Overview - 9</td>
<td>XMOD2 D4</td>
<td>Red</td>
<td>status /user</td>
<td>
<table>
<tr><th>Priority</th><th>Description</th><th>Blink sequencing</th></tr>
<tr><td>1</td><td>Power On Reset</td><td>******** (slow blinking)</td></tr>
<tr><td>2</td><td>PS Init low</td><td>******** (fast blinking)</td></tr>
<tr><td>3</td><td>SC17</td><td>User Defined</td></tr>
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</td>
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<td>Overview - 12</td>
<td>SFP D1</td>
<td>Red</td>
<td>status /user</td>
<td>
<table>
<tr><th>Priority</th><th>Description</th><th>Blink sequencing</th></tr>
<tr><td>1</td><td>Power On Reset</td><td>******** (slow blinking)</td></tr>
<tr><td>2</td><td>PS Init low</td><td>******** (fast blinking)</td></tr>
<tr><td>3</td><td>RGPIO(0), when RGPIO Enabled over FPGA</td><td>User Defined</td></tr>
<tr><td>4</td><td>--</td><td>OFF</td></tr>
</table>
</td>
</tr>
</table>

<table>
<tr><td>Overview - 13</td><td>SFP D8</td><td>Green</td><td>status /user</td><td><table><tr><th>Priority</th><th>Description</th><th>Blink sequencing</th></tr><tr><td>1</td><td>Power On Reset</td><td>******** (slow blinking)</td></tr><tr><td>2</td><td>PS Init low</td><td>******** (fast blinking)</td></tr><tr><td>3</td><td>RGPIO(1), when RGPIO Enabled over FPGA</td><td>User Defined</td></tr><tr><td>4</td><td>--</td><td>OFF</td></tr></table></td></tr>
<tr><td>Overview - 14</td><td>D17 - USB HUB LED (Suspend)</td><td>Green</td><td>status</td><td>ON, no USB connected, OFF, USB connected</td></tr>
<tr><td>Overview - 15</td><td>SFP D9</td><td>Red</td><td>status /user</td><td><table><tr><th>Priority</th><th>Description</th><th>Blink sequencing</th></tr><tr><td>1</td><td>Power On Reset</td><td>******** (slow blinking)</td></tr><tr><td>2</td><td>PS Init low</td><td>******** (fast blinking)</td></tr><tr><td>3</td><td>RGPIO(2), when RGPIO Enabled over FPGA</td><td>User Defined</td></tr><tr><td>4</td><td>--</td><td>OFF</td></tr></table></td></tr>
<tr><td>Overview - 16</td><td>SFP D10</td><td>Green</td><td>status /user</td><td><table><tr><th>Priority</th><th>Description</th><th>Blink sequencing</th></tr><tr><td>1</td><td>Power On Reset</td><td>******** (slow blinking)</td></tr><tr><td>2</td><td>PS Init low</td><td>******** (fast blinking)</td></tr><tr><td>3</td><td>RGPIO(3), when RGPIO Enabled over FPGA</td><td>User Defined</td></tr><tr><td>4</td><td>--</td><td>OFF</td></tr></table></td></tr>
<tr><td>Overview - 17</td><td>ETH J7</td><td>Yellow</td><td>status</td><td><table><tr><th>Priority</th><th>Description</th><th>Blink sequencing</th></tr><tr><td>1</td><td>Power On Reset</td><td>******** (slow blinking)</td></tr><tr><td>2</td><td>PS Init low</td><td>******** (fast blinking)</td></tr><tr><td>3</td><td>ETH PHY LED</td><td>(not PHY_LED0)</td></tr></table></td></tr>
<tr><td>Overview - 18</td><td>ETH J7</td><td>Green /Orange</td><td>status</td><td><table><tr><th>Priority</th><th>Description</th><th>Blink sequencing</th></tr><tr><td>1</td><td>Power On Reset</td><td>******** (slow blinking)</td></tr><tr><td>2</td><td>PS Init low</td><td>******** (fast blinking)</td></tr><tr><td>3</td><td>ETH PHY LED</td><td>(PHY_LED1)</td></tr></table></td></tr>
</table>

<table>
<tr>
<td>Overview - 19</td>
<td>D4</td>
<td>Green</td>
<td>status /user</td>
<td>
<table>
<tr><th>Priority</th><th>Description</th><th>Blink sequencing</th></tr>
<tr><td>1</td><td>1.8V disabled, inter CPLD RGPIO is disabled</td><td>******** (fast blinking)</td></tr>
<tr><td>2</td><td>1.8V enabled, inter CPLD RGPIO is disabled</td><td>*****ooo</td></tr>
<tr><td>3</td><td>Power On Reset</td><td>****oooo</td></tr>
<tr><td>4</td><td>USB Reset</td><td>***ooooo</td></tr>
<tr><td>5</td><td>RGPIO(4), when RGPIO Enabled over FPGA</td><td>User Defined</td></tr>
<tr><td>6</td><td>all fine</td><td>*ooooooo</td></tr>
</table>
</td>
</tr>
<tr>
<td>Overview - 19</td>
<td>D5</td>
<td>Red</td>
<td>status /user</td>
<td>
<table>
<tr><th>Priority</th><th>Description</th><th>Blink sequencing</th></tr>
<tr><td>1</td><td>1.8V disabled, inter CPLD RGPIO is disabled</td><td>******** (fast blinking)</td></tr>
<tr><td>2</td><td>1.8V enabled, inter CPLD RGPIO is disabled</td><td>*****ooo</td></tr>
<tr><td>3</td><td>Power On Reset</td><td>****oooo</td></tr>
<tr><td>4</td><td>PCie Reset</td><td>***ooooo</td></tr>
<tr><td>5</td><td>RGPIO(4), when RGPIO Enabled over FPGA</td><td>User Defined</td></tr>
<tr><td>6</td><td>all fine</td><td>*ooooooo</td></tr>
</table>
</td>
</tr>
</table>

Carrier LEDs (CPLD Firmware depended)

Label	Designator	Color	Connected to	Description
Overview - 10	D1	Red	DONE signal (PS Configuration Bank 503)	This LED goes ON when power has been applied to the module and stays ON until MPSoC's programmable logic is configured properly.

Module LEDs

JTAG/UART

There are 2 JTAG programmer on the carrier:

Label	Designator	Description
Overview - 8	J12	• SoC JTAG/UART over USB, UART Speed depends on design, normally 115200 • XMOD with Xilinx Licence (green dot)
Overview - 9	J28	• CPLD or FMC JTAG over USB • XMOD without Xilinx Licence • Press Button to see Firmware ID over UART (need CPLD Firmware 7 or newer), UART Speed 115200

DIP Switch on bouth XMOD JTAG adapters must be set like on the following table.

XMOD DIP Switch	Setting
1	ON
2	OFF
3	OFF
4	OFF

XMOD JTAG DIP Switch. Attention: Never changes the default setting

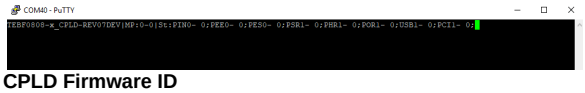
For more information refer to TE0790 Resources.

CPLD Firmware

Firmware Update Instruction and CPLD description are available on TEBF0818 CPLD Firmware Source code of the firmware is available on the download area of the TEBF0818.

Firmware Versions and some statistics can be displayed over second XMOD:

- Included since CPLD Firmware Update to REV07
- UART Speed is 115200
- Press XMOD Button to see output, otherwise RX/TX are loop backed



CPLD Firmware ID

Type	Description
SCB818-REV01	CPLD Firmware Version

MP	• Main Power State, Note: Only correct, if 1.8V is powered on
	• First Number indicates 1.8V Power state(1-ON)
	• Second Number indicates Main State Machine:
	  ◦ 0:IDLE (Power OFF)
	  ◦ 1:ATX ON/OFF
	  ◦ 2:V5 ON/OFF
	  ◦ 3:Module Power ON/OFF (Different domains over LED visible)
	  ◦ 4:1.8V ON/OFF
	  ◦ 5:Periphery ON/OFF
	  ◦ 6: Wait Ready (Power Ok, SoC on Reset)
	  ◦ 7. Ready (Power/SoC OK)

PIN	• PS Init, when Power Reset released • First Number current PS-INIT (Inverted) • Second Number PSINIT counter
PEE	• PS ERROR, when Power Reset released • First Number current PS-ERROR • Second Number ERROR counter

PES	• PS ERROR Status, when Power Reset released • First Number current PS-ERROR Status • Second Number ERROR Status counter
PSR	• PS Soft Reset(also high, PS Power On Rese is active) • First Number current PS-Soft Reset • Second Number PS-Soft Reset counter
PHR	• PS Power On Reset • First Number current PS- Power On Reset • Second Number PS- Power On Reset counter
POR	• Main Power On Reset • First Number current Main- Power On Reset • Second Number Main Power On Reset counter
USB	• USB Reset • First Number current USB Reset • Second Number USB reset counter
PCI	• PCIe Reset • First Number current PCIe Reset • Second Number PCIe reset counter

CPLD Firmware and Statistic over UART

Reference Designs

Link to different Reference Designs (Descriptions and Download)

- TE0803 Reference Designs
- TE0807 Reference Designs
- TE0808 Reference Designs

It's recommended to use prebuilt Boot.bin and image.ub of newest Starterkit Reference Design for first test. Basic Steps:

1. Power Supply over ATX, optional 12V power jack
2. Download Reference Design
3. Copy Boot.bin and image.ub on SD
4. Connect USB to XMOD with Green Dot
5. Open Putty
6. Set Boot Mode to SD, set DIP S5-1 and S5-2 to ON (Overview 5) and inserted SD with Design on SD Slot (Overview R)
7. Press Power Button on Enclosure or on Carrier (Overview 3)
8. For more detailed check Reference Design description

Notes

Module and Carrier are also as starter kit available:

- Starter Kit 803
- Starter Kit 807
- Starter Kit 808

Links to all documentation and download resources:

- TEBF0808 Resources
- TE0808 Resources
- TE0807 Resources
- TE0803 Resources
- TE0790 Resources