AM0010 Test Board

Table of contents

Overview

Refer to https://wiki.trenz.org/am0010-info for the current online version of this manual and other available documentation.

Key Features

- Vitis/Vivado 2023.2
- PetaLinux
- SD (2.0)
- ETH
- USB (2.0)
- I2C
- eMMC
- FMeter

Revision History

Date	Vivado	Project Built	Authors	Description
2024-01-25	2023.2	AM0010-test_board-vivado_2023.2-build_4_20240124124216.zip AM0010-test_board_noprebuilt-vivado_2023.2-build_4_20240124124216.zip	Manuela Strücker	• Update Vivado 2023.2 • new assembly variants
2023-08-25	2022.2	AM0010-test_board-vivado_2022.2-build_7_20230825125934.zip AM0010-test_board_noprebuilt-vivado_2022.2-build_7_20230825125934.zip	Manuela Strücker	• Update Vivado 2022.2 • new assembly variants
2021-11-19	2020.2	AM0010-test_board-vivado_2020.2-build_9_20211119071538.zip AM0010-test_board_noprebuilt-vivado_2020.2-build_9_20211119072230.zip	Mohsen Chamanbaz / John Hartfiel	• initial release

Design Revision History

Release Notes and Know Issues

Issues	Description	Workaround	To be fixed version

USB	USB3 Stick does not work on USB2 Interface, only USB2 Stick	---	---

Known Issues

Requirements

Software

Software	Version	Note
Vitis	2023.2	needed, Vivado is included into Vitis installation
PetaLinux	2023.2	needed

Software

Hardware

Basic description of TE Board Part Files is available on TE Board Part Files.

Complete List is available on "<project folder>\board_files*_board_files.csv"

Design supports following modules:

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMMC	Others	Notes
AM0010-01-3BI21FA	3eg_1i_4gb	REV01	4GB	128MB	8GB	NA	NA
AM0010-01-3BI21MA*	3eg_1i_4gb	REV01	4GB	128MB	8GB	NA	NA
AM0010-01-4DE21MA	4ev_1e_4gb	REV01	4GB	128MB	8GB	NA	NA
AM0010-01-S001	4ev_1e_4gb	REV01	4GB	128MB	8GB	NA	CS
AM0010-01-S002	4ev_1e_4gb	REV01	4GB	128MB	8GB	NA	CS
AM0010-01-S003	4ev_1e_4gb	REV01	4GB	128MB	8GB	NA	CS reduced comp
AM0010-02-3BE21MA	3eg_1e_4gb	REV02	4GB	128MB	8GB	NA	NA
AM0010-02-3BI21MA	3eg_1i_4gb	REV02	4GB	128MB	8GB	NA	NA
AM0010-02-4AE21MA	4cg_1e_4gb	REV02	4GB	128MB	8GB	NA	NA
AM0010-02-4DE21MA	4ev_1e_4gb	REV02	4GB	128MB	8GB	NA	NA
AM0010-02-5DE21MA	5ev_1e_4gb	REV02	4GB	128MB	8GB	NA	NA
AM0010-02-5DI21MA	5ev_1i_4gb	REV02	4GB	128MB	8GB	NA	NA

*used as reference

Hardware Modules

Design supports following carriers:

Carrier Model	Notes
AMB0010-01*	

*used as reference

Hardware Carrier

Additional HW Requirements:

Additional Hardware	Notes
TE0790 (XMOD FTDI JTAG Adapter)	
Heat sink	
Mini-USB cable	
12V Power supply	
SD card	

*used as reference

Additional Hardware

Content

For general structure and usage of the reference design, see Project Delivery - AMD devices

Design Sources

Type	Location	Notes
Vivado	<project folder>\block_design <project folder>\constraints <project folder>\ip_lib <project folder>\board_files	Vivado Project will be generated by TE Scripts
Vitis	<project folder>\sw_lib	Additional Software Template for Vitis and apps_list.csv with settings automatically for Vitis app generation
PetaLinux	<project folder>\os\petalinux	PetaLinux template with current configuration

Design sources

Additional Sources

Type	Location	Notes
init.sh	<project folder>\misc\sd\	Additional Initialization Script for Linux

Additional design sources

Prebuilt

File	File-Extension	Description
BIF-File	*.bif	File with description to generate Bin-File
BIN-File	*.bin	Flash Configuration File with Boot-Image (Zynq-FPGAs)
BIT-File	*.bit	FPGA (PL Part) Configuration File
Boot Script-File	*.scr	Distro Boot Script file
DebugProbes-File	*.ltx	Definition File for Vivado/Vivado Labtools Debugging Interface
Diverse Reports	---	Report files in different formats
Device Tree	*.dts	Device tree (2 possible, one for u-boot and one for linux)
Hardware-Platform-Description-File	*.xsa	Exported Vivado hardware description file for Vitis and PetaLinux
LabTools Project-File	*.lpr	Vivado Labtools Project File
OS-Image	*.ub	Image with Linux Kernel (On Petalinux optional with Devicetree and RAM-Disk)
Software-Application-File	*.elf	Software Application for Zynq or MicroBlaze Processor Systems

Prebuilt files (only on ZIP with prebuilt content)

Download

Reference Design is only usable with the specified Vivado/Vitis/PetaLinux version. Do never use different Versions of Xilinx Software for the same Project.

Reference Design is available on:

- AM0010 "Test Board" Reference Design

Design Flow

> ⚠ Reference Design is available with and without prebuilt files. It's recommended to use TE prebuilt files for first launch.

Trenz Electronic provides a tcl based built environment based on Xilinx Design Flow.

See also:

- AMD Development Tools#XilinxSoftware-BasicUserGuides
- Vivado Projects - TE Reference Design
- Project Delivery.

The Trenz Electronic FPGA Reference Designs are TCL-script based project. Command files for execution will be generated with "_create_win_setup.cmd" on Windows OS and "_create_linux_setup.sh" on Linux OS.

TE Scripts are only needed to generate the vivado project, all other additional steps are optional and can also executed by Xilinx Vivado/Vitis GUI. For currently Scripts limitations on Win and Linux OS see: Project Delivery Currently limitations of functionality

> ⚠ **Caution!** Win OS has a 260 character limit for path lengths which can affect the Vivado tools. To avoid this issue, use Virtual Drive or the shortest possible names and directory locations for the reference design (for example "x:\<project folder>")

1. Run _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell:

_create_win_setup.cmd/_create_linux_setup.sh

```
------------------------Set design paths----------------------------
-- Run Design with: _create_win_setup
-- Use Design Path: <absolute project path>
--------------------------------------------------------------------
-------------------------TE Reference
Design---------------------------
--------------------------------------------------------------------
-- (0)  Module selection guide, project creation...prebuilt export...
-- (1)  Create minimum setup of CMD-Files and exit Batch
-- (2)  Create maximum setup of CMD-Files and exit Batch
-- (3)  (internal only) Dev
-- (4)  (internal only) Prod
-- (c)  Go to CMD-File Generation (Manual setup)
-- (d)  Go to Documentation (Web Documentation)
-- (g)  Install Board Files from Xilinx Board Store (beta)
-- (a)  Start design with unsupported Vivado Version (beta)
-- (x)  Exit Batch (nothing is done!)
----
Select (ex.:'0' for module selection guide):
```

2. Press 0 and enter to start "Module Selection Guide"
3. Create project and follow instructions of the product selection guide, settings file will be configured automatically during this process.
   - optional for manual changes: Select correct device and Xilinx install path on "design_basic_settings.cmd" and create Vivado project with "vivado_create_project_guimode.cmd"

     > ⚠ Note: Select correct one, see also Vivado Board Part Flow

4. Create hardware description file (.xsa file) for PetaLinux project and export to prebuilt folder

run on Vivado TCL (Script generates design and export files into "<project folder>\prebuilt\hardware\<short name>")

```
TE::hw_build_design -export_prebuilt
```

> Using Vivado GUI is the same, except file export to prebuilt folder.

5. Create and configure your PetaLinux project with exported .xsa-file, see PetaLinux KICKstart
    - use TE Template from "<project folder>\os\petalinux"
    - use exported .xsa file from "<project folder>\prebuilt\hardware\<short name>" . **Note:** HW Export from Vivado GUI creates another path as default workspace.
    - The build images are located in the "<plnx-proj-root>/images/linux" directory
6. Configure the **boot.scr** file as needed, see Distro Boot with Boot.scr
7. Generate Programming Files with Vitis (recommended)
    a. Copy PetaLinux build image files to prebuilt folder
        - copy **u-boot.elf**, **system.dtb**, **image.ub** and **boot.scr** from "<plnx-proj-root>/images/linux" to prebuilt folder

        > "<project folder>\prebuilt\os\petalinux\<ddr size>" or "<project folder>\prebuilt\os\petalinux\<short name>"

    b. Generate Programming Files with Vitis

run on Vivado TCL (Script generates applications and bootable files, which are defined in "test_board\sw_lib\apps_list.csv")
`TE::sw_run_vitis -all` `TE::sw_run_vitis (optional; Start Vitis from Vivado GUI or start with TE Scripts on Vivado TCL)`

    > TCL scripts generate also platform project, this must be done manually in case GUI is used. See Vitis

8. Generate Programming Files with Petalinux (alternative), see PetaLinux KICKstart

Launch

Programming

> Check Module and Carrier TRMs for proper HW configuration before you try any design.
>
> Reference Design is also available with prebuilt files. It's recommended to use TE prebuilt files for first launch.

Xilinx documentation for programming and debugging: Vivado/Vitis/SDSoC-Xilinx Software Programming and Debugging

Get prebuilt boot binaries

1. Run _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell
2. Press 0 and enter to start "Module Selection Guide"
    a. Select assembly version
    b. Validate selection
    c. Select create and open delivery binary folder

> Note: Folder "<project folder>_binaries_<Article Name>" with subfolder "boot_<app name>" for different applications will be generated

QSPI-Boot mode

Option for **Boot.bin** on QSPI Flash and **image.ub** and **boot.scr** on **SD** or **USB**.

1. Connect **JTAG** and power on carrier with module
2. Open Vivado Project with "vivado_open_existing_project_guimode.cmd" or if not created, create with "vivado_create_project_guimode.cmd"

run on Vivado TCL (Script programs BOOT.bin on QSPI flash)
`TE::pr_program_flash -swapp u-boot` `TE::pr_program_flash -swapp hello_am0010 (optional)`

> To program with Vitis/Vivado GUI, use special FSBL (fsbl_flash) on setup

3. Copy **image.ub** and **boot.scr** on **SD** or **USB**
    - use files from "<project folder>_binaries_<Article Name>\boot_linux" from generated binary folder,see: Get prebuilt boot binaries
    - or use prebuilt file location, see "<project folder>\prebuilt\file_location.txt"
4. Set Boot Mode to **QSPI-Boot** and insert **SD** or **USB**.
    - Depends on Carrier, see carrier TRM.

SD-Boot mode

1. Copy **image.ub**, **boot.src** and **Boot.bin** on **SD**
    - use files from "<project folder>_binaries_<Article Name>\boot_linux" from generated binary folder, see: Get prebuilt boot binaries
    - or use prebuilt file location, see "<project folder>\prebuilt\file_location.txt"
2. Set Boot Mode to SD-Boot.
    - Depends on Carrier, see carrier TRM.
3. Insert SD-Card in SD-Slot.

JTAG

Not used on this example.

Usage

1. Prepare HW like described on section Programming
2. Connect UART USB (most cases same as JTAG)
3. Select SD Card as Boot Mode (or QSPI - depending on step 1)

> Note: See TRM of the Carrier, which is used.

> Starting with Petalinux version 2020.1, the industry standard "Distro-Boot" boot flow for U-Boot was introduced, which significantly expands the possibilities of the boot process and has the primary goal of making booting much more standardised and predictable.
> The boot options described above describe the common boot processes for this hardware; other boot options are possible.
> For more information see Distro Boot with Boot.scr

4. Power On PCB

   1. ZynqMP Boot ROM loads FSBL from SD/QSPI into OCM,

   2. FSBL init the PS, programs the PL using the bitstream and loads PMU, ATF and U-boot from SD/QSPI into DDR,

   3. U-boot loads Linux (**image.ub**) from SD/QSPI/... into DDR

Linux

1. Open Serial Console (e.g. putty)
   - Speed: 115200
   - select COM Port

   > Win OS, see device manager, Linux OS see dmesg |grep tty (UART is *USB1)

2. Linux Console:

```
# password disabled
petalinux login: root
Password: root
```

   > Note: Wait until Linux boot finished

3. You can use Linux shell now.

```
i2cdetect -y -r 0        (check I2C 0 Bus)
i2cdetect -y -r 1   (check I2C 1 Bus)
udhcpc                                (ETH0 check)
lsusb                                (USB check)
```

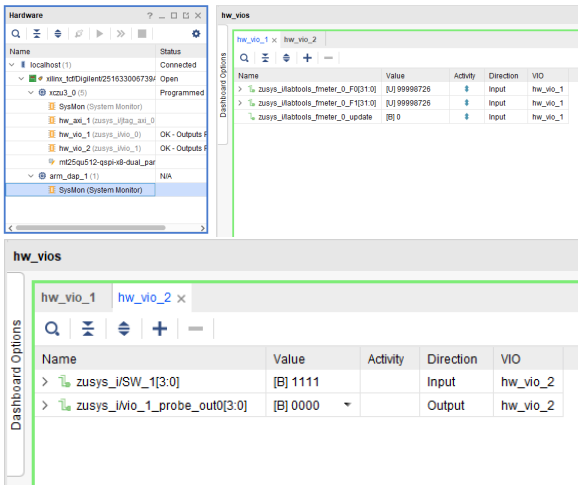
4. Option Features

   - Webserver to get access to Zynq
     - insert IP on web browser to start web interface
   - init.sh scripts
     - add init.sh script on SD, content will be load automatically on startup (template included in "<project folder>\misc\SD")

Vivado HW Manager

Open Vivado HW-Manager and add VIO signal to dashboard (*.ltx located on prebuilt folder)

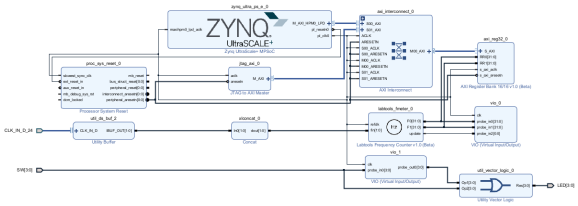
- Control: Dip switches and LEDs
- Monitoring: Output clock of SI53340 clock buffer with 2:1 input mux



Vivado Hardware Manager

System Design - Vivado

Block Design



Block Design

PS Interfaces

Activated interfaces:

Type	Note
DDR	
QSPI	MIO
SD0 (eMMC)	MIO
SD1 (as SD2.0)	MIO
I2C0	MIO

I2C1	MIO
UART0	MIO
UART1	MIO
GPIO0..2	MIO
SWDT0..1	
TTC0..3	
GEM3	MIO
USB0 (as USB2.0)	MIO

PS Interfaces

Constrains

Basic module constrains

_i_bitgen_common.xdc

```
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property BITSTREAM.CONFIG.UNUSEDPIN PULLNONE [current_design]
```

Design specific constrain

_i_io.xdc

```
##############################################
#CLOCKs
##############################################
#   Y6       B224_CLK0_P
#   Y5       B224_CLK0_N
#   V6       B224_CLK1_P
#   V5
B224_CLK1_N
#set_property -dict { IOSTANDARD LVDS_25 PACKAGE_PIN Y6 } [get_ports
{CLK_IN_D_224_clk_p[0]}]
#set_property -dict { IOSTANDARD LVDS_25 PACKAGE_PIN V6 } [get_ports
{CLK_IN_D_224_clk_p[1]}]
#   AA13     B24_L7_P
#   AB13     B24_L7_N
#   AC14     B24_L6_P
#   AC13     B24_L6_N
set_property -dict { IOSTANDARD LVDS_25 PACKAGE_PIN AA13 } [get_ports
{CLK_IN_D_24_clk_p[0]}]
set_property -dict { IOSTANDARD LVDS_25 PACKAGE_PIN AC14 } [get_ports
{CLK_IN_D_24_clk_p[1]}]

##############################################
#LED and DIP Switch
##############################################
#   D15      USER_LED[0]
#   D14      USER_LED[1]
```

```
#   G15      USER_LED[2]
#   G14      USER_LED[3]
set_property -dict { IOSTANDARD LVCMOS33 PACKAGE_PIN D15 } [get_ports {LED
[0]}]
set_property -dict { IOSTANDARD LVCMOS33 PACKAGE_PIN D14 } [get_ports {LED
[1]}]
set_property -dict { IOSTANDARD LVCMOS33 PACKAGE_PIN G15 } [get_ports {LED
[2]}]
set_property -dict { IOSTANDARD LVCMOS33 PACKAGE_PIN G14 } [get_ports {LED
[3]}]
#   F13      USER_SW[0]
#   G13      USER_SW[1]
#   E15      USER_SW[2]
#   F15      USER_SW[3]
set_property -dict { IOSTANDARD LVCMOS33 PACKAGE_PIN F13 } [get_ports {SW
[0]}]
set_property -dict { IOSTANDARD LVCMOS33 PACKAGE_PIN G13 } [get_ports {SW
[1]}]
set_property -dict { IOSTANDARD LVCMOS33 PACKAGE_PIN E15 } [get_ports {SW
[2]}]
set_property -dict { IOSTANDARD LVCMOS33 PACKAGE_PIN F15 } [get_ports {SW
[3]}]
##############################################
#HYPERRAM
##############################################
# #CK
# set_property PACKAGE_PIN AG10 [get_ports CLK_P]
# #CKN/RFU
# set_property PACKAGE_PIN AH10 [get_ports CLK_N]
# #DQ0..7
# set_property PACKAGE_PIN AB9  [get_ports {D[0]}]
# set_property PACKAGE_PIN AC11 [get_ports {D[1]}]
# set_property PACKAGE_PIN Y10  [get_ports {D[2]}]
# set_property PACKAGE_PIN AA8  [get_ports {D[3]}]
# set_property PACKAGE_PIN Y9   [get_ports {D[4]}]
# set_property PACKAGE_PIN AD11 [get_ports {D[5]}]
# set_property PACKAGE_PIN AB10 [get_ports {D[6]}]
# set_property PACKAGE_PIN AF10 [get_ports {D[7]}]
# #RWDS/RDS
# set_property PACKAGE_PIN AA10 [get_ports RWDS]
# #CSN
# set_property PACKAGE_PIN AD10 [get_ports CS0_N ]
# #RFU
# set_property PACKAGE_PIN AE10 [get_ports CS1_N]
# #RESETN
# set_property PACKAGE_PIN AB11 [get_ports RESET_N]
# #INT
# set_property PACKAGE_PIN AA11 [get_ports INT_N ]
```

Software Design - Vitis

For Vitis project creation, follow instructions from:

Vitis

Application

Template location: "<project folder>\sw_lib\sw_apps\"

zynqmp_fsbl

TE modified 2023.2 FSBL

General:

- Modified Files: xfsbl_main.c, xfsbl_hooks.h/.c, xfsbl_board.h/.c (search for 'TE Mod' on source code)
- Add Files: te_xfsbl_hooks.h/.c (for hooks and board)
- General Changes:
    - Display FSBL Banner and Device Name

Module Specific:

- Add Files: all TE Files start with te_*
    - ETH+OTG Reset over MIO
    - USB Reset over MIO
    - eMMC Reset over MIO

zynqmp_pmufw

Xilinx default PMU firmware.

General Example:

hello_am0010

Hello AM0010 is a Xilinx Hello World example as endless loop instead of one console output.

u-boot

U-Boot.elf is generated with PetaLinux. Vitis is used to generate Boot.bin.

Software Design - PetaLinux

For PetaLinux installation and project creation, follow instructions from:

- PetaLinux KICKstart

Config

Start with **petalinux-config** or **petalinux-config --get-hw-description**

Changes:

- select SD default instead of eMMC:
    - CONFIG_SUBSYSTEM_PRIMARY_SD_PSU_SD_1_SELECT=y
- add new flash partition for bootscr and sizing
    - CONFIG_SUBSYSTEM_FLASH_PSU_QSPI_0_BANKLESS_PART0_SIZE=0xA00000
    - CONFIG_SUBSYSTEM_FLASH_PSU_QSPI_0_BANKLESS_PART1_SIZE=0x2000000
    - CONFIG_SUBSYSTEM_FLASH_PSU_QSPI_0_BANKLESS_PART2_SIZE=0x40000
    - CONFIG_SUBSYSTEM_FLASH_PSU_QSPI_0_BANKLESS_PART3_NAME="bootscr"
    - CONFIG_SUBSYSTEM_FLASH_PSU_QSPI_0_BANKLESS_PART3_SIZE=0x80000
- Identification
    - CONFIG_SUBSYSTEM_HOSTNAME="Trenz"

    - CONFIG_SUBSYSTEM_PRODUCT="AM0010"

U-Boot

Start with **petalinux-config -c u-boot**

Changes:

- MAC from eeprom together with uboot and device tree settings:
    - CONFIG_ENV_OVERWRITE=y
    - CONFIG_NET_RANDOM_ETHADDR is not set
- Boot Modes:
    - CONFIG_QSPI_BOOT=y
    - CONFIG_SD_BOOT=y
    - CONFIG_ENV_IS_IN_FAT is not set
    - CONFIG_ENV_IS_IN_NAND is not set
    - CONFIG_ENV_IS_IN_SPI_FLASH is not set
    - CONFIG_SYS_REDUNDAND_ENVIRONMENT is not set
    - CONFIG_BOOT_SCRIPT_OFFSET=0x2A40000
- Identification
    - CONFIG_IDENT_STRING=" AM0010"

Change platform-top.h:

Device Tree

```
/include/ "system-conf.dtsi"


/*------------------ SD --------------------*/
// eMMC
// &sdhci0 {
//     // disable-wp;
//     no-1-8-v;
// };

// SD card
&sdhci1 {
    disable-wp;
    no-1-8-v;
};


/*-------------------- USB 2.0 only ----------------*/
&dwc3_0 {
    status = "okay";
    dr_mode = "host";
    maximum-speed = "high-speed";
    /delete-property/phy-names;
    /delete-property/phys;
    /delete-property/snps,usb3_lpm_capable;
    snps,dis_u3_susphy_quirk;
    snps,dis_u2_susphy_quirk;
};

&usb0 {
    status = "okay";
    /delete-property/ clocks;
```

```
    /delete-property/ clock-names;
    clocks = <0x3 0x20>;
    clock-names = "bus_clk";
};


/*------------------ ETH PHY --------------------*/
 &gem3 {
    /delete-property/ local-mac-address;
    phy-handle = <&phy0>;

    nvmem-cells = <ð0_addr>;
    nvmem-cell-names = "mac-address";

    phy0: phy@0x3 {
        device_type = "ethernet-phy";
        reg = <0x3>;
    };
};


/*------------------ QSPI -------------------- */
&qspi {
    #address-cells = <1>;
    #size-cells = <0>;
    status = "okay";
    flash0: flash@0 {
        compatible = "jedec,spi-nor";
        reg = <0x0>;
        #address-cells = <1>;
        #size-cells = <1>;

        spi-rx-bus-width = <4>;
        spi-tx-bus-width = <4>;
        spi-max-frequency = <90000000>;
    };
};


/*------------------ I2C --------------------- */
&i2c0 {

    // needs a special wakeup sequence, i2c-detect and similar will not
work
    // https://github.com/Infineon/optiga-trust-m/
    // optiga: optiga@30 {
    //     compatible = "";
    //     reg = <0x30>;
    // };

    eeprom: eeprom@53 {
        compatible = "microchip,24aa025", "atmel,24c02";
        reg = <0x53>;

        #address-cells = <1>;
        #size-cells = <1>;
        eth0_addr: eth-mac-addr@FA {
          reg = <0xFA 0x06>;
        };
    };
```

```
    // needs a special wakeup sequence, i2c-detect and similar will not
work
    // crypto: crypto@60 {
    //     compatible = "atmel,atecc508a", "atmel,atecc608a";
    //     reg = <0x60>;
    // };
};

//&i2c1 {
//  extern: extern@<> {
//     compatible = "";
//     reg = <>;
//  };
//};
```

Kernel

Start with **petalinux-config -c kernel**

Changes:

- Only needed to fix JTAG Debug issue:
  - # CONFIG_CPU_FREQ is not set

Rootfs

Start with **petalinux-config -c rootfs**

Changes:

- For web server app:
  - CONFIG_busybox-httpd=y
- For additional test tools only:
  - CONFIG_i2c-tools=y
  - CONFIG_packagegroup-petalinux-utils=y (util-linux,cpufrequtils,bridge-utils,mtd-utils, usbutils,pciutils,canutils,i2c-tools,smartmontools,e2fsprogs)
- For auto login:
  - CONFIG_imagefeature-serial-autologin-root=y

FSBL patch (alternative for vitis fsbl trenz patch)

See "<project folder>\os\petalinux\project-spec\meta-user\recipes-bsp\embeddedsw"

Applications

See "<project folder>\os\petalinux\project-spec\meta-user\recipes-apps\"

startup

Script App to load init.sh from SD Card if available.

webfwu

Webserver application suitable for ZynqMP access. Need busybox-httpd

Additional Software

No additional software is needed.

App. A: Change History and Legal Notices

Document Change History

To get content of older revision go to "Change History" of this page and select older document revision number.

Date	Document Revision	Authors	Description
Error rendering macro 'page-info' Ambiguous method overloading for method jdk.proxy241.$Proxy3496#hasContentLevelPermission. Cannot resolve	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy241.$Proxy3496#hasContentLevelPermission. Cannot resolve	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy241.$Proxy3496#hasContentLevelPermission. Cannot resolve	• Update Vivado 2023.2 • new assembly variants

which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian

which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian

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2023-08-25	v.11	Manuela Strücker	• Update Vivado 2022.2 • new assembly variants
2021-11-19	v.10	John Hartfiel	• initial release
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			Ambiguous method overloading for method jdk.proxy241.$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between	

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Document change history.

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WEEE

Information for users within the European Union in accordance with Directive 2002/96/EC of the European Parliament and of the Council of 27 January 2003 on waste electrical and electronic equipment (WEEE).

Users of electrical and electronic equipment in private households are required not to dispose of waste electrical and electronic equipment as unsorted municipal waste and to collect such waste electrical and electronic equipment separately. By the 13 August 2005, Member States shall have ensured that systems are set up allowing final holders and distributors to return waste electrical and electronic equipment at least free of charge. Member States shall ensure the availability and accessibility of the necessary collection facilities. Separate collection is the precondition to ensure specific treatment and recycling of waste electrical and electronic equipment and is necessary to achieve the chosen level of protection of human health and the environment in the European Union. Consumers have to actively contribute to the success of such collection and the return of waste electrical and electronic equipment. Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.

Trenz Electronic is registered under WEEE-Reg.-Nr. DE97922676.

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