

CR00100 Test Board

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Refer to https://www.infineon.com/dgdl/CR00100-test_board_noprebuilt-quartus_20.1.1-20220225103813.zip for the current online version of this manual and other available documentation.

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Revision History

Date	Project Built	Authors	Description
2021-04-20	CR00100-test_board_noprebuilt-quartus_21.1.0-20220421150346.zip	Thomas Dück	<ul style="list-style-type: none">update to Quartus Prime Lite 21.1
2021-02-25	CR00100-test_board_noprebuilt-quartus_20.1.1-20220225103813.zip	Thomas Dück	<ul style="list-style-type: none">initial release

Design Revision History

Release Notes and Know Issues

Issues	Description	Workaround	To be fixed version
No known issues	---	---	---

Known Issues

Requirements

Software

Software	Version	Note
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Quartus Prime Lite	21.1	needed
NIOS II SBT for Eclipse	---	optional

Software

Hardware

Complete List is available on `<project folder>/board_files/*_board_files.csv`

Design supports following modules:

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMMC	Others	Notes
CR00100-01-DBC82A*	08_C8_8MB	REV01	8MByte	--	--	--	--
CR00100-01-FBC82A	16_C8_8MB	REV01	8MByte	--	--	--	--

*used as reference

Hardware Modules

Design supports following carriers:

Carrier Model	Notes

*used as reference

Hardware Carrier

Additional HW Requirements:

Additional Hardware	Notes
USB cable for JTAG/UART	Check Carrier Board and Programmer for correct type

*used as reference

Additional Hardware

Content

For general structure and usage of the reference design, see [Project Delivery - Intel devices](#)

Design Sources

Type	Location	Notes
Quartus	<code><project folder>/source_files/quartus</code>	Quartus project will be generated by TE Scripts
Software	<code><project folder>/source_files/software</code>	Additional software will be generated by TE Scripts

Design sources

Prebuilt

File	File-Extension	Description
SOPC Information File	*.sopcinfo	File with description of the .qsys file to create software for the target hardware
SRAM Object File	*.sof	Ram configuration file
Software-Application-File	*.elf	Software application for NIOS II processor system
Diverse Reports	---	Report files in different formats

Prebuilt files (only on ZIP with prebuilt content)

Download

Reference Design is only usable with the specified Quartus version. Do never use different versions of Quartus software for the same project.

Reference Design is available on:

- [CR00100 "Test Board" Reference Design](#)

Design Flow



Reference Design is available with and without prebuilt files. It's recommended to use TE prebuilt files for first launch.

Trenz Electronic provides a tcl based built environment based on Quartus Design Flow.

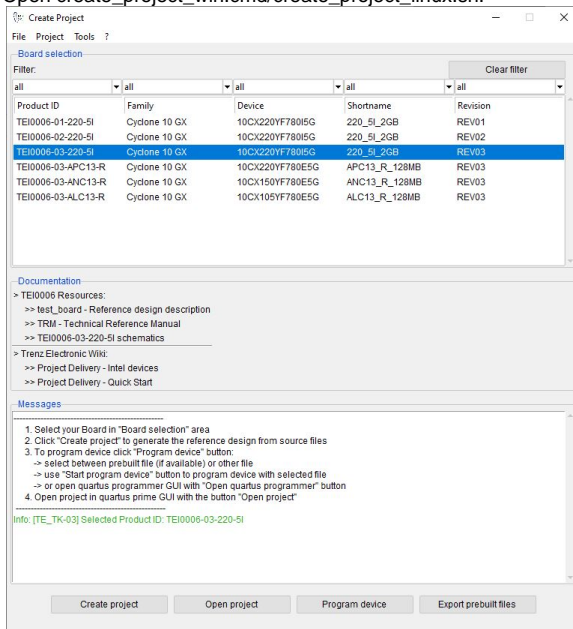
See also:

- [Project Delivery - Intel devices](#)

The Trenz Electronic FPGA Reference Designs are TCL-script based projects. To create a project, open a project or program a device execute "create_project_win.cmd" on Windows OS and "create_project_linux.sh" on Linux OS.

TE Scripts are only needed to generate the quartus project, all other additional steps are optional and can also be executed by Intel Quartus/SDK GUI. For currently Scripts limitations on Win OS and Linux OS see: [Project Delivery - Intel devices](#) [Currently limitations of functionality](#)

1. Open `create_project_win.cmd/create_project_linux.sh`:



'Create Project' GUI example

2. Select Board in "Board selection"
3. Click on "Create project" button to create project
 - a. (optional for manual changes) Select correct quartus installation path in "`<project folder>/settings/design_basic_settings.tcl`"

Launch

Programming



Check Module and Carrier TRMs for proper HW configuration before you try any design.

MAX10 Flash

1. Connect JTAG and power on carrier with module
2. Open `create_project_win.cmd/create_project_linux.sh`
3. Select correct board in "Board selection"
4. Click on "Program device" button
 - a. if prebuilt files are available: select "Program prebuilt file"
 - b. using own generated programming file: select "Program other file" and click on "Browse ..." to open own generated programming file
 - c. (optional) click on "Open programmer GUI" to program device with Quartus programmer GUI
5. Click on "Start program device" button

JTAG

Not used on this example.

Usage

1. Prepare HW like described on section [Programming](#)
2. Connect UART USB (most cases same as JTAG)
3. Power on PCB
4. Press user button 'S2' to toggle between two frequencies for the blinking led 'LED2'

UART

1. Open Serial Console (e.g. PuTTY)
 - a. select COM Port

Win OS: see device manager

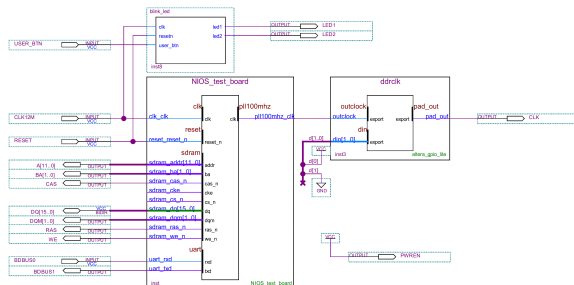
Linux OS: see `dmesg | grep tty` (UART is *USB1)

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- b. Speed: 115200
2. Press reset button
3. Console output depends on used Software project, see [Software Design - SDK#Application](#)

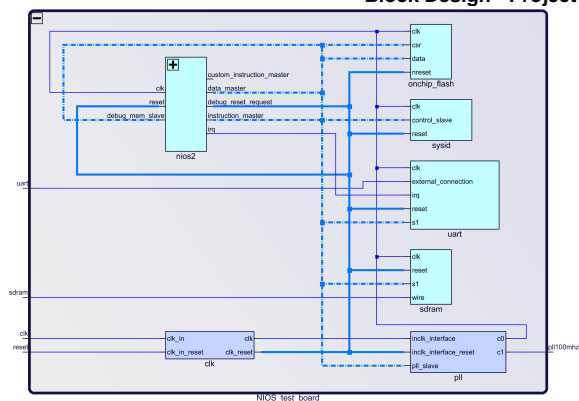
System Design - Quartus

Block Design

The block designs may differ depending on the assembly variant.



Block Design - Project



Block Design - Platform Designer

Software Design - SDK

Application

Used software project depends on board assembly variant. Template location: *<project folder>/source_files/software/*

hello_cr00100

This is a Hello World example as endless loop instead of one console output.

Appx. A: Change History and Legal Notices

Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

Date	Document Revision	Authors	Description
<div>Error rendering macro 'page-info'</div> <div>Ambiguous method overload ing for method jdk. proxy24 1.\$Proxy 3496#hasContentLevelPermission</div>	<div>Error rendering macro 'page-info'</div> <div>Ambiguous method overload ing for method jdk. proxy24 1.\$Proxy 3496#hasContentLevelPermission</div>	<div>Error rendering macro 'page-info'</div> <div>Ambiguous method overload ing for method jdk. proxy24 1.\$Proxy 3496#hasContentLevelPermission</div>	<div>• update to Quartus Prime Lite 21.1</div>

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2022-03-01	v.4	Thomas Dück	<ul style="list-style-type: none">initial release 20.1
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Document change history

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Error rendering macro 'page-info'

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invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due
to overlapping prototypes between: [interface com.atlassian.confluence.user.
ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.
ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class
com.atlassian.confluence.core.ContentEntityObject]