PCN-20220309 TE0715-04 to TE0715-05 Hardware Revision Change

Download PDF version of this document.

Company	Trenz Electronic GmbH
PCN Number	PCN-20220309
Title	TE0715-04 to TE0715-05 Hardware Revision Change
Subject	Hardware Revision Change
Issue Date	2022-03-14

Products Affected

This change affects all Trenz Electronic TE0715 SoMs of revision 04.

Affected Product	Replacement
TE0715-04-*	TE0715-05-*

Changes

#1 Replace EN6347QI (U1) by MPM3840GQV-Z.

Type: Schematic Change

Reason: Enpirion DCDCs are discontinued.

Impact: None.

#2 Replace TPS82085SIL (U2, U3, U8, U24) by MPM3834CGPA.

Type: Schematic Change

Reason: Supply chain optimization.

Impact: None.

#3 Replace TPS27082LDDCR (Q1) by MP5077GG-Z.

Type: Schematic Change

Reason: Supply chain optimization.

Impact: None.

#4 Add power supervisor BD39040MUF (U25).

Type: Schematic Change

Reason: Improved voltage rail supervision.

Impact: None. More power rails are now monitored.

#5 Add protection diode D5 to U23.3 (#MR input).

Type: Schematic Change

Reason: Avoid voltage high-signal-state at U23 manual reset pin 3 without powered supervisor.

Impact: None.

#6 Connect power supervisor U23 to 3.3VIN power rail (was 3.3V).

Type: Schematic Change

Reason: Avoid high-signal-state at U23 manual reset pin 3 without powered supervisor.

Impact: None.

#7 Change voltage divider resistors (R56, R58) to set the threshold for U23.

Type: Schematic Change

Reason: Set reset threshold for U26 to 0.905 V.

Impact: None. Improved reset behaviour.

#8 Change net name "PG_DDR_PWR" to "PG_AII" and connect BD39040MUF "PG_AII" - signal U25.15 to system controller U26.27 with pull-up resistor R67.

Type: Schematic Change

Reason: Power supervisor connection.

Impact: None. If custom CPLD design used, check for compatibility.

#9 Connect MIO8-Signal "SPE_SCK_FB/VCFG1" (U5.E18) to system controller (U26.8).

Type: Schematic Change

Reason: Enable boundary scan for MIO bank 1.

Impact: None. If custom CPLD design used, check for compatibility.

#10 Connect net "PS-POR-B" via resistor R75 net name "RST" to system controller (U26.9).

Type: Schematic Change

Reason: Monitor or set POR-signal.

Impact: None. If custom CPLD design used, check for compatibility.

#11 Change pull-down/floating status for U5.T16 and U5.U16 for revision indicator.

Type: Schematic Change

Reason: Revision indicator via pins.

Impact: None.

#12 Remove GND connection from FPGA "RSVDGND" pin (U5.G12).

Type: Schematic Change

Reason: Xilinx recommendation.

Impact: None.

#13 Replace BKP0603HS121-T (L1, L2, L3, L4, L5, L6, L7, L8, L9, L11) by MPZ0603S121HT000.

Type: Schematic Change

Reason: Ferrite beads are discontinued.

Impact: None.

#14 Change decoupling capacitor (C9, C30) from net "1.8V" at pin U5 bank 501 to net "1V".

Type: Schematic Change

Reason: Decoupling improvement for "1V" voltage rail.

Impact: None.

#15 Remove decoupling capacitor (C12) for net "1.8V" at pin U5 bank 501.

Type: Schematic Change

Reason: Xilinx decoupling recommendation.

Impact: None. Designator changed.

#16 Add decoupling capacitor (C50, C51, C88, C89, C108, C118) for net "1V".

Type: Schematic Change

Reason: Decoupling improvement for "1V" voltage rail.

Impact: None.

#17 Change decoupling capacitor (C21, C144) for VCCPLL.

Type: Schematic Change

Reason: Decoupling improvement for VCCPLL.

Impact: None.

#18 Add/Change decoupling capacitor (C107, C128) for VCCAUX and VCCPAUX.

Type: Schematic Change

Reason: Decoupling improvement for VCCAUX and VCCPAUX.

Impact: None.

#19 Add decoupling capacitor (C128) for AVDD3.

Type: Schematic Change

Reason: BOM Optimization.

Impact: None.

#20 Change decoupling capacitor (C136, C142, C139, C145) for net DDR_PWR.

Type: Schematic Change

Reason: Decoupling improvement for VCCPLL.

Impact: None.

#21 Add/Change decoupling capacitor (C50, C51, C86, C88, C89, C108, C118) for VCCBRAM.

Type: Schematic Change

Reason: Decoupling improvement for VCCBRAM.

Impact: None.

#22 Add input capacitor (C153, C154) for DCDC U4.

Type: Schematic Change

 $\textbf{Reason:} \ \, \textbf{Decoupling improvement for VDDQSNS and VDD}.$

Impact: None.

#23 Change resistor (R21) physical size.

Type: Schematic Change **Reason:** BOM Optimization.

Impact: None. Physical dimension changed.

#24 LIB update.

Type: SCH and PCB Change

Reason: Improve production yield.

Impact: None.

#25 Change PCB layout of Samtec B2B signals.

Type: PCB Change

Reason: Result of this PCN changes.

Impact: The length of the tracks has been changed. Pinout of Samtec B2B connectors is not affected. Changed trace length has to be taken into account in existing designs. The trace length for new revision are added to the 4x5 series pinout generator. Please, check if change in trace length still matches your requirements. Adaption of carrier may be necessary.

#26 Change schematic documentation.

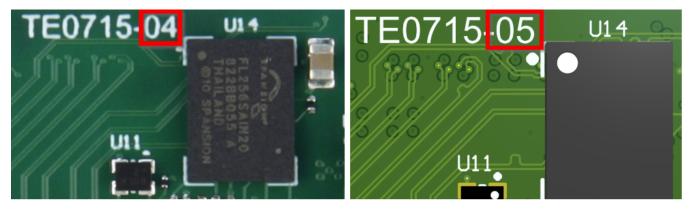
Type: DOC Change

Reason: Documentation optimization.

Impact: None. B2B information, legal notices, revision history, system overview, and power diagram are inserted or changed. Schematic page number changes

Method of Identification

The model code and revision number of the module "TE0715-04" and "TE0715-05" are printed on the top side of the PCB for revision 04 and 05.



Production Shipment Schedule

The new revision 05 will be shipped from November 2022. If the new revision is not suitable for your application and still the former revision of the board is needed, please contact us.

Contact Information

If you have any questions related to this PCN, please contact Trenz Electronics Technical Support at

- forum.trenz-electronic.de
- wiki.trenz-electronic.de
- support%trenz-electronic.de (subject = PCN-20220309)
- phone

 - national calls: 05741 3200-0
 international calls: 0049 5741 3200-0

Disclaimer

Any projected dates in this PCN are based on the most current product information at the time this PCN is being issued, but they may change due to unforeseen circumstances. For the latest schedule and any other information, please contact your local Trenz Electronic sales office, technical support or

This PCN follows JEDEC Standard J-STD-046.