TE0808 Test Board

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Overview

Design Example with minimum PS Setup (DDR, QSPI, UART0) only for custom boards or easier debug via Vitis.

Refer to http://trenz.org/te0808-info for the current online version of this manual and other available documentation.

Key Features

- Vitis/Vivado 2023.2
- QSPI
- Custom Carrier (minimum PS Design with available module components only)
- Modified FSBL (some additional outputs only)

Revision History

Date	Vivado	Project Built	Authors	Description
2024-03-13	2023.2	TE0808-test_board-vivado_2023.2-build_4_20240313130413.zip TE0808-test_board_noprebuilt-vivado_2023.2-build_4_20240313130413.zip	Manuela Strücker	• 2023.2 release • new assembly variants
2023-06-01	2022.2	TE0808-test_board-vivado_2022.2-build_1_20230601101432.zip TE0808-test_board_noprebuilt-vivado_2022.2-build_1_20230601101432.zip	Manuela Strücker	• 2022.2 release • new assembly variants
2023-04-13	2021.2.1	TE0808-test_board-vivado_2021.2-build_20_20230413090245.zip TE0808-test_board_noprebuilt-vivado_2021.2-build_20_20230413090245.zip	Manuela Strücker	• new assembly variants
2022-09-29	2021.2.1	TE0808-test_board-vivado_2021.2-build_17_20220928203325.zip TE0808-test_board_noprebuilt-vivado_2021.2-build_17_20220928203325.zip	Manuela Strücker	• script update • new assembly variants

2022-09-12	2021.2.1	TE0808-test_board-vivado_2021.2-build_15_20220912090608.zip TE0808-test_board_noprebuilt-vivado_2021.2-build_15_20220912090608.zip	Manuela Strücker	• update board part files compatible to Vivado 2021.2.1
2022-03-21	2021.2	TE0808-test_board-vivado_2021.2-build_11_20220321063547.zip TE0808-test_board_noprebuilt-vivado_2021.2-build_11_20220321063547.zip	John Hartfiel	• replace Starterkit FSBL with default one
2022-03-16	2021.2	TE0808-test_board-vivado_2021.2-build_11_20220316091917.zip TE0808-test_board_noprebuilt-vivado_2021.2-build_11_20220316091917.zip	Manuela Strücker	• 2021.2 release • update board files
2021-05-12	2020.2	TE0808-test_board-vivado_2020.2-build_5_20210512133121.zip TE0808-test_board_noprebuilt-vivado_2020.2-build_5_20210512133137.zip	John Hartfiel	• update board files
2021-02-05	2020.2	TE0808-test_board-vivado_2020.2-build_0_20210204141911.zip TE0808-test_board_noprebuilt-vivado_2020.2-build_1_20210204142855.zip	John Hartfiel	• 2020.2 update
2020-09-29	2019.2	TE0808-test_board_noprebuilt-vivado_2019.2-build_15_20200929070740.zip TE0808-test_board-vivado_2019.2-build_15_20200929070725	John Hartfiel	• bugfix 8GB board parts
2020-09-22	2019.2	TE0808-test_board_noprebuilt-vivado_2019.2-build_14_20200922073159.zip TE0808-test_board-vivado_2019.2-build_14_20200922073144.zip	John Hartfiel	• new assembly variants

2020-03-25	2019.2	TE0808-test_board_noprebuilt-vivado_2019.2-build_8_20200325083246.zip TE0808-test_board-vivado_2019.2-build_8_20200325083204.zip	John Hartfiel	• script update
2020-01-22	2019.2	TE0808-test_board_noprebuilt-vivado_2019.2-build_3_20200122142231.zip TE0808-test_board-vivado_2019.2-build_3_20200122142208.zip	John Hartfiel	• 2019.2 update • Vitis support
2019-08-09	2018.3	TE0808-test_board_noprebuilt-vivado_2018.3-build_07_20190809131546.zip TE0808-test_board-vivado_2018.3-build_07_20190809131522.zip	John Hartfiel	• new assembly variants
2019-05-06	2018.3	TE0808-test_board_noprebuilt-vivado_2018.3-build_05_20190507124141.zip TE0808-test_board-vivado_2018.3-build_05_20190507124130.zip	John Hartfiel	• custom FSBL
2018-07-11	2018.2	TE0808-test_board_noprebuilt-vivado_2018.2-build_02_20180711143743.zip TE0808-test_board-vivado_2018.2-build_02_20180711143702.zip	John Hartfiel	• additional notes for FSBL generated with Win SDK • changed *.bif
2018-03-29	2017.4	TE0808-test_board-vivado_2017.4-build_07_20180329151341.zip TE0808-test_board_noprebuilt-vivado_2017.4-build_07_20180329151355.zip	John Hartfiel	• new assembly variant
2018-01-16	2017.4	TE0808-test_board-vivado_2017.4-build_04_20180116144644.zip TE0808-test_board_noprebuilt-vivado_2017.4-build_04_20180116144657.zip	John Hartfiel	• Update Board Part for TEBF0808 ◦ no changes for test board design and minimal board parts

2018-01-15	2017.4	TE0808-test_board-vivado_2017.4-build_03_20180115084954.zip TE0808-test_board_noprebuilt-vivado_2017.4-build_03_20180115085020.zip	John Hartfiel	• rework Board Part Files
2017-12-20	2017.2	TE0808-test_board-vivado_2017.2-build_07_20171220192501.zip TE0808-test_board_noprebuilt-vivado_2017.2-build_07_20171220192448.zip	John Hartfiel	• Update Board Part Files
2017-11-22	2017.2	TE0808-test_board-vivado_2017.2-build_05_20171122080211.zip TE0808-test_board_noprebuilt-vivado_2017.2-build_05_20171122080228.zip	John Hartfiel	• Update Board Part CSV File • Regenerate design
2017-11-16	2017.2	TE0808-test_board-vivado_2017.2-build_05_20171116151545.zip TE0808-test_board_noprebuilt-vivado_2017.2-build_05_20171116151600.zip	John Hartfiel	• Update Board Part CSV File with new Flash assembly variants
2017-11-13	2017.2	TE0808-test_board-vivado_2017.2-build_05_20171113140954.zip TE0808-test_board_noprebuilt-vivado_2017.2-build_05_20171113141908.zip	John Hartfiel	• initial release

Design Revision History

Release Notes and Know Issues

Issues	Description	Workaround	To be fixed version
Xilinx Software	Incompatibility of board files for ZynqMP with eMMC activated between 2021.2 and 2021.2.1 patch, see Xilinx Forum Request	use corresponding board files for the Vivado versions	--
QSPI Flash	Flash programming is not supported with boot mode QSPI or SD.	If flash programming fails, configure device for JTAG boot mode and try again or use older Vivado Versions for programming. (Vivado 2020.2 or 2019.2)	--

Known Issues

Requirements

Software

Software	Version	Note
Vitis	2023.2	needed, Vivado is included into Vitis installation

Software

Hardware

Basic description of TE Board Part Files is available on TE Board Part Files.

Complete List is available on "<project folder>\board_files*_board_files.csv"

Design supports following modules:

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMMC	Others	Notes
~~TE0808-ES1~~	es1_2gb	REV03|REV02	2GB	64MB	NA	NA	Not longer supported by vivado
~~TE0808-ES2~~	es2_2gb	REV04|REV03	2GB	64MB	NA	NA	Not longer supported by vivado
~~TE0808-2ES2~~	2es2_2gb	REV04|REV03	2GB	64MB	NA	NA	Not longer supported by vivado
TE0808-04-06EG-1E3	6eg_1e_4gb	REV04	4GB	128MB	NA	1 mm connectors	NA
TE0808-04-06EG-1EE	6eg_1e_4gb	REV04	4GB	128MB	NA	NA	NA
TE0808-04-09EG-1EA	9eg_1e_2gb	REV04	2GB	64MB	NA	NA	NA
TE0808-04-09EG-1EB	9eg_1e_4gb	REV04	4GB	64MB	NA	NA	NA
TE0808-04-09EG-1ED	9eg_1e_4gb	REV04	4GB	64MB	NA	1 mm connectors	NA
TE0808-04-09EG-1EE	9eg_1e_4gb	REV04	4GB	128MB	NA	NA	NA
TE0808-04-09EG-1EL	9eg_1e_4gb	REV04	4GB	128MB	NA	1 mm connectors	NA
TE0808-04-09EG-2IB	9eg_2i_4gb	REV04	4GB	64MB	NA	NA	NA
TE0808-04-09EG-2IE	9eg_2i_4gb	REV04	4GB	128MB	NA	NA	NA
TE0808-04-6BE21-A	6eg_1e_4gb	REV04	4GB	128MB	NA	NA	NA
TE0808-04-6BE21-L	6eg_1e_4gb	REV04	4GB	128MB	NA	1 mm connectors	NA
TE0808-04-6BI21-A	6eg_1i_4gb	REV04	4GB	128MB	NA	NA	NA
TE0808-04-6BI21-X	6eg_1i_4gb	REV04	4GB	128MB	NA	NA	U41 replaced with schottky diodes

TE0808-04-6GI21-L	6eg_2i_4gb	REV04	4GB	128MB	NA	1 mm connectors	NA
TE0808-04-9BE21-A	9eg_1e_4gb	REV04	4GB	128MB	NA	NA	NA
TE0808-04-9BE21-L	9eg_1e_4gb	REV04	4GB	128MB	NA	1 mm connectors	NA
TE0808-04-9GI21-A	9eg_2i_4gb	REV04	4GB	128MB	NA	NA	NA
TE0808-04-15EG-1EB	15eg_1e_4gb	REV04	4GB	64MB	NA	NA	NA
TE0808-04-15EG-1EE	15eg_1e_4gb	REV04	4GB	128MB	NA	NA	NA
TE0808-04-BBE21-A	15eg_1e_4gb	REV04	4GB	128MB	NA	NA	NA
TE0808-05-6BE21-A	6eg_1e_4gb	REV05	4GB	128MB	NA	NA	NA
TE0808-05-6BE21-F	6eg_1e_4gb	REV05	4GB	128MB	NA	NA	NA
TE0808-05-6BE21-AK	6eg_1e_4gb	REV05	4GB	128MB	NA	NA	NA
TE0808-05-6BE21-L	6eg_1e_4gb	REV05	4GB	128MB	NA	1 mm connectors	NA
TE0808-05-6BI21-D	6eg_1i_4gb	REV05	4GB	128MB	NA	1 mm connectors	SoC without encryption
TE0808-05-6BI21-X	6eg_1i_4gb	REV05	4GB	128MB	NA	NA	U41 replaced with schottky diodes
TE0808-05-6BI41-X	6eg_1i_8gb	REV05	8GB	128MB	NA	NA	Single Die DDR; U41 replaced with schottky diodes
TE0808-05-9BE21-A	9eg_1e_4gb	REV05	4GB	128MB	NA	NA	NA
TE0808-05-9BE21-AK	9eg_1e_4gb	REV05	4GB	128MB	NA	1 mm connectors	NA
TE0808-05-9BE21-AZ	9eg_1e_4gb	REV05	4GB	128MB	NA	1 mm connectors	NA
TE0808-05-9BE21-KZ	9eg_1e_4gb	REV05	4GB	128MB	NA	1 mm connectors	NA
TE0808-05-9BE21-L	9eg_1e_4gb	REV05	4GB	128MB	NA	1 mm connectors	NA
TE0808-05-9BE21-LK	9eg_1e_4gb	REV05	4GB	128MB	NA	1 mm connectors	NA
TE0808-05-9BE21-LZ	9eg_1e_4gb	REV05	4GB	128MB	NA	1 mm connectors	NA
TE0808-05-9BE81-A	9eg_1e_4gb	REV05	4GB	128MB	NA	NA	NA
TE0808-05-9BI41-X	9eg_1i_8gb	REV05	8GB	128MB	NA	NA	Single Die DDR; U41 replaced with schottky diodes
TE0808-05-9GI21-A	9eg_2i_4gb	REV05	4GB	128MB	NA	NA	NA
TE0808-05-9GI21-AK	9eg_2i_4gb	REV05	4GB	128MB	NA	NA	NA
TE0808-05-9GI21-AZ	9eg_2i_4gb	REV05	4GB	128MB	NA	NA	NA
TE0808-05-9GI21-C	9eg_2i_4gb	REV05	4GB	128MB	NA	NA	SoC without encryption
TE0808-05-9GI21-KZ	9eg_2i_4gb	REV05	4GB	128MB	NA	CAO	CAO

TE0808-05-BBE21-A	15eg_1e_4gb	REV05	4GB	128MB	NA	NA	NA
TE0808-05-BBE21-AK	15eg_1e_4gb	REV05	4GB	128MB	NA	NA	NA
TE0808-05-BBE21-AZ	15eg_1e_4gb	REV05	4GB	128MB	NA	NA	NA
TE0808-05-BBE21-L	15eg_1e_4gb	REV05	4GB	128MB	NA	1 mm connectors	NA
TE0808-05-BBE81-A	15eg_1e_4gb	REV05	4GB	128MB	NA	NA	NA
TE0808-05-BBE81-E	15eg_1e_4gb	REV05	4GB	128MB	NA	NA	NA
TE0808-05-BBE81-EK	15eg_1e_4gb	REV05	4GB	128MB	NA	NA	NA
TE0808-05-S001	9eg_1e_8gb_D	REV05	8GB	128MB	NA	CAO	CAO;Single Die DDR
TE0808-05-S002	15eg_1e_4gb	REV05	4GB	128MB	NA	CAO	CAO
TE0808-05-S003	15eg_1e_4gb	REV05	4GB	128MB	NA	CAO	CAO
TE0808-05-S004	9eg_2i_4gb	REV05	4GB	128MB	NA	CAO	CAO
TE0808-05-S005	9eg_2i_4gb	REV05	4GB	128MB	NA	CAO	CAO
TE0808-05-S006	9eg_2i_4gb	REV05	4GB	128MB	NA	CAO	CAO
TE0808-05-S007	9eg_1e_4gb	REV05	4GB	128MB	NA	NA	CAO
TE0808-05-S014	9eg_1e_4gb	REV05	4GB	128MB	NA	NA	CAO
TE0808-05-S016	9eg_1e_4gb	REV05	4GB	128MB	NA	CAO	CAO
TE0808-05-S018	9eg_2e_4gb	REV05	4GB	128MB	NA	CAO	CAO
TE0808-05-S019	9eg_2e_4gb	REV05	4GB	128MB	NA	CAO	CAO
TE0808-05-S020	9eg_2i_4gb	REV05	4GB	128MB	NA	CAO	CAO
TE0808-05-S021	9eg_2i_4gb	REV05	4GB	128MB	NA	CAO	CAO
TE0808-05-S022	6cg_1e_4gb	REV05	4GB	128MB	NA	CAO	CAO
TE0808-05-S025	6eg_1e_4gb_D	REV05	4GB	128MB	NA	CAO	CAO
TE0808-05-S026	9eg_2i_4gb	REV05	4GB	128MB	NA	CAO:Si5345 not assembled	CAO: without PLL
TE0808-05-S027	9eg_2i_4gb	REV05	4GB	128MB	NA	CAO	CAO
TE0808-05-S029	9eg_2i_4gb	REV05	4GB	128MB	NA	CAO	CAO
TE0808-05-S033	15eg_1e_4gb	REV05	4GB	128MB	NA	NA	CAO
TE0808-05-S035	15eg_1e_4gb	REV05	4GB	128MB	NA	CAO	CAO
TE0808-05-S036	15eg_1e_4gb	REV05	4GB	128MB	NA	CAO	CAO
TE0808-05-S038	9eg_1e_4gb	REV05	4GB	128MB	NA	CAO	CAO
TE0808-05-S039	6eg_1e_4gb	REV05	4GB	128MB	NA	CAO	CAO: without PLL

TE0808-05-S041	6eg_1e_4gb_D	REV05	4GB	128MB	NA	CAO	CAO

*used as reference

Hardware Modules

Note: Design contains also Board Part Files for TE0808+TEBF0808 configuration, this board part files are not used for this reference design.

Design supports following carriers:

Carrier Model	Notes
Custom PCB	use simple Board Part files, if MIO connected is different to TEBF0808
TEBF0808*	Used as reference carrier.
TEBT0808-01	Change UART0 to UART1 (MIO68...69) and regenerate design

*used as reference

Hardware Carrier

Additional HW Requirements:

Additional Hardware	Notes
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*used as reference

Additional Hardware

Content

For general structure and usage of the reference design, see Project Delivery - AMD devices

Design Sources

Type	Location	Notes
Vivado	<project folder>\block_design <project folder>\constraints <project folder>\ip_lib <project folder>\board_files	Vivado Project will be generated by TE Scripts
Vitis	<project folder>\sw_lib	Additional Software Template for Vitis and apps_list.csv with settings automatically for Vitis app generation

Design sources

Additional Sources

Type	Location	Notes
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Additional design sources

Prebuilt

File	File-Extension	Description
BIF-File	*.bif	File with description to generate Bin-File
BIN-File	*.bin	Flash Configuration File with Boot-Image (Zynq-FPGAs)
BIT-File	*.bit	FPGA (PL Part) Configuration File
Diverse Reports	---	Report files in different formats
Hardware-Platform-Description-File	*.xsa	Exported Vivado hardware description file for Vitis and PetaLinux
LabTools Project-File	*.lpr	Vivado Labtools Project File
Software-Application-File	*.elf	Software Application for Zynq or MicroBlaze Processor Systems

Prebuilt files (only on ZIP with prebult content)

Download

Reference Design is only usable with the specified Vivado/Vitis/PetaLinux version. Do never use different Versions of Xilinx Software for the same Project.

Reference Design is available on:

- TE0808 "Test Board" Reference Design

Design Flow

Reference Design is available with and without prebuilt files. It's recommended to use TE prebuilt files for first launch.

Trenz Electronic provides a tcl based built environment based on Xilinx Design Flow.

See also:

- AMD Development Tools#XilinxSoftware-BasicUserGuides
- Vivado Projects - TE Reference Design
- Project Delivery.

The Trenz Electronic FPGA Reference Designs are TCL-script based project. Command files for execution will be generated with "_create_win_setup.cmd" on Windows OS and "_create_linux_setup.sh" on Linux OS.

TE Scripts are only needed to generate the vivado project, all other additional steps are optional and can also executed by Xilinx Vivado/Vitis GUI. For currently Scripts limitations on Win and Linux OS see: Project Delivery Currently limitations of functionality

Caution! Win OS has a 260 character limit for path lengths which can affect the Vivado tools. To avoid this issue, use Virtual Drive or the shortest possible names and directory locations for the reference design (for example "x:\<project folder>")

1. Run _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell:

_create_win_setup.cmd/_create_linux_setup.sh

```
------------------------Set design paths---------------------------
-- Run Design with: _create_win_setup
-- Use Design Path: <absolute project path>
-------------------------------------------------------------------
------------------------TE Reference
Design--------------------------
-------------------------------------------------------------------
-- (0)  Module selection guide, project creation...prebuilt export...
-- (1)  Create minimum setup of CMD-Files and exit Batch
-- (2)  Create maximum setup of CMD-Files and exit Batch
-- (3)  (internal only) Dev
-- (4)  (internal only) Prod
-- (c)  Go to CMD-File Generation (Manual setup)
-- (d)  Go to Documentation (Web Documentation)
-- (g)  Install Board Files from Xilinx Board Store (beta)
-- (a)  Start design with unsupported Vivado Version (beta)
-- (x)  Exit Batch (nothing is done!)
----
Select (ex.:'0' for module selection guide):
```

2. Press 0 and enter to start "Module Selection Guide"
3. Create project and follow instructions of the product selection guide, settings file will be configured automatically during this process.
    - optional for manual changes: Select correct device and Xilinx install path on "design_basic_settings.cmd" and create Vivado project with "vivado_create_project_guimode.cmd"

Note: Select correct one, see also Vivado Board Part Flow

Important: Use Board Part Files, which **did not** end with *_tebf0808

4. Create hardware description file (.xsa file) and export to prebuilt folder

run on Vivado TCL (Script generates design and export files into "<project folder>\prebuilt\hardware\<short name>")

```
TE::hw_build_design -export_prebuilt
```

Using Vivado GUI is the same, except file export to prebuilt folder.

5. Generate Programming Files with Vitis

run on Vivado TCL (Script generates applications and bootable files, which are defined in "test_board\sw_lib\apps_list.csv")

```
TE::sw_run_vitis -all
TE::sw_run_vitis (optional; Start Vitis from Vivado GUI or start
with TE Scripts on Vivado TCL)
```

⚠ TCL scripts generate also platform project, this must be done manually in case GUI is used. See Vitis

Launch

Programming

⚠ Check Module and Carrier TRMs for proper HW configuration before you try any design.

Reference Design is also available with prebuilt files. It's recommended to use TE prebuilt files for first launch.

Xilinx documentation for programming and debugging: Vivado/Vitis/SDSoC-Xilinx Software Programming and Debugging

Get prebuilt boot binaries

1. Run _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell
2. Press 0 and enter to start "Module Selection Guide"
    a. Select assembly version
    b. Validate selection
    c. Select create and open delivery binary folder

ⓘ Note: Folder "<project folder>_binaries_<Article Name>" with subfolder "boot_<app name>" for different applications will be generated

QSPI-Boot mode

1. Connect JTAG and power on carrier with module
2. Open Vivado Project with "vivado_open_existing_project_guimode.cmd" or if not created, create with "vivado_create_project_guimode.cmd"

run on Vivado TCL (Script programs BOOT.bin on QSPI flash)

```
TE::pr_program_flash -swapp hello_te0808
```

SD-Boot mode

This does not work, because SD controller is not selected on PS.

JTAG

Load configuration and Application with Vitis Debugger into device

Usage

QSPI Boot:

1. Prepare HW like described on section Programming
2. Connect UART USB (most cases same as JTAG)
3. Select QSPI as Boot Mode

> Note: See TRM of the Carrier, which is used.

4. Power On PCB

   1. ZynqMP Boot ROM FSBL from QSPI into OCM,

   2. FSBL init the PS, programs the PL using the bitstream and loads PMU, ATF and U-boot from QSPI into DDR

System Design - Vivado

Block Design

Block Design

PS Interfaces

Activated interfaces:

Type	Note
DDR	
QSPI	MIO
UART0	MIO, please select other one, if you have connected UART to second controller or other MIO
SWDT0..1	

TTC0..3	

PS Interfaces

Constrains

Basic module constrains

_i_bitgen.xdc

```
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property BITSTREAM.CONFIG.UNUSEDPIN PULLNONE [current_design]
```

Design specific constrain

Not needed.

Software Design - Vitis

For Vitis project creation, follow instructions from:

Vitis

Application

Template location: "<project folder>\sw_lib\sw_apps\"

zynqmp_fsbl

TE modified 2023.2 FSBL

General:

- Modified Files: xfsbl_main.c, xfsbl_hooks.h/.c, xfsbl_board.h/.c (search for 'TE Mod' on source code)
- Add Files: te_xfsbl_hooks.h/.c (for hooks and board)
- General Changes:
  - Display FSBL Banner and Device Name

hello_te0808

Hello TE0808 is a Xilinx Hello World example as endless loop instead of one console output.

Additional Software

No additional software is needed.

Appx. A: Change History and Legal Notices

Document Change History

To get content of older revision go to "Change History" of this page and select older document revision number.

Date	Document Revision	Authors	Description
Error rendering macro 'page-info' Ambiguous method overloading for method jdk.proxy241.$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String,	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy241.$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String,	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy241.$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String,	• 2023.2 release • new assembly variants

class com. atlassian . confluen ce. pages. Page] due to overlapp ing prototyp es between : [interfac e com. atlassian . confluen ce.user. Conflue nceUser , class java. lang. String, class com. atlassian . confluen ce.core. Content EntityOb ject] [interfac e com. atlassian

class com. atlassian . confluen ce. pages. Page] due to overlapp ing prototyp es between : [interfac e com. atlassian . confluen ce.user. Conflue nceUser , class java. lang. String, class com. atlassian . confluen ce.core. Content EntityOb ject] [interfac e com. atlassian

class com. atlassian . confluen ce. pages. Page] due to overlapp ing prototyp es between : [interfac e com. atlassian . confluen ce.user. Conflue nceUser , class java. lang. String, class com. atlassian . confluen ce.core. Content EntityOb ject] [interfac e com. atlassian

.user. User, class java. lang. String, class com. atlassian . confluen ce.core. Content EntityOb ject]	.user. User, class java. lang. String, class com. atlassian . confluen ce.core. Content EntityOb ject]	.user. User, class java. lang. String, class com. atlassian . confluen ce.core. Content EntityOb ject]	
2023-06-14	v.45	Manuela Strücker	• 2022.2 release • new assembly variants
2023-04-13	v.43	Manuela Strücker	• new assembly variants
2022-09-29	v.41	Manuela Strücker	• script update • new assembly variants
2022-09-12	v.40	Manuela Strücker	• update board part files compatible to Vivado 2021.2.1
2022-09-06	v.38	Manuela Strücker	• Design Bugfix
2022-03-16	v.36	Manuela Strücker	• Release 2021.2
2021-05-25	v.35	Manuela Strücker	• Document Style update
2021-05-12	v.34	John Hartfiel	• update board files

2021-02-05	v.33	John Hartfiel	• Release 2020.2 • Document Style update
2021-02-05	v.31	John Hartfiel	• new assembly variants
2020-03-25	v.28	John Hartfiel	• script update
2020-01-27	v.27	John Hartfiel	• documentation update
2020-01-22	v.26	John Hartfiel	• new assembly variants • Release 2019.2
2019-08-09	v.24	John Hartfiel	• new assembly variants • small document style update
2019-05-07	v.22	John Hartfiel	• Release 2018.3
2018-07-11	v.21	John Hartfiel	• Release 2018.2
2018-03-29	v.20	John Hartfiel	• new assembly variant
2018-02-08	v.19	John Hartfiel	• Release 2017.4
2017-12-20	v.14	John Hartfiel	• Design Update • typo correction on documentation
2017-11-22	v.10	John Hartfiel	• Update assembly versions with new Flash size • Update HW Table Name • Update Design
2017-11-14	v.6	John Hartfiel	• Release 2017.2
--	all		--

Error rendering macro 'page-info'

Ambiguous method overloading for method jdk.proxy241.$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page]

due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.

		atlassian . confluence.core. ContentEntityObject]	

Document change history.

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