AVN-20220506 4 x 5 modules controller IOs redefinition and CPLD updates

It serves as a preview of the planned updates of the CPLD firmware and the change/expansion of the controller signals of the 4 x 5 modules. This document will be continuously updated until all 4 x 5 modules have been revised.

Last change:

Error rendering macro 'page-info'

Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]

Company	Trenz Electronic GmbH
AVN Number	AVN-20220506
Title	AVN-20220506 4 x 5 modules controller IOs redefinition
Subject	Information about 4 x 5 module controller IO rework
Issue Date	2022-05-06

Products Affected

This change affects all Trenz Electronic 4 x 5 SOM and Carriers*.

Affected Product	Effected Changes	Status*	CPLD	Change Log current development state	Link to current firmware description
TEM0007	#1,#2,#3,#4	Released	LCMXO2-256HC	• JTAG timing correction • Port names according to PCB REV01 schemaic • SC_PGOOD,NOSEQ ports set as inout and pull up ports • Debouncer added • Power sequencing added with three counters to delay between states • SC_PGOOD depends an PG_ALL and power sequencing state • MR_n as reset output	TEM0007 CPLD
TE0710	#?	Unprocessed	LCMXO2-256HC		TE0710 CPLD

TE0711	#1,#2,#3,#4, #5,#6	Processing	LCMXO2-256HC	• Signals are renamed according to the schematic. • NOSEQ pin is added. • PGOOD(STAT_SC2) pulled up. • JTAG signals timing corrected. • LED function changed • MODE_SC1 is connected to LED • I2C to GPIO slave added • CPLD_REVISION as generic parameter added • NOSEQ_SC4 and STAT_SC2 defined as INOUT • Pulled up or pulled down ports was controlled according to CPLD IO standardization. • UIO and UI_CLK pins defined as I2C pins. But UIO and ULF functions are as before.	TE0711 CPLD

TE0712	#1,#3,#4,#5,#6	Released	LCMXO2-256HC	• Renaming the port signals according to the schematic.
				• Defining and reading CPLD Revision via i2c interface.
				• JTAG signal timing adjustment
				• Adding i2c to gpio ip (i2c_slave.vhd)
				• LEDs functions was changed:
				  ◦ SYSLED1 (green LED) shows the DONE and RESIN and GPIO_output(17) bit state of GPIO_output register.
				  ◦ SYSLED2 (Red LED) shows the state of NOSEQ and MODE pins.
				• PG_SENSE renamed to PG_ALL.
				• PGOOD pulled up.
					TE0712 CPLD

TE0713	#1,#2,#3,#4, #5,#6	Processing	LCMXO2-256HC	• I2C to GPIO added to communicate with FPGA • Signals are renamed adccording to the schematic. • NOSEQ pin added. • CPLD_REVISION as generic parameter added. • PGOOD and NOSEQ pins pulled up. • JTAG signals timing corrected.	TE0713 CPLD
TE0715	#1,#2,#3,#4, #5,#6	Released	LCMXO2-256HC	• Boot mode configuration via hardware (dip switch) and firmware added (Boot mode configuration via linux console) • Pullup or pulldown states of PORT pins was checked. • Adding i2c to gpio ip (i2c_slave.vhd) • Changing oscillator frequency from 12.09 MHZ to 24.18MHZ • PORT signals according to the schematic are renamed. • JTAG time constraint correction • PGOOD pin is used as boot mode selector pin. • VCFG1 (MIO8) pin can be changed by i2cset command. This pin must be grounded by boundary scaning.Refer to the following site :https://support.xilinx.com/s/article/57930?language=en_US	TE0715 CPLD
TE0720	#1,#2,#5,#6,#7 (#4 since CPLD Rev06)	Released	LCMXO2-1200HC	• Added matched functions for WDT Chip BD39040MUF-CE2 • PG_ALL pin pulled up. • User can activate WDT as before. • If no WDT chip on the board, hardware WDT will be switched automatically on software WDT with PL clock input (X6 pin of CPLD and K20 of FPGA). • If no WDT chip on the board, software WDT will work with CR1(14) clock input as before. • If WDT chip on the board, hardware and software WDT work separately with PL input clock (X6 pin) for hardware WDT and CR1(14) as input clock for software WDT. • For software WDT : phytool write eth0/0x1A/7 0xA500 • For hardware WDT : phytool write eth0/0x1A/7 0xB600 • Using CR5[15:14] to save the WDT status ("00" WDT deactive, "01" Hardware WDT, "10" Software WDT, "11" No WDT chip on the board, software WDT with PL clock input) • Using Register4 of mdio_slave_interface to see WDT status via FSBL code (first test in vivado 20.2 and vivado 21.2) or following instruction in linux: phytool read eth0/0x1A/4 • Boot mode configuration via MDIO interface (phytool) • PGOOD pin is used as boot mode selector pin. • NOSEQ pin is used as tristate via i2c interface. • Reseting the FPGA after boot mode configuration • Matched to FSBL code to show all informations while booting in linux console. For example Boot mode, pudc state ... • Monitoring CR4[15:8] and CR5[10] continuously, to implement a state machine for boot mode configuration correctly. • Using CR4[15:12] as control bit to reset FPGA • Using CR4[9:8] as boot mode configuration , if the FPGA is not restarted still via soft reset. • Defining a new input register for mdio_slave_interface (CR5) • Using CR5[9:8] as boot mode configuration, if the FPGA is restarted already via soft reset. • Using CR5[10] to monitor , if the FPGA is restarted already via soft reset. • Using Register4 to read the generic parameters and other parameters via FSBI code or phytool command in linux : Phytool read eth0/0x1A/4 • Using i2c_slave.vhd instead of I2C_to_GPIO.v • Changing Firmware Register MDIO_SL_REGISTER_4_CONTENT to CPLD_REVISION register.	TE0720 CPLD
TE0741	#1,#4,(#5 still in process)	Processing	LCMXO2-256HC	• Added one wire slave and master in code. But it works only , when the clock of master and slave are synchronized. Therefore one wire master and slave is added only in simulation and not in synthesis.	TE0741 CPLD

TE0820	#1,#2,#3,#4, #5,#6	Released	LCMXO2-256HC	• Adding configuration of boot mode in linux console and via generic parameters
				• PGOOD pin used as boot mode selector pin.
				• Adding boot mode configuration via hardware
				• JTAG time constraint correction
				• Adding i2c to gpio ip (i2c_slave.vhd)
				• LED function is changed.
				• New generic parameter defined : PCB_REV
				• EN1 pin
				  ◦ is renamed to RST_EN.
				  ◦ pin is input for PCB_REV=4 and it is enable pin same as before.
				  ◦ is reset output for PCB_REV=5 or newer.
					TE0820 CPLD

TE0821	#1,#2,#3,#4, #5,#6	Processing	LCMXO2-256HC	• Adding configuration of boot mode in linux console and via generic parameters • PGOOD pin used as boot mode selector pin. • Adding boot mode configuration via hardware • JTAG time constraint correcture • Adding I2C to gpio ip (i2c_slave.vhd) • LED function was changed.	TE0821 CPLD
TE0823	#1,#2,#3,#4, #5,#6	Processing	LCMXO2-256HC	• Adding configuration of boot mode in linux console and via generic parameters • PGOOD pin used as boot mode selector pin. • Adding boot mode configuration via hardware • JTAG time constraint correcture • Adding I2C to gpio ip (i2c_slave.vhd) • LED function was changed.	TE0823 CPLD
TE0841	#?	Unprocessed	LCMXO2-256HC		TE0841 CPLD
TE0701	#2, #4	Test phase	LCMXO2-1200HC	• Connecting PGOOD to CM2 to use as boot mode pin selector • JTAG timing correction	TE0701 CPLD
TE0703	#1,#2,#3,#4,#6	Released	LCMXO2-1200HC	• Oscillator frequency is changed from 12.09 MHz to 24.18 MHZ. • Access to CPLD of TE0715 with a generic parameter added. (For optional jed file to access CPLD of TE0715 module) • PGOOD used as second boot mode selector pin and connected to dip switch S2-1. PGOOD and MODE are boot mode selector pins. • S2-1 dip switch (CM1) functionality is changed.In HW PCB REV0 to REV04 is used for SD card detection but in HW PCB REV05 and REV06 is used to set or reset PGOOD. • MIO14 is connected to FTDI_RXD directly without depending on PGOOD. • CM1 (Dip switch S2-2) has no effect on MIO9 anymore. That means MIO9 is connected to SD_CD only and not to SD_CD and CM1.	TE0703 CPLD - CC703S
TE0705	#2, #3, #4	Released	LCMXO2-1200HC	• JTAG timing correction • Renaming ports according to the schematic REV04 • RGPIO is removed. • I2C to GPIO sub system is added for communication between FPGA on the module and CPLD on the carrier board. (MIO10 --> SCL , MIO11 --> SDA) • Access to CPLD chip of TE0715 either via USR0 Dip switch for PCB REV04 or via CM0 and CM1 for PCB REV03 revisions • In PCB REV04 USR0 is used to access to TE0715 CPLD • In PCB REV04 USR1 is used to change NOSEQ signal, if no access to TE0715 CPLD is active (USR0 = OFF) • In PCB REV04 USR2 is used to change PGOOD, if no access to TE0715 CPLD is active (USR0 = OFF) • In PCB REV04 USR3 is used to change JTAGMODE signal of CPLD of module. USR3 = OFF --> Access to FPGA , USR3 = ON --> Access to CPLD of module • In PCB REV03 CM0 and CM1 dip switches are used to access to CPLD of TE0715 or other modules. • Displaying PGOOD and NOSEQ signal states on PHY_LED1/PHY_LED1_A • Displaying state of POK_FMC (power ok signal of EN5335QI PowerSoC) on PHY_LED2/PHY_LED2_A	TE0705 CPLD
TEB2000	#1,#2,#3,#4, #5,#6	Processing	LCMXO2-1200HC	• I2C port added. • I2C to GPIO component added. • NOSEQ can be changed via I2C port. • UART1 port added. This board has two UART ports. (UART0 and UART1) • New construction for UART0 and UART1 serial interfaces • Generic parameter CPLD_REVISION added. • JTAG timing correction • LED states and related ports/signals are changed. --> SD_CD, NOSEQ, MIO0, PGOOD, CM0 and CM1 • New mapping for related ports/signals to GPIO_input and GPIO_output registers • New Ports are defined according to the schematic or revision 1	---
TE0706	#?	HW changes	---	---	---
TEBA0841	#?	HW changes	---	---	---
TEF1002	#?	Unprocessed	10M08		TEF1002 SC CPLD MAX10
TEB0707	#?	Unprocessed	10M08		TEB0707 MAX10 CPLD

*Status:

- No changes: ---
- HW changes: HW changes are need to support new features
- Unprocessed: Revision not started
- Processing: Revision in process
- Test phase: rework finished test phase started
- Released (date): Firmware is released and will be used

Changes

#1 Unification of the IO types

Type: Improvement

Reason: Add possibility for Zynq modules to change boot

Impact: Depends custom carrier realisation. Mostly none.

Standardization:

Name	Module B2B Pin	Carrier B2B Pin	Direction	CPLD Pullup active	Changes
JTAGSEL	JM1-89	JB1-90	in	---	• None
SC_EN1	JM1-28	JB1-27	in	yes	• Depending on module activate weak Pullup
SC_NOSEQ	JM1-7	JB1-8	**inout**	yes	• Depending on module from input or not used to inout. • Depending on module activate weak Pullup on CPLD, in case it's connected to CPLD • Used as Multifunction Pin, in case it's connected to CPLD
SC_PGOOD	JM1-30	JB1-29	**inout**	yes	• Depending on module from output or not used to inout with weak pullup on module • Activate weak Pullup on CPLD, in case it's connected to CPLD • Used as additional Boot Mode Pin on Zynq Modules (input usage) • Used as PGOOD signal (output usage)
SC_BOOTMODE	JM1-32	JB1-31	in	yes	• Depending on module activate weak Pullup

See also 4 x 5 SoM Integration Guide#4x5SoMIntegrationGuide-4x5ModuleControllerIOs

#2 Redefinition of SC_PGOOD

Type: Improvement

Reason: Add possibility for Zynq modules to support more boot modes (mostly QSPI, SD, JTAG). JTAG only boot mode is needed for QSPI Programming with newer Vivado Version. See AR#00002 - QSPI Programming issues

Impact: None.

#3 Redefinition of SC_NOSEQ

Type: Improvement

Reason: Add possibility for to used this pin as multifunction pin. Options depends on the module

Impact: None, as long as this pin was used as module input or bidirectional signal

#4 Add JTAG timing constrains

Type: Improvement

Reason: Add timing constrain to JTAG signal to improve signal quality

Impact: None.

#5 CPLD Firmware Identification

Type: Improvement

Reason: Add possibility to identify CPLD Firmware via FPGA. Interface depends on module (I2C, MDIO,...)

Impact: None.

#6 Additional features

Type: Improvement

Reason: Add new module depended features to the CPLD functionality, see CPLD description

Impact: None.

#7 Bugfix

Type: Bugfix

Reason: Fixed some insignificant bugs, see CPLD description

Impact: None.

Method of Identification

Depending on Module series, new feature to read CPLD Firmware version was added.

Contact Information

If you have any questions related to this AVN, please contact Trenz Electronics Technical Support at

- forum.trenz-electronic.de
- wiki.trenz-electronic.de
- support%trenz-electronic.de (subject = AVN-20220506)
- phone
    - national calls: 05741 3200-0
    - international calls: 0049 5741 3200-0

Disclaimer

Any projected dates in this AVN are based on the most current product information at the time this AVN is being issued, but they may change due to unforeseen circumstances. For the latest schedule and any other information, please contact your local Trenz Electronic sales office, technical support or local distributor.

This AVN follows JEDEC Standard J-STD-046.