OZOM-A: Frequency Counter

Preface

Making a frequency counter is nothing fancy? Yes, but how about to create specialized frequency counter hardware with say up to 16 channels with max input clock rate >= 800MHz within 10 minutes? And verify this software defined hardware in the next 20? And implement this on open source software defined hardware platform?

Step 1:

Step X:



We have added a frequency Counter IP and connected it to our test signal sources and to Vivado labtools VIO (Virtual Input Output).

Step Z:



Result: it works from idea to result no trial and error, no just do it, try it out and it just works. This was the very first project on the open source software define hardware OZoM Model-A.

There are 12 frequency measurement channels implemented, connected to ZYNQ Fabric Clock, to both Zynq PS Timer wavegen outputs (no frequency as those timers are not initialized) and to two Clock Manager MMCM that generates two clocks.

So our frequency meter displays the measured frequency of an 800MHz signal. Using hardware that did not exist in 30 minutes ago. Hardware that anyone anywhere can load into the "software defined hardware".

🖵 Re-customize IP		N			X								
ZYNQ7 Processing System (5.5)													
🎁 Documentation 🍓 Presets 🛅 IP Location 🍓 Import XPS Settings													
Page Navigator Clock Configuration Summary Report													
Zynq Block Design	Basic Clocking Advanced Clocking												
PS-PL Configuration	← Input Frequency (MHz) 33.333333 CPU Clock Ratio 6:2:1 ▲ Search: Q.												
Peripheral I/O Pins													
MIO Configuration	😝 Component	Clock Source	Requested Frequen	Actual Frequency(M	Range(MHz)								
Clock Configuration	Processor/Memory Clocks IO Peripheral Clocks												
DDR Configuration :		IO PLL 🔻	100	100.000000	0.100000:250.000000								
SMC Timing Calculation		IO PLL 🔻	200 📀	200.000000	0.100000 : 250.000000								
Interrupts	FCLK_CLK2	IO PLL 🔻	33.333333 🛞	33.333336	0.100000:250.000000								
	FCLK_CLK3	IO PLL 👻	1.024 🙁	1.023018	0.100000:250.000000								
	÷ System Debug Clocks ⊕ Timers												
					OK Cancel								

Those are the Fabric clocks generated by the Zynq PS subsystem, all of them are measured correctly.

🗜 Re-customize IP		2							X				
Clocking Wizard (5.1)													
Documentation 📄 IP Location													
IP Symbol Resource		Component Name clk	_wiz_0										
Show disabled ports		de dires De l'esse	Output Charles	-		Dent Den		(
	^ I		Output Clocks	M	MCM Settings	Port Rena	aming	Summary					
		The phase is calculated relative to the active input dock.											
		Output Clock	Output Freq (MHz) Requested Actua		Actual	Phase (de Requeste		e (degrees) ested	degrees) ted Actual				
		✓ ck_out1	100.000	0	100.000	0.000		8	0.000				
clk_out1		Ck_out2	800	0	800.000	0.000.00		8	0.000				
-ck_hi ck_outz-		Ck_out3	33.3	8	33.333		0.000	8	0.000				
locked -		ck_out4	100.000		N/A		0.000		N/A				
		clk_out5	100.000		N/A		0.000		N/A				
		clk_out6	100.000		N/A.		0.000		N/A				
		clk_out7	100.000		N/A		0.000		N/A				
•	• •	•	III										
								ОК	Cancel				

Two additional clocks generated by the Clock Manager in the Zynq PL are also correctly measured.

But is the clock really 800MHz? Lets try to measure it with some other methods!



Measurement setup 1: OZoM-A is powered from lab supply, power consumption 0.76W, 800MHz clock is connected to signal in the header, Signal hound with air-loop is used to measure the frequency.



Here it is the generated 800MHz signal has been measured to be really 800MHz. Well but maybe this is harmonic and not the signal itself?



Here is more proof that there really was a 800MHz signal that we measured.