TE0630 Known Issues

Possible race condition during power up

S1B and S1A both set to ON can lead to a race condition. When Bitgen option "reset_on_error" is not set, the module does not boot.

Explanation

When S1B switch is ON, FPGA and FX2 start at the same time and as S1A is also ON, FX2 runs custom firmware which initializes SPI and trying to switch ON FPGA power (which is already forced to ON by S1B). So FX2 create error during FPGA load. As "reset_on_error" is not set FPGA will not try to boot again.

Solutions

1. If you don't use our USB API, switch S1A to OFF (S1B to ON). This way you disable FX2 activity on SPI bus and FPGA will boot from SPI by power on. (Fastest boot)

2. If you need USB API.

- Switch S1B to OFF (S1A to ON). This way FX2 firmware will control FPGA power and FPGA will be powered up and start boot only after full FX2 initialization.
- Enable "reset_on_error" option for bootstream generation. This way, even if S1B is on and FX2 SPI init and FPGA boot will be in the same time (and bitstream will be corrupted during transfer by SPI) FPGA will reboot again if error occur.

Init and boot time depend on board capacitance and power supply so may vary from board to board, which affect to boot behavior.