Vivado Board Part Flow

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Definition

TE Board Part Files

Usage

TE reference design scripts provide all necessary steps for a local board part installation and PS-Initialization. Reference Designs provide additional informations and instructions

General sescription of the reference design project delivery:

- Project Delivery #QuickStart
- Project Delivery #Initialise TE-scripts on Vivado/LabTools
- Project Delivery #Block Design Conventions

For manual Initialization use following description.

Installation

Overview

The Vivado® Design Suite allows you to create projects based on specific boards. Trenz Electronic provides Vivado Board Part files in the download area. This files are included into the reference projects, please choose a reference design under the proper module.

There are three options for installing the Board Part files

- Option1: Use Trenz Electronic Reference Design with local board part file
- Option2: Xilinx Git Hub for Vivado
- Option3: Install into a User Repository
- Option4: Install into the Vivado installation

Attention: The board part files of our reference designs are for the corresponding Vivado version of the project delivery. It's possible to use them with other Vivado versions, but maybe it's not working correctly, if this is done.

Option 1: Use Trenz Electronic Reference Design with local board part file

Trenz Electronic will provide board part files for new assembly variants at first with the latest reference designs version.

- Since 2018.3 special "Module Selection Guide" is included into "_create_win_setup.cmd" and "_create_linux_setup.sh"
- These board part file will be set for the local project, if the project is generated with the provided scripts from the project delivery. More information on: Project Delivery AMD devices
- A overview page of the latest reference designs and links to the documentation and downloads are available on: TE Reference Designs Overview#Overview
- 1. Download the reference design from the corresponding download area of the Trenz Electronic Product
- 2. Since 2018.3 special "Module Selection Guide" is included into "_create_win_setup.cmd" and "_create_linux_setup.sh"
- 3. Unzip download (use short directory name)

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- 4. Execute "_create_win_setup.cmd" or "_create_linux_setup.sh" (depending on the used OS)
- 5. Follow instruction on the console window
 - a. (optional) Select Vivado Installation path and Version (will be possible in the expected version wasn't found on Xilinx installation path)
 b. Console will show a list of available assembly versions (board files) for the reference design:

ID Product ID	SoC/FPGA Typ	SHORT DIR	PCB REV	DOR Size	Flash Siz	e ENMC Size	Others	Notes
54 TE0803-03-48E21-L	xczu4eg-sfvc784-1-e	4eg_4gb	REV03	4GB	12818	NA	1 mm connectors	NA
56 TE0803-03-4BI21-A	xczu4eg-sfvc784-1-i	4eg_1_4gb	REV03	4GB	128HB	NA	NA	NA
60 TE0803-03-4DE21-L	xczu4ev-sfvc784-1-e	4ev_4gb	REV03	4GB	128MB	INA	1 mm connectors	NA
62 TE0803-03-4GE21-L	xczu4eg-sfvc784-2-e	4eg_2_4gb	REV03	4GB	128MB	NA	1 mm connectors	NA I
66 TE0803-03-5DI21-A		Sev_i_4gb	REV03		128MB			
68 TE0803-03-3RI21-A	xczu3eg-sfvc784-1L-i	3eg_li_4gb	REV03	4GB	128MB	NA	NA	NA I
70 TE0803-03-38I21-A	xczu3eg-sfvc784-1-i	3eg_i_4gb	REV03	4GB	128MB	INA	NA	NA
72 TE0803-03-4DI21-L	xczu4ev-sfvc784-1-1	4ev_i_4gb	REV03	4GB	128MB	NA	1 mm connectors	NA
78 TE0803-03-4GI21-A	xczu4eg-sfvc784-2-i	4eg_2i_4gb	REV03		128MB			
82 TE0803-03-5DI24-A	xczu5ev-sfvc784-1-1	Sev_i_4gb	REV03	4GB	512MB	NA	NA	NA
84 TE0803-03-48I21-X	xczu4eg-sfvc784-1-i	4eg_i_4gb	REV03		12818			U41 replaced with diode
86 TE0803-03-38E21-A	xczu3eg-sfvc784-1-e	3eg_4gb	REV03		128MB			
Last Input:ddr> Meta: Input:ddr> Meta: Input:ddr Step 2: Insert DOR Size 4 Sector 2: Insert DOR Size 4 Sector 2: Insert DOR Size 5 Sector 2: Insert DOR Size 5 Sector 2: Insert DOR Size 5 Sector 2: Insert DOR Size 5 Sector 2: Insert Size 5 Sector	and with list elements, wildca 'g or 'g' then is 2 steps: little): little; press it or 'l' st, press it or 'l' st, press it or 'l' method press it of the 's' press: 'press' or 'free' store of the 's' store of the 's'							

c. Select ID number to select the board or use filter function to reduce the table with one of the other categories from the table header d. Verify selection and create project

Option 2: Xilinx Git Hub for Vivado (not recommended at the moment, git hub is currently not up to date)

A Board Files for Trenz Electronic Modules will be available on Xilinx Git Hub store for Vivado 2020.1 and newer

Trenz Electronic will update board files which are available the Github regularly, but latest board part files tested with the corresponding Vivado version will be still delivered first with the reference designs.

Xilinx Git Hub Link: https://github.com/Xilinx/XilinxBoardStore

1. Open Vivado

2. Select download path for Git Hub Store (got to Tools Settings):

2.	XHub Store
Tool Settings	Configure download location and proxy for XHub store.
Project	
IP Defaults	
V XHub Store	Contigure Download Location
Board Repository	Download location: S:/xilinx/vivado/2020.1/xhub 🚳 ···
Example Project Repository	
Source File	Configure Proxy
Display	No proxy
WebTalk	Manual proxy configuration
Help	
> Text Editor	Host Name: proxys g
3rd Party Simulators	
> Colors	Port: 8,080 -
Selection Rules	✓

3. Open XHub Store and select "Boards" Tab

e Flow Tools Window Help			
	À XiHub Stores		:
HLx Editions	Welcome to XHub Stores. You can browse and search the available applicatio	is and install to your local drive.	4
Quick Start	Id Apps Boards Example Designs		<u>G</u> o to Git
Quick Start		Details	
	Q.	Name: UltraSOM (ZYNQ-UltraScale+) TE0803-*-3AE10-A (2GB DDR) with TEB	F0808. * SPRT PCB: REV03
	Collinx Construction of CombH Construction of CombH Construction of CombH	Description: Zynq UltraScale+ TE0803-*-3AE10-A(2GB DDR) Board (form factor 5 2x DDR4, speed grade -1 and extended temperature range. "Supported P REVID SEPU2 REVID Reard Path for usage with carechard TERE	7.6 cm) with 4x 512 MByte CB Revisions: IRNR
	> E Kintex-7	Revision: 6.0	
	> 🗁 Kintex UltraScale	Revision History	
	> 🗁 Zyng UltraScale+	URL: https://github.com//ulinx/blinxBoardStore/tree/2020.1/boards/Trenz_Ele	ctronic/TE0803_3CG_1E/6.0
lasks	> 🗁 ZYNQ-7	Company: Trenz Electronic GmbH	
Manage ID >	> = ZYNQ-75		
Open Hardware Manager	> Digitant Inc		
XHub Stores >	> 🖾 Avnet		
Learning Center			
Documentation and Tutorials > Quick Take Videos >			
Release Notes Guide >			
	Refresh Catalog was last updated on 09/07/2020 5/49:24 PM	¢	Close



5. Installed Board files will be marked with the green check mark.

Option 3: Install into a User Repository

This Option allows you to install the Vivado Board Part files to any location of your choosing. The disadvantage is that it required an additional command to point the tools to your repository.

```
This description is for Vivado 2015.1 and higher. Older Vivado versions used other variable names, so some changes are necessary.
Since Vivado 2017.1, "init.tcl" should be renamed to "Vivado_init.tcl"
1. Create init.tcl with following content:
```

2. Put init.tcl in one of the possible locations for init.tcl:

```
a. Vivado Project (For current version only): <installdir>/vivado/<version>/scripts/
```

- b. User Data(For all versions): C:/Users/<user>/AppData/Roaming/Xilinx/Vivado/
- Copy the Board part files folder from the reference project (<reference_design>/board_files/) into the folder C:/TE (the folder location can be changed in the init.tcl script). The *.csv file from <reference_design>/board_files/ is not necessary for this way.

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4. Start your Vivado Version and the TCL-console printout should be the following:

Vivado 2015.4	- 🗆 🗙
<u>F</u> ile Flow <u>T</u> ools <u>Window H</u> elp	Q- Search commands
Productivity. Multiplied.	E XILINX All programmable.
Quick Start	A Recent Projects
Create New Project Open Project Open Example Project	test_memory B:/SVN/cores/2015.4/design/TE0841/test_memory ibert_Jseries_gtx_0_example b:/SVN/cores/2015.4/design/TE0741/si/bert_7se z-turn_templ S:/tmp/z-turn_templ
Tasks	s:/tmp/zc702/vivado
Manage IP Open Hardware Manager Xilimx Td Store	hdmii-hdmio s;/tmp/sdsoc/te20_2i/hdmii-hdmio/vivado pde_eyescan B;/SVN/cores/2015.4/design/TE0712/stapp1198/ pde_eyescan B;/SVN/cores/2015.4/design/TE0712/pde_eyesca test_board B;/SVN/cores/2015.4/design/TE0712/test_board/
🧳 🎉 🏹	pcie_7x_0_example B:/SVN/cores/2015.4/design/TE0712/test_pciest pcie_evescan
Documentation and Tutorials Quick Take Videos Release Notes Guide	B:/SVN/cores/2015.4/design/TEC0725/xapp1198
Td Console	_ 🗆 🖻 ×
Sourcing tcl script 'C:/Xilinx/Vivado/2015.4/scripts/init.tcl' Set Board Part RepoPath: C:/TE start_gui	· · · · · · · · · · · · · · · · · · ·
Type a Tcl command here	

A Please make sure you use plain ASCII text editor when creating the init.tcl file, any non ASCII character in the file will make Vivado to freeze on startup.

A working init.tcl file is provided in the archive with this tutorial. With this method you can set up a permanent initialization TCL that is read by Vivado each time it launches. Details about the init.tcl file are included in UG835 Vivado Design Suite Tcl Command Reference Guide. UG835 describes where to put the init.tcl file.

Option 4: Install into the Vivado installation

This is the quickest option, but it is not recommended by Xilinx. Use at your own risk.

1. Copy the Board part files folder from the reference project (<reference_design>/board_files/) into the folder <*installdir*>/vivado/<version>/data /boards/board_files/. Create this folder if it does not exist yet. The *.csv file from <reference_design>/board_files/ is not necessary for this way.

Load on Vivado

Regardless of which method you choose, the new boards should now be visible in Vivado 2015.1 or higher for vendor trenz.biz. To test this out, do the following.

- 1. Launch Vivado.
- 2. Select Create New Project.
- 3. Click Next> to get started.
- 4. Set the project name and location. Press Next>.
- Select project hame and locate
 Select project type Click Next>.
 At the Default Part screen, a, Click Boards under Specify.

- b, Click trenz.biz under Vendor.

The options should appear as shown.

æ			New Project				×
Default Part Choose a defaul	t Xilinx part or board for your	project. This o	can be changed lat	er.			
Select: Parts	📓 Boards						
Ve <u>n</u> dor:	trenz.biz	Ŧ					
Display <u>N</u> ame:	All Remaining	-					
Board Rev:	All	-					
_			Reset All Filter				
Search: Q-		Vandar	Reard Day	Dart	I/O Dia Caunt	File Version	Ava
Display Name		venuor	board Rev	Part	1/O Pin Count	File version	IOB
📓 Artix-7 TE0710 A	15T	trenz.biz	0.2	xc7a15tcsg324-2	324	1.0	210 🔺
Artix-7 TE0710 A	35T	trenz.biz	0.2	xc7a35tcsg324-2	324	1.01	210
Artix-7 TE0710 A	50T	trenz.biz	0.2	xc7a50tcsg324-2	324	1.02	210
Artix-7 TE0710 A	75T	trenz.biz	0.2	xc7a75tcsg324-2	324	1.03	210
Artix-7 TE0710 A	100T	trenz.biz	0.2	xc7a100tcsg324-2	324	1.04	210 🗸
<							> 🗆
				< <u>B</u> ack <u>N</u> ext	: > <u>F</u> inis	h C	ancel

For more information about this capability, please refer to the following Quick Take video.

• http://www.xilinx.com/training/vivado/using-vivado-with-xilinx-evaluation-boards.htm

Software Requirements

The software used is

- Xilinx Vivado 2015.4 or higher (for install option 1, 3, 4)
 Xilinx Vivado 2019.1.3 or higher (for install option 1, 2, 3, 4)

Zynq PS-Initialization (7Series/UltraScale+)

- Install Board Parts, see: Board Part Installation
 Create Project with Board Part

r, search, and browse parts by their resources. The selection will be app	lied.					
arts <mark>Boards -</mark>						
eset <u>A</u> ll Filters						
ndor: trenz.biz v Name: All R	emaining			✓ Board Re	ev: All	
earch: Q- V						
isplay Name	Preview	Vendor	File Version	Part	I/O Pin Count	Board R
litraSOM (ZYNQ-UltraScale+) TE0808-*-BBE21-(A,L)/-15EG-1(E,B) 4GB DDR). *SPRT PCB: REV05, REV04.		trenz.biz	3.0	xczu15eg-ffvc900-1-e	900	0.4
ItraSOM (ZYNQ-UItraScale+) TE0808-*-BBE21-(AL)/-15EG-1E(E,B) 4GB DDR) with TEBF0808. *SPRT Module PCB: REV05, REV04.		trenz.biz	4.0	xczu15eg-ffvc900-1-e	900	0.4
lltraSOM (ZYNQ-UltraScale+) E0808-*-6BE21-(A,L)/-6EG-1E(E,3) 4GB DDR). *SPRT PCB: REV05, REV04.		trenz biz	3.0	xczu6eg-ffvc900-1-e	900	0.4
ItraSOM (ZYNQ-UltraScale+) TE0808-*-6BE21-(A,L)-6EG-1E(E,3) 4GB DDR) with TEBF0808. *SPRT Module PCB: REV05, REV04.		trenz.biz	4.0	xczu6eg-ffvc900-1-e	900	0.4
IltraSOM (ZYNQ-UltraScale+) TE0808-*-6Bl21-(A,X,D) 4GB DDR), *SPRT PCB: REV05,REV04.		trenz.biz	3.0	xczu6eg-ffvc900-1-i	900	0.4
IltraSOM (ZYNQ-UltraScale+) TE0808-*-6Bi41-X 3GB DDR). *SPRT PCB: REV05.		trenz.biz	5.0	xczu6eg-ffvc900-1-i	900	0.5
IltraSOM (ZYNQ-UltraScale+) TE0808-*-6Bl21-(A,X,D) 4CB DDR) with TERE0808 *SPET Module PCB: REV05 REV04		trenz biz	4.0	xczu6eo-ffvc900-1-i	900	0.4

3. Create Block-Design and add Zynq-Processing System



4. Run Block Automation

Q	Description
 All Automation (1 out of 1 selected) Transformed and the selected of the selected of	This option sets the board preset on the Processing System. All current properties will be overwritten by the board preset. This action cannot be undone.
	NOTE: Apply Board Preset will discard existing IP configuration - please uncheck this box, if you wish to retain previous configuration. Instance: /zynq_uttra_ps_e_0
	Options
	Apply Board Preset: 🧭
•	OK
S configuration is finished w	ith basic Settings:
agram × Address Editor × Đ, O, IX, IX, I⊕ Q, IX, I⊕ +	× ୬ ଏ ≯ C ଏ = Default View ✓
ļ	zyng_ultra_ps_e_0 M_AXI_HPM0_LPD + CAN_0 +
	rs_and, ack ap_s_ads_audo_ack ap_s_ads_audo_ack pads_aud_data_in phd_plug_detect UltraSCALE+
	Zynq UltraScale+ MPSoC

 6. (optional)Some Reference Design contains local extensions for some carrier depended configuration, located in the subfolder <board_parts>/. These Scripts must be source manually on the TCL-Console after "Block-Design Automation"