TE0717 Test Board

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Overview

Refer to https://wiki.trenz.org/te0717-info for the current online version of this manual and other available documentation.

This example shows a simple MicroBlaze Design that executes in an endless loop letting the red LED blink and prints "Hello Trenz Module TE0717" via UART for 10 minutes.

Key Features

- Vitis/Vivado 2021.2
- MicroBlaze
- UART
- QSPI Flash
- HyperRAM
- SPI ELF Bootloader

Revision History

Date	Vivado	Project Built	Authors	Description
2022-06-20	2021.2	TE0717-test_board_noprebuilt-vivado_2021.2-build_14_20220628114204.zip TE0717-test_board-vivado_2021.2-build_14_20220628114204.zip	Waldemar Hanemann	• initial release

Design Revision History

Release Notes and Know Issues

Issues	Description	Workaround	To be fixed version
No known issues		---	---

Known Issues

Requirements

Software

Software	Version	Note
Vitis	2021.2	needed, Vivado is included into Vitis installation

Software

Hardware

Basic description of TE Board Part Files is available on TE Board Part Files.

Complete List is available on "<project folder>\board_files*_board_files.csv"

Design supports following modules:

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMMC	Others	Notes
TE0717-01-P1C-5-A	01_100_1C_8MB	REV01	Hyperram 8MB	8MB	---	---	

*used as reference

Hardware Modules

Design supports following carriers:

Carrier Model	Notes
TEB0717	

*used as reference

Hardware Carrier

Additional HW Requirements:

Additional Hardware	Notes
USB Cable for JTAG/UART	Check Carrier Board and Programmer for correct type
XMOD Programmer	Carrier Board dependent, only if carrier has no own FTDI

*used as reference

Additional Hardware

Content

For general structure and usage of the reference design, see Project Delivery - AMD devices

Design Sources

Type	Location	Notes
Vivado	<project folder>\block_design <project folder>\constraints <project folder>\ip_lib <project folder>\board_files	Vivado Project will be generated by TE Scripts
Vitis	<project folder>\sw_lib	Additional Software Template for Vitis and apps_list.csv with settings automatically for Vitis app generation

Design sources

Additional Sources

Type	Location	Notes

Additional design sources

Prebuilt

File	File-Extension	Description
BIT-File	*.bit	FPGA (PL Part) Configuration File
DebugProbes-File	*.ltx	Definition File for Vivado/Vivado Labtools Debugging Interface
Hardware-Platform-Description-File	*.xsa	Exported Vivado hardware description file for Vitis and PetaLinux
LabTools Project-File	*.lpr	Vivado Labtools Project File
MCS-File	*.mcs	Flash Configuration File with Boot-Image (MicroBlaze or FPGA part only)
MMI-File	*.mmi	File with BRAM-Location to generate MCS or BIT-File with *.elf content (MicroBlaze only)
Software-Application-File	*.elf	Software Application for Zynq or MicroBlaze Processor Systems

Prebuilt files (only on ZIP with prebuilt content)

Download

Reference Design is only usable with the specified Vivado/Vitis/PetaLinux version. Do never use different Versions of Xilinx Software for the same Project.

Reference Design is available on:

- TE0717 "Test Board" Reference Design

Design Flow

> ⚠ Reference Design is available with and without prebuilt files. It's recommended to use TE prebuilt files for first launch.

Trenz Electronic provides a tcl based built environment based on Xilinx Design Flow.

See also:

- Xilinx Development Tools#XilinxSoftware-BasicUserGuides
- Vivado Projects - TE Reference Design
- Project Delivery.

The Trenz Electronic FPGA Reference Designs are TCL-script based project. Command files for execution will be generated with "_create_win_setup.cmd" on Windows OS and "_create_linux_setup.sh" on Linux OS.

TE Scripts are only needed to generate the vivado project, all other additional steps are optional and can also executed by Xilinx Vivado/Vitis GUI. For currently Scripts limitations on Win and Linux OS see: Project Delivery Currently limitations of functionality

> **Caution!** Win OS has a 260 character limit for path lengths which can affect the Vivado tools. To avoid this issue, use Virtual Drive or the shortest possible names and directory locations for the reference design (for example "x:\<project folder>")

1. Run _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell:

_create_win_setup.cmd/_create_linux_setup.sh

```
------------------------Set design paths----------------------------
-- Run Design with: _create_win_setup
-- Use Design Path: <absolute project path>
------------------------------------------------------------------
-------------------------TE Reference
Design---------------------------
------------------------------------------------------------------
-- (0)  Module selection guide, project creation...prebuilt export...
-- (1)  Create minimum setup of CMD-Files and exit Batch
-- (2)  Create maximum setup of CMD-Files and exit Batch
-- (3)  (internal only) Dev
-- (4)  (internal only) Prod
-- (c)  Go to CMD-File Generation (Manual setup)
-- (d)  Go to Documentation (Web Documentation)
-- (g)  Install Board Files from Xilinx Board Store (beta)
-- (a)  Start design with unsupported Vivado Version (beta)
-- (x)  Exit Batch (nothing is done!)
----
Select (ex.:'0' for module selection guide):
```

2. Press 0 and enter to start "Module Selection Guide"
3. Create project and follow instructions of the product selection guide, settings file will be configured automatically during this process.
   - optional for manual changes: Select correct device and Xilinx install path on "design_basic_settings.cmd" and create Vivado project with "vivado_create_project_guimode.cmd"

     > Note: Select correct one, see also Vivado Board Part Flow

4. Create hardware description file (.xsa file) and export to prebuilt folder

run on Vivado TCL (Script generates design and export files into "<project folder>\prebuilt\hardware\<short name>")

```
TE::hw_build_design -export_prebuilt
```

> Using Vivado GUI is the same, except file export to prebuilt folder.

5. Generate Programming Files with Vitis
   a. Run on Vivado TCL:

Script generates applications and bootable files, which are defined in "sw_lib\apps_list.csv"

```
TE::sw_run_vitis -all
```

b. Copy "\prebuilt\software\<short name>\hello_te0717.elf" into "\firmware\microblaze_0\"
c. Regenerate Vivado Project or Update Bitfile only, with new "hello_te0717.elf"

> TCL scripts generate also platform project, this must be done manually in case GUI is used. See Vitis

Launch

Programming

> Check Module and Carrier TRMs for proper HW configuration before you try any design.
>
> Reference Design is also available with prebuilt files. It's recommended to use TE prebuilt files for first launch.

Xilinx documentation for programming and debugging: Vivado/Vitis/SDSoC-Xilinx Software Programming and Debugging

Get prebuilt boot binaries

1. Run _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell
2. Press 0 and enter to start "Module Selection Guide"
    a. Select assembly version
    b. Validate selection
    c. Select create and open delivery binary folder

> Note: Folder "<project folder>_binaries_<Article Name>" with subfolder "boot_<app name>" for different applications will be generated

QSPI-Boot mode

1. Connect JTAG and power on carrier with module
2. Open Vivado Project with "vivado_open_existing_project_guimode.cmd" or if not created, create with "vivado_create_project_guimode.cmd"

run on Vivado TCL (Script programs .mcs-File on QSPI flash)

```
TE::pr_program_flash -swapp hello_te0717
```

3. Press the reset button to start the application and see the output in the console

JTAG

1. Connect JTAG and power on PCB
2. Open Vivado HW Manager
3. Program FPGA with Bitfile from "prebuilt\hardware\<short dir>\"

Usage

1. Prepare HW like described on section Programming
2. Connect UART USB (most cases same as JTAG)
3. Select QSPI as Boot Mode

> Note: See TRM of the Carrier, which is used.

4. Power On PCB

   1. FPGA Loads Bitfile(spi bootloader included) from Flash

   2. The spi bootloader loads the hello_te0717.elf application from address 0x005e0000 to RAM

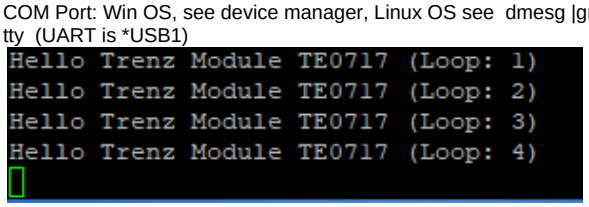
   3. Hello Trenz will be run on UART console for 10 minutes.

   info: Do not reboot, if Bitfile programming over JTAG is used as programming method.

   a. ## UART

      Open Serial Console (e.g. putty)

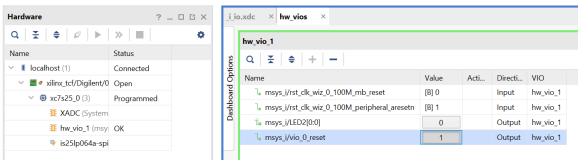
      i. Speed: 9600
      ii. COM Port: Win OS, see device manager, Linux OS see dmesg |grep tty (UART is *USB1)



Vivado HW Manager

Open Vivado HW-Manager and add VIO signal to dashboard (*.ltx located on prebuilt folder)

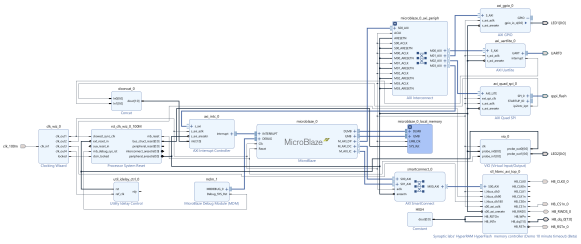
- Control:
  - LED2 (green LED)
  - reset MicroBlaze (active low)
- Monitoring:
  - Reset of Periphery and MicroBlaze



Vivado Hardware Manager

System Design - Vivado

Block Design



Block Design

Constraints

Basic module constraints

_i_bitgen_common.xdc

```
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property BITSTREAM.CONFIG.CONFIGRATE 66 [current_design]
set_property CONFIG_VOLTAGE 3.3 [current_design]
set_property CFGBVS VCCO [current_design]
set_property CONFIG_MODE SPIx4 [current_design]
set_property BITSTREAM.CONFIG.SPI_32BIT_ADDR YES [current_design]
set_property BITSTREAM.CONFIG.SPI_BUSWIDTH 4 [current_design]
set_property BITSTREAM.CONFIG.M1PIN PULLNONE [current_design]
set_property BITSTREAM.CONFIG.M2PIN PULLNONE [current_design]
set_property BITSTREAM.CONFIG.M0PIN PULLNONE [current_design]

set_property BITSTREAM.CONFIG.USR_ACCESS TIMESTAMP [current_design]
```

_i_bitgen.xdc

```
set_property BITSTREAM.CONFIG.UNUSEDPIN PULLDOWN [current_design]
#
#
#
```

Design specific constraints

_i_io.xdc

```
set_property PACKAGE_PIN G11 [get_ports clk_100m]
set_property IOSTANDARD LVCMOS33 [get_ports clk_100m]

set_property IOSTANDARD LVCMOS33 [get_ports {LED1[0]}]
set_property IOSTANDARD LVCMOS33 [get_ports {LED2[0]}]
set_property PACKAGE_PIN D14 [get_ports {LED1[0]}]
set_property PACKAGE_PIN C14 [get_ports {LED2[0]}]
```

_i_hyperram.xdc

```
set_property PACKAGE_PIN F13 [get_ports HB_CLK0_0]
#set_property PACKAGE_PIN A14 [get_ports HB_CLK0n_0]

set_property PACKAGE_PIN A13 [get_ports {HB_dq_0[0]}]
set_property PACKAGE_PIN B13 [get_ports {HB_dq_0[1]}]
set_property PACKAGE_PIN D12 [get_ports {HB_dq_0[2]}]
set_property PACKAGE_PIN D13 [get_ports {HB_dq_0[3]}]
set_property PACKAGE_PIN A12 [get_ports {HB_dq_0[4]}]
set_property PACKAGE_PIN G14 [get_ports {HB_dq_0[5]}]
set_property PACKAGE_PIN F14 [get_ports {HB_dq_0[6]}]
set_property PACKAGE_PIN B14 [get_ports {HB_dq_0[7]}]


set_property PACKAGE_PIN E13 [get_ports HB_RWDS_0]

set_property PACKAGE_PIN E12 [get_ports HB_CS1n_0]
set_property PACKAGE_PIN F12 [get_ports HB_RSTn_0]

#set_property PACKAGE_PIN A18 [get_ports HB_CS0n_0 ]
#set_property PACKAGE_PIN J18 [get_ports HB_INTn_0 ]
#set_property PACKAGE_PIN C17 [get_ports HB_RSTOn_0]


#
# FPGA Pin Voltage assignment
#
set_property IOSTANDARD LVCMOS33 [get_ports HB_CLK0_0]
#set_property IOSTANDARD LVCMOS33 [get_ports HB_CLK0n_0]
set_property IOSTANDARD LVCMOS33 [get_ports {HB_dq_0[*]}]
set_property IOSTANDARD LVCMOS33 [get_ports HB_CS1n_0]
set_property IOSTANDARD LVCMOS33 [get_ports HB_RSTn_0]
set_property IOSTANDARD LVCMOS33 [get_ports HB_RWDS_0]

#set_property IOSTANDARD LVCMOS18 [get_ports HB_CS0n_0]
#set_property IOSTANDARD LVCMOS18 [get_ports HB_INTn_0]
#set_property IOSTANDARD LVCMOS18 [get_ports HB_RSTOn_0]

#set_property PULLUP true [get_ports HB_RSTOn_0]
#set_property PULLUP true [get_ports HB_INTn_0]

#
#Hyperbus Clock - change according to clk pin on PLL
#
#create_generated_clock -name clk_0   -source [get_pins msys_i/clk_wiz_0
/inst/mmcm_adv_inst/CLKIN1] -master_clock clk_100m [get_pins msys_i
```

```
/clk_wiz_0/inst/mmcm_adv_inst/CLKOUT0]
#create_generated_clock -name clk_90  -source [get_pins msys_i/clk_wiz_0
/inst/mmcm_adv_inst/CLKIN1] -master_clock clk_100m [get_pins msys_i
/clk_wiz_0/inst/mmcm_adv_inst/CLKOUT1]
#create_generated_clock -name clk_180 -source [get_pins msys_i/clk_wiz_0
/inst/mmcm_adv_inst/CLKIN1] -master_clock clk_100m [get_pins msys_i
/clk_wiz_0/inst/mmcm_adv_inst/CLKOUT2]

#
#100Mhz clock freqeuncy - change accordingly
#
set hbus_freq_ns   10

set dqs_in_min_dly -0.5
set dqs_in_max_dly  0.5

set HB_dq_ports    [get_ports HB_dq_0[*]]

#
#Create RDS clock and RDS virtual clock
#
create_clock -period $hbus_freq_ns -name rwds_clk      [get_ports
HB_RWDS_0]
create_clock -period $hbus_freq_ns -name virt_rwds_clk

#
#Input Delay Constraint -  HB_RWDS-HB_DQ
#
set_input_delay -clock [get_clocks virt_rwds_clk]             -max
${dqs_in_max_dly} ${HB_dq_ports}
set_input_delay -clock [get_clocks virt_rwds_clk] -clock_fall -max
${dqs_in_max_dly} ${HB_dq_ports} -add_delay

set_input_delay -clock [get_clocks virt_rwds_clk]             -min
${dqs_in_min_dly} ${HB_dq_ports} -add_delay
set_input_delay -clock [get_clocks virt_rwds_clk] -clock_fall -min
${dqs_in_min_dly} ${HB_dq_ports} -add_delay

set_multicycle_path -setup -end -rise_from [get_clocks virt_rwds_clk] -
rise_to [get_clocks rwds_clk] 0
set_multicycle_path -setup -end -fall_from [get_clocks virt_rwds_clk] -
fall_to [get_clocks rwds_clk] 0

set_false_path  -fall_from [get_clocks virt_rwds_clk] -rise_to [get_clocks
rwds_clk] -setup
set_false_path  -rise_from [get_clocks virt_rwds_clk] -fall_to [get_clocks
rwds_clk] -setup
set_false_path  -fall_from [get_clocks virt_rwds_clk] -fall_to [get_clocks
rwds_clk] -hold
set_false_path  -rise_from [get_clocks virt_rwds_clk] -rise_to [get_clocks
rwds_clk] -hold

#set_false_path -from [get_clocks clk_0] -to [get_clocks rwds_clk]
#set_false_path -from [get_clocks rwds_clk] -to [get_clocks clk_0]

set_false_path -from [get_clocks rwds_clk] -to [get_clocks -of_objects
[get_pins msys_i/clk_wiz_0/inst/mmcm_adv_inst/CLKOUT0]]
set_false_path -from [get_clocks -of_objects [get_pins msys_i/clk_wiz_0
/inst/mmcm_adv_inst/CLKOUT0]] -to [get_clocks rwds_clk]

#
```

```
#Output Delay Constraint -  HB_CLK0-HB_DQ
#

create_generated_clock -name HB_CLK0_0 -source [get_pins */*/*/U_IO/U_CLK0
/dq_idx_[0].ODDR_inst/C] -multiply_by 1 -invert [get_ports HB_CLK0_0]

set_output_delay -clock [get_clocks HB_CLK0_0] -min -1.000 ${HB_dq_ports}
set_output_delay -clock [get_clocks HB_CLK0_0] -max  1.000 ${HB_dq_ports}
set_output_delay -clock [get_clocks HB_CLK0_0] -min -1.000 ${HB_dq_ports} -
clock_fall -add_delay
set_output_delay -clock [get_clocks HB_CLK0_0] -max  1.000 ${HB_dq_ports} -
clock_fall -add_delay


set_false_path -from [get_pins */*/*/U_HBC/*/dq_io_tri_reg/C] -to
${HB_dq_ports}

#set_false_path -from * -to [get_pins */*/inst/*/i_iavs0_270_rstn_1_reg
/CLR]
#set_false_path -from * -to [get_pins */*/inst/*/i_iavs0_270_rstn_2_reg
/CLR]
#set_false_path -from * -to [get_pins */*/inst/*/i_iavs0_270_rstn_3_reg
/CLR]
```

Software Design - Vitis

For Vitis project creation, follow instructions from:

Vitis

Application

Template location: "<project folder>\sw_lib\sw_apps\"

Hello TE0717

Trenz Hello World example as endless loop

Template location: \sw_lib\sw_apps\hello_te0717

The printed Text and the blinking of the red LED1 can be modified

spi_bootloader

TE modified SPI Bootloader from Henrik Brix Andersen.

Bootloader to load app or second bootloader from flash into DDR.

Here it loads the hello_te0717.elf from QSPI-Flash to RAM.

Descriptions:

- Modified Files: bootloader.c
- Changes:

- Change the SPI defines in the header
- Add some reiteration in the frist spi read call

Additional Software

No additional software is needed.

App. A: Change History and Legal Notices

Document Change History

To get content of older revision go to "Change History" of this page and select older document revision number.

Date	Document Revision	Authors	Description
Error rendering macro 'page-info' Ambiguous method overloading for method jdk.proxy241.$Proxy3496#hasContentLevelPermission. Cannot resolve	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy241.$Proxy3496#hasContentLevelPermission. Cannot resolve	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy241.$Proxy3496#hasContentLevelPermission. Cannot resolve	• initial release

which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian

which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian

which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian

. confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	. confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	. confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	
--	all	**Error rendering macro 'page-info'** Ambiguous method overloading for	--

method
jdk.
proxy24
1.$Proxy
3496#ha
sConten
tLevelPe
rmission
.
Cannot
resolve
which
method
to
invoke
for [null,
class
java.
lang.
String,
class
com.
atlassian
.
confluen
ce.
pages.
Page]
due to
overlapp
ing
prototyp
es
between
:
[interfac
e com.
atlassian
.

		confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	

Document change history.

Legal Notices

Data Privacy

Please also note our data protection declaration at https://www.trenz-electronic.de/en/Data-protection-Privacy

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REACH, RoHS and WEEE

REACH

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Users of electrical and electronic equipment in private households are required not to dispose of waste electrical and electronic equipment as unsorted municipal waste and to collect such waste electrical and electronic equipment separately. By the 13 August 2005, Member States shall have ensured that systems are set up allowing final holders and distributors to return waste electrical and electronic equipment at least free of charge. Member States shall ensure the availability and accessibility of the necessary collection facilities. Separate collection is the precondition to ensure specific treatment and recycling of waste electrical and electronic equipment and is necessary to achieve the chosen level of protection of human health and the environment in the European Union. Consumers have to actively contribute to the success of such collection and the return of waste electrical and electronic equipment. Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.

Trenz Electronic is registered under WEEE-Reg.-Nr. DE97922676.

Error rendering macro 'page-info'

Ambiguous method overloading for method jdk.proxy241.$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]