TE0817 Test Board

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Overview

Refer to https://trenz.org/te0817-info for the current online version of this manual and other available documentation.

Key Features

- Vitis/Vivado 2022.2
- QSPI
- Custom Carrier (minimum PS Design with available module components only)
- Modified FSBL (some additional outputs only)

Revision History

Date	Vivado	Project Built	Authors	Description
2023-06-29	2022.2	TE0817-test_board-vivado_2022.2-build_2_20230629142058.zip TE0817-test_board_noprebuilt-vivado_2022.2-build_2_20230629142058.zip	Manuela Strücker	• 2022.2 release
2022-09-12	2021.2.1	TE0817-test_board-vivado_2021.2-build_15_20220912093808.zip TE0817-test_board_noprebuilt-vivado_2021.2-build_15_20220912093808.zip	Manuela Strücker	• update board part file compatible to Vivado 2021.2.1
2022-06-27	2021.2	TE0817-test_board-vivado_2021.2-build_14_20220627122123.zip TE0817-test_board_noprebuilt-vivado_2021.2-build_14_20220627122123.zip	Manuela Strücker	• initial release

Design Revision History

Release Notes and Know Issues

Issues	Description	Workaround	To be fixed version
Xilinx Software	Incompatibility of board files for ZynqMP with eMMC activated between 2021.2 and 2021.2.1 patch, see Xilinx Forum Request	use corresponding board files for the Vivado versions	--

Known Issues

Requirements

Software

Software	Version	Note
Vitis	2022.2	needed, Vivado is included into Vitis installation
PetaLinux	2022.2	needed
SI ClockBuilder Pro	---	optional

Software

Hardware

Basic description of TE Board Part Files is available on TE Board Part Files.

Complete List is available on "<project folder>\board_files*_board_files.csv"

Design supports following modules:

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMMC	Others	Notes
TE0817-01-7DE21-A*	7ev_1e_4gb	REV01	4GB	128MB	NA	NA	NA

*used as reference

Hardware Modules

Design supports following carriers:

Carrier Model	Notes
TEBT0818	
TEBF0818*	

*used as reference

Hardware Carrier

Additional HW Requirements:

Additional Hardware	Notes

*used as reference

Additional Hardware

Content

For general structure and usage of the reference design, see Project Delivery - AMD devices

Design Sources

Type	Location	Notes
Vivado	<project folder>\block_design <project folder>\constraints <project folder>\ip_lib <project folder>\board_files	Vivado Project will be generated by TE Scripts
Vitis	<project folder>\sw_lib	Additional Software Template for Vitis and apps_list.csv with settings automatically for Vitis app generation

Design sources

Additional Sources

Type	Location	Notes
---	---	---

Additional design sources

Prebuilt

File	File-Extension	Description
BIF-File	*.bif	File with description to generate Bin-File
BIN-File	*.bin	Flash Configuration File with Boot-Image (Zynq-FPGAs)
BIT-File	*.bit	FPGA (PL Part) Configuration File
DebugProbes-File	*.ltx	Definition File for Vivado/Vivado Labtools Debugging Interface
Diverse Reports	---	Report files in different formats
Hardware-Platform-Description-File	*.xsa	Exported Vivado hardware description file for Vitis and PetaLinux
LabTools Project-File	*.lpr	Vivado Labtools Project File
Software-Application-File	*.elf	Software Application for Zynq or MicroBlaze Processor Systems

Prebuilt files (only on ZIP with prebuilt content)

Download

Reference Design is only usable with the specified Vivado/Vitis/PetaLinux version. Do never use different Versions of Xilinx Software for the same Project.

Reference Design is available on:

- TE0817 "Test Board" Reference Design

Design Flow

Reference Design is available with and without prebuilt files. It's recommended to use TE prebuilt files for first launch.

Trenz Electronic provides a tcl based built environment based on Xilinx Design Flow.

See also:

- AMD Development Tools#XilinxSoftware-BasicUserGuides
- Vivado Projects - TE Reference Design
- Project Delivery.

The Trenz Electronic FPGA Reference Designs are TCL-script based project. Command files for execution will be generated with "_create_win_setup.cmd" on Windows OS and "_create_linux_setup.sh" on Linux OS.

TE Scripts are only needed to generate the vivado project, all other additional steps are optional and can also executed by Xilinx Vivado/Vitis GUI. For currently Scripts limitations on Win and Linux OS see: Project Delivery Currently limitations of functionality

Caution! Win OS has a 260 character limit for path lengths which can affect the Vivado tools. To avoid this issue, use Virtual Drive or the shortest possible names and directory locations for the reference design (for example "x:\<project folder>")

1. Run _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell:

_create_win_setup.cmd/_create_linux_setup.sh

```
-----------------------Set design paths---------------------------
-- Run Design with: _create_win_setup
-- Use Design Path: <absolute project path>
------------------------------------------------------------------
------------------------TE Reference
Design--------------------------
------------------------------------------------------------------
-- (0)  Module selection guide, project creation...prebuilt export...
-- (1)  Create minimum setup of CMD-Files and exit Batch
-- (2)  Create maximum setup of CMD-Files and exit Batch
-- (3)  (internal only) Dev
-- (4)  (internal only) Prod
-- (c)  Go to CMD-File Generation (Manual setup)
-- (d)  Go to Documentation (Web Documentation)
-- (g)  Install Board Files from Xilinx Board Store (beta)
-- (a)  Start design with unsupported Vivado Version (beta)
-- (x)  Exit Batch (nothing is done!)
----
Select (ex.:'0' for module selection guide):
```

2. Press 0 and enter to start "Module Selection Guide"
3. Create project and follow instructions of the product selection guide, settings file will be configured automatically during this process.

- optional for manual changes: Select correct device and Xilinx install path on "design_basic_settings.cmd" and create Vivado project with "vivado_create_project_guimode.cmd"

  > ⚠ Note: Select correct one, see also Vivado Board Part Flow

4. Create hardware description file (.xsa file) and export to prebuilt folder

   run on Vivado TCL (Script generates design and export files into "<project folder>\prebuilt\hardware\<short name>")

   ```
   TE::hw_build_design -export_prebuilt
   ```

   > ⓘ Using Vivado GUI is the same, except file export to prebuilt folder.

5. Generate Programming Files with Vitis

   run on Vivado TCL (Script generates applications and bootable files, which are defined in "test_board\sw_lib\apps_list.csv")

   ```
   TE::sw_run_vitis -all
   TE::sw_run_vitis (optional; Start Vitis from Vivado GUI or start with TE Scripts on Vivado TCL)
   ```

   > ⚠ TCL scripts generate also platform project, this must be done manually in case GUI is used. See Vitis

Launch

Programming

> ⚠ Check Module and Carrier TRMs for proper HW configuration before you try any design.
>
> Reference Design is also available with prebuilt files. It's recommended to use TE prebuilt files for first launch.

Xilinx documentation for programming and debugging: Vivado/Vitis/SDSoC-Xilinx Software Programming and Debugging

Get prebuilt boot binaries

1. Run _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell
2. Press 0 and enter to start "Module Selection Guide"
   a. Select assembly version
   b. Validate selection
   c. Select create and open delivery binary folder

> Note: Folder "<project folder>_binaries_<Article Name>" with subfolder "boot_<app name>" for different applications will be generated

QSPI-Boot mode

1. Connect **JTAG** and power on carrier with module
2. Set Boot Mode to **JTAG**
3. Open Vivado Project with "vivado_open_existing_project_guimode.cmd" or if not created, create with "vivado_create_project_guimode.cmd"

run on Vivado TCL (Script programs BOOT.bin on QSPI flash)
`TE::pr_program_flash -swapp hello_te0817`

4. Set Boot Mode to **QSPI-Boot**
   - Depends on Carrier, see carrier TRM.

SD-Boot mode

This does not work, because SD controller is not selected on PS.

JTAG

Load configuration and Application with Vitis Debugger into device

Usage

1. Prepare HW like described on section Programming
2. Connect UART USB (most cases same as JTAG)
3. Select QSPI as Boot Mode

> Note: See TRM of the Carrier, which is used.

4. Power On PCB
   1. Zynq Boot ROM loads FSBL from QSPI into OCM,
   2. FSBL init PS, programs PL using the bitstream and loads Application into DDR,

System Design - Vivado

Block Design

Block Design

PS Interfaces

Activated interfaces:

Type	Note
DDR	
QSPI	MIO
UART0	MIO
SWDT0..1	
TTC0..3	

PS Interfaces

Constraints

Basic module constraints

_i_bitgen.xdc

```
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property BITSTREAM.CONFIG.UNUSEDPIN PULLNONE [current_design]
```

Design specific constraints

Not needed.

Software Design - Vitis

For Vitis project creation, follow instructions from:

Vitis

Application

Template location: "<project folder>\sw_lib\sw_apps\"

zynqmp_fsbl

TE modified 2022.2 FSBL

General:

- Modified Files: xfsbl_main.c, xfsbl_hooks.h/.c, xfsbl_board.h/.c (search for 'TE Mod' on source code)
- Add Files: te_xfsbl_hooks.h/.c (for hooks and board)
- General Changes:
  - Display FSBL Banner and Device Name

hello_te0817

Hello TE0817 is a Xilinx Hello World example as endless loop instead of one console output.

Additional Software

No additional software is needed.

App. A: Change History and Legal Notices

Document Change History

To get content of older revision go to "Change History" of this page and select older document revision number.

Date	Document Revision	Authors	Description
Error rendering macro 'page-info' Ambiguous	**Error rendering macro 'page-info'** Ambiguous	**Error rendering macro 'page-info'** Ambiguous	• 2022.2 release

method overloading for method jdk.proxy241.$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interfac

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e com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	e com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	e com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	

2022-09-12	v.5	Manuela Strücker	• initial release
2022-09-06	v.4	Manuela Strücker	• initial release
--	all	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy241.$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.	--

atlassian . confluence. pages. Page] due to overlapping prototypes between : [interface com. atlassian . confluence.user. ConfluenceUser, class java. lang. String, class com. atlassian . confluence.core. ContentEntityObject] [interface com. atlassian .user. User,

		class java. lang. String, class com. atlassian . confluen ce.core. Content EntityOb ject]	

Document change history.

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