

# TE0717 Getting Started Guide

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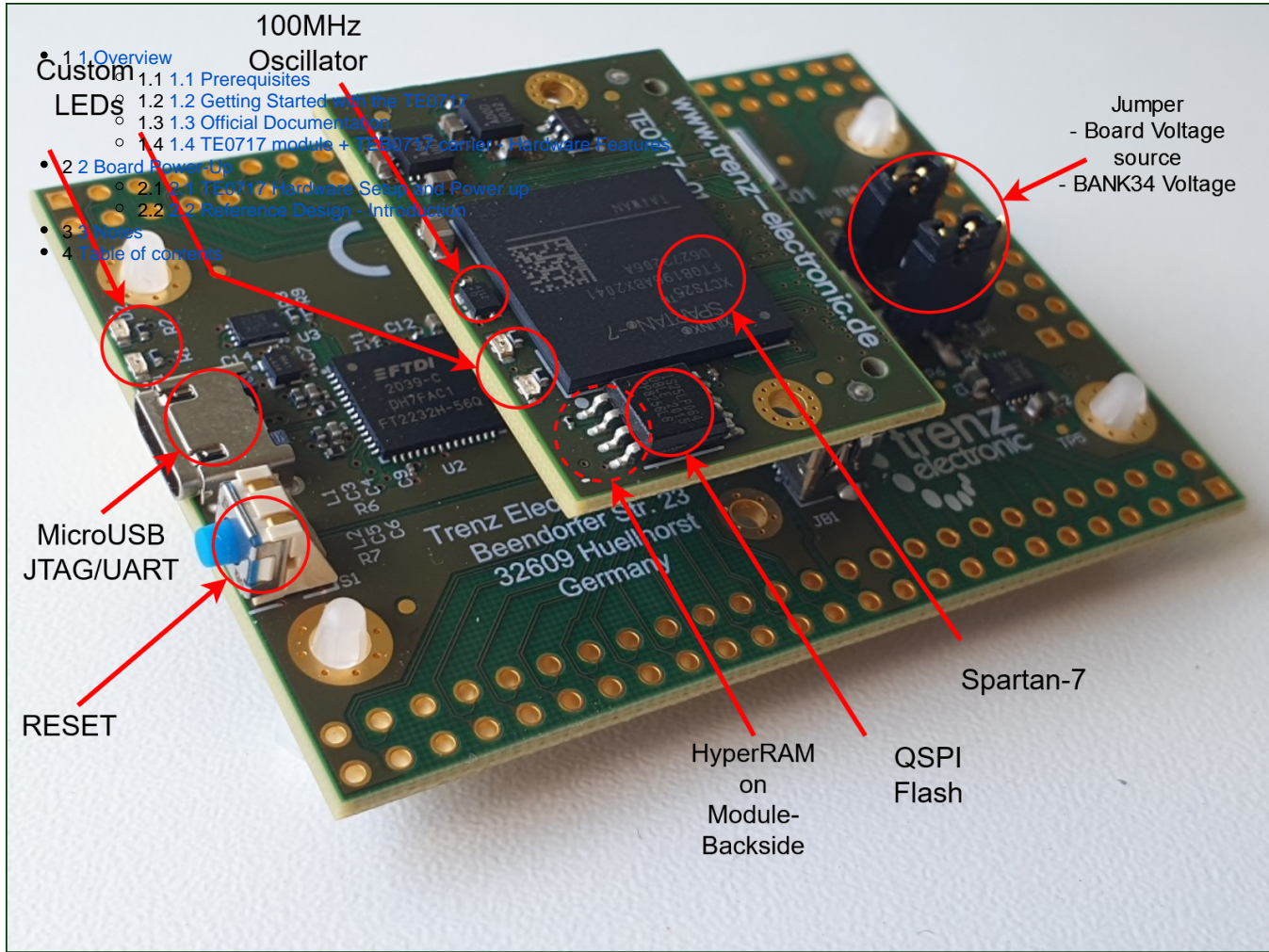


Figure 1: Module TE0717 with Carrier TEB0717

## 1 Overview

This guide showcases the important components of the module-carrier combination TE0717 + TEB0717 and introduces the available script-based reference design to get the board up and running.

### 1.1 Prerequisites

Hardware	Software
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- TE0717 module
- TEB0717 carrier
- Micro-USB cable

- Vitis (Vivado included)
- PuTTY (or any other serial communicator)
- [TE0717 Reference Design](#)

## 1.2 Getting Started with the TE0717

The module TE0717 has a Xilinx Spartan-7 FPGA onboard that allows you to create extensive digital hardware and software designs.

Most of the FPGA IOs are spread around the carrier. The TE0717 is assembled with HyperRAM(64 Mbit), QSPI non-volatile Flash memory(64 Mbit) and plenty of IOs which enable great hardware expandability. For communication and configuration the carrier offers a JTAG/UART Interface.

This Getting Started Guide shows how to set up the board, attach the jumpers, wire it up and connect it with the software. The [TE0717 Test Board](#) description goes into "how to use the provided reference design" and in [here](#) we touch the aspect of how to add your own IP to the design. This includes changing the Vivado Block Design, regenerating the bitstream and using the hardware export(.xsa file) in Vitis to develop software that runs on the MicroBlaze.

## 1.3 Official Documentation

- Official links to the shop:
  - coming soon!
- Technical Reference Manual:
  - coming soon!
- Resources & Reference Designs:
  - [TE0717 Resources](#)
  - [TE0717 Reference Designs](#)

## 1.4 TE0717 module + TEB0717 carrier - Hardware Features

- FPGA
  - Xilinx Spartan-7 - XC7S25-1FTGB196C
- Clocking
  - 100 MHz clock from clocking chip SiT8008 on TE0717 module
- Memory
  - 8 MByte DDR HyperRAM
  - 8 MByte Quad-SPI Flash
- Communication
  - On carrier USB-JTAG Programming
- Connectors
  - B2B connector - Module(JM1) to Carrier(JB1)
  - Unpopulated PIN Header on carrier(J3, J4, J5)
- Configuration and Debug
  - On carrier USB-JTAG interface
- Jumper
  - Adjustable BANK34 supply voltage (J2)
  - Power source (J1)
- General Purpose I/O
  - 2x2 user LEDs (red,green)

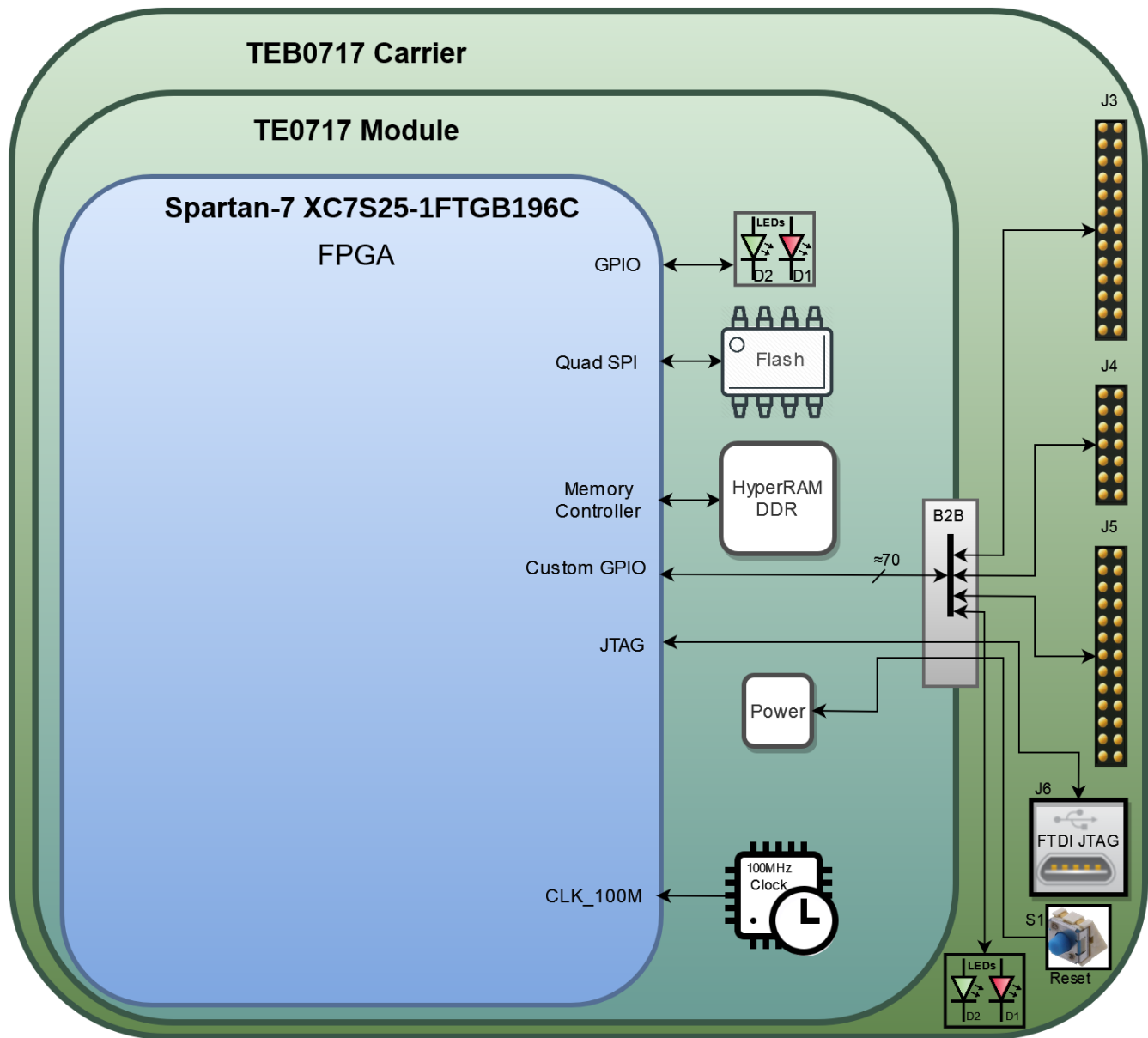


Figure 2: TE0717+TEB0717 Hardware Blockdiagram

Basic IOs<->FPGA connections are as following, Table 1:

	Color	Signal	FPGA Pin	Function
LED D1(on carrier)	red	B14_L24_P	P10	general purpose
LED D2(on carrier)	green	B14_L24_N	P11	"
LED D1(on module)	red	LED1	D14	"
LED D2(on module)	green	LED2	C14	"
Clock	--	CLK_100M	G11	singled ended 100MHz clock



Information on IO routing and FPGA pin connections can be found in the [schematics](#).

## 2 Board Power-Up

### 2.1 TE0717 Hardware Setup and Power up

1. Before connecting the Board to the PC, make sure to properly mount the module TE0717 onto the carrier TEB0717 via the B2B connector like in Figure 1.
2. Check the Jumper setting

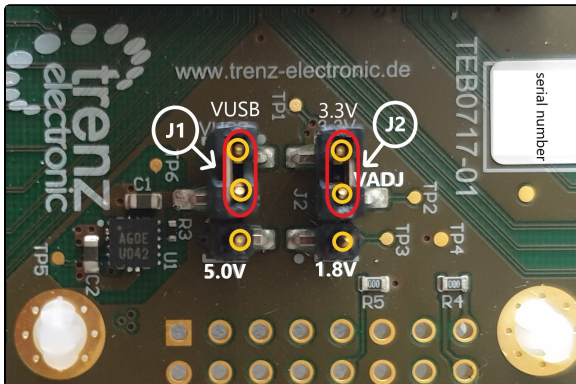


Figure 3: Jumper setting

The Voltage set with Jumper J1 determines the source of the input voltage for the voltages regulator chip U1. Either 5V from the MicroUSB port(VUSB) or 5V from pin header J4.

With the shown setting of Jumper J2 the voltage VADJ is set to 3.3V that comes from the carriers voltage regulator chip U1. The 1.8V comes from the module. The Voltage VADJ is wired to the module and is used as the BANK34 supply voltage.

3. Use a MicroUSB cable to connect your board to the PC.cc
4. All the LEDs are simply routed to the FPGA, hence none of them should be turned on. If the qspi flash on the module is preloaded with a design though, it might be that some LEDs are blinking.
5. In case the QSPI Flash is loaded with the reference design, you can connect to the board with a program like *PuTTY*. Just open up a serial session with baud-rate of **9600** and the right COM-port(visible in Device Manager).  
You may need to press the RESET-button.

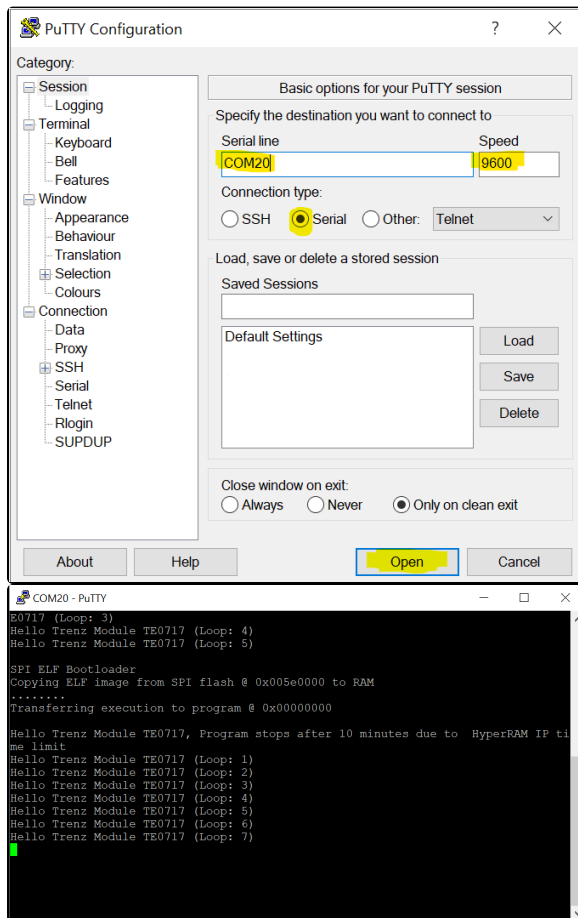


Figure 4: Terminal(MicroBlaze output)

## 2.2 Reference Design - Introduction

We provide a reference design that interacts with most of the peripheral on the module. The provided design "*TE0717 test board*" shows how to connect the different parts of the module to simplify the development of your own application. You can use it for your own design but keep in mind the overall FPGA resources and power consumption before deployment.

The reference design we are introducing in this guide is "*TE0717 test board*". The most important steps to get it up and running are explained on [TE0717 Test Board](#). The Download is available [here](#).

The reference design is only usable with the specified Vivado/Vitis version. Always use the same version of Xilinx Software for one Project. (e.g. use reference design 2021.2 with vitis installation 2021.2)

The components of the reference design are illustrated in the following figure:

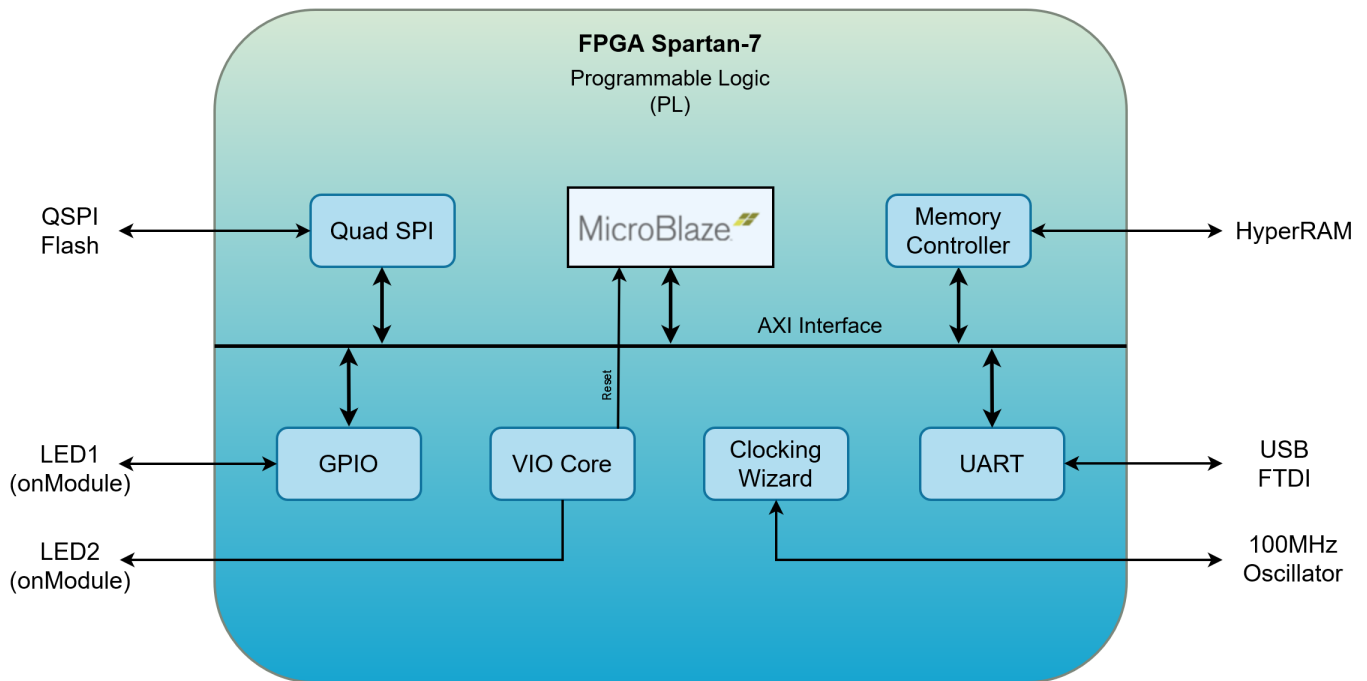


Figure 5: Blockdiagram of the Reference Design

The Cores are connected via the AXI Interface with the MicroBlaze Processor. How they are mapped into the address space can be seen in the address editor:

Name	Interface	Slave Segment	Master Base Address	Range	Master High Address
Network 0					
/microblaze_0 (32 address bits : 4G)					
/axi_gpio_0/S_AXI	S_AXI	Reg	0x4000_0000	64K	0x4000_FFFF
/axi_intc_0/S_AXI	s_axi	Reg	0x4120_0000	64K	0x4120_FFFF
/axi_quad_spi_0/AXI_LITE	AXI_LITE	Reg	0x44A0_0000	64K	0x44A0_FFFF
/axi_uartlite_0/S_AXI	S_AXI	Reg	0x4060_0000	64K	0x4060_FFFF
/microblaze_0/local_memory/dmb_bram_if_cntb/SLMB	SLMB	Mem	0x0000_0000	16K	0x0000_FFFF
/all_hnmc_axi_top_0/500_AXI	500_AXI	HyperRAM	0x0400_0000	8M	0x04FF_FFFF
/microblaze_0/instruction (32 address bits : 4G)					
/microblaze_0/local_memory/finb_bram_if_cntb/SLMB	SLMB	Mem	0x0000_0000	16K	0x0000_FFFF
/all_hnmc_axi_top_0/500_AXI	500_AXI	HyperRAM	0x0400_0000	8M	0x04FF_FFFF

Figure 6: Vivado Address Editor - Address Mapping

For example the AXI GPIO IP Core which has a LED1 connected to it, can be controlled with software(C/C++) by raising the bits mapped to the address 0x4000 0000.

The VIO Core enables you to control connected IOs via the Vivado Hardware Manager(like LED2).

## 3 Notes

### Document Revision History

Version	Date	Description	Author
1.0	2022-07-20	initial release	WH

## Revision History