TE0714 Test Board

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Overview

This example contains a simple MicroBlaze Design with an endless loop application printing "Hello Trenz Module TE0714 and setting the onBoard LED blink.

Refer to http://trenz.org/te0714-trm for the current online version of this manual and other available documentation.

Key Features

- Vitis/Vivado 2021.2
- MicroBlaze
- UART
- QSPI Flash
- Fmeter

Revision History

Date	Vivado	Project Built	Authors	Description
2023-04-17	2021.2	TE0714-test_board_noprebuilt-vivado_2021.2-build_20_20230417135347.zip TE0714-test_board-vivado_2021.2-build_20_20230417135347.zip	Waldemar Hanemann	• Added variants
2022-10-17	2021.2	TE0714-test_board_noprebuilt-vivado_2021.2-build_18_20221017131053.zip TE0714-test_board-vivado_2021.2-build_18_20221017131053.zip	Waldemar Hanemann	• Added VIO, JTAG2AXI Master, AXI 32REG IP • EN_GTPWR Pin control adjustment - tristate
2022-07-22	2021.2	TE0714-test_board_noprebuilt-vivado_2021.2-build_14_20220722142940.zip TE0714-test_board-vivado_2021.2-build_14_20220722142940.zip	Waldemar Hanemann	• initial release

Design Revision History

Release Notes and Know Issues

Issues	Description	Workaround	To be fixed version

No known issues	---	---	---

Known Issues

Requirements

Software

Software	Version	Note
Vitis	2021.2	needed, Vivado is included into Vitis installation

Software

Hardware

Basic description of TE Board Part Files is available on TE Board Part Files.

Complete List is available on "<project folder>\board_files*_board_files.csv"

Design supports following modules:

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMMC	Others	Notes
TE0714-02-35-2I	35_2i	REV02	---	16MB	---	---	3.3V qspi flash
TE0714-02-35-2IC6	35_2ic6	REV02	---	16MB	---	---	1.8V qspi flash
TE0714-02-50-2I	50_2i	REV02	---	16MB	---	---	3.3V qspi flash
TE0714-02-50-2IC6	50_2ic6	REV02	---	16MB	---	---	1.8V qspi flash
TE0714-03-35-2I	35_2i	REV03	---	16MB	---	---	3.3V qspi flash
TE0714-03-35-2I3	35_2i	REV03	---	16MB	---	---	3.3V qspi flash
TE0714-03-35-2IC7	35_2i	REV03	---	16MB	---	---	3.3V qspi flash
TE0714-03-50-2I	50_2i	REV03	---	16MB	---	---	3.3V qspi flash
TE0714-03-50-2IAC6	50_2iac6	REV03	---	16MB	---	---	1.8V qspi flash
TE0714-03-S007	50_2i	REV03	---	16MB	---	---	3.3V qspi flash
TE0714-04-42I-7-B	35_2i	REV04	---	16MB	---	---	3.3V qspi flash
TE0714-04-52I-7-B*	50_2i	REV04	---	16MB	---	---	3.3V qspi flash
TE0714-04-42I-7-C	35_2i	REV04	---	16MB	---	---	3.3V qspi flash

*used as reference

Hardware Modules

Design supports following carriers:

Carrier Model	Notes
TEBA0714-01*	

*used as reference

Hardware Carrier

Additional HW Requirements:

Additional Hardware	Notes
USB Cable for JTAG/UART	Check Carrier Board and Programmer for correct type
XMOD Programmer	Carrier Board dependent, only if carrier has no own FTDI

*used as reference

Additional Hardware

Content

For general structure and usage of the reference design, see Project Delivery - AMD devices

Design Sources

Type	Location	Notes
Vivado	<project folder>\block_design <project folder>\constraints <project folder>\ip_lib <project folder>\board_files	Vivado Project will be generated by TE Scripts
Vitis	<project folder>\sw_lib	Additional Software Template for Vitis and apps_list.csv with settings automatically for Vitis app generation

Design sources

Additional Sources

Type	Location	Notes
---	---	---

Additional design sources

Prebuilt

File	File-Extension	Description
BIF-File	*.bif	File with description to generate Bin-File
DebugProbes-File	*.ltx	Definition File for Vivado/Vivado Labtools Debugging Interface

Hardware-Platform-Description-File	*.xsa	Exported Vivado hardware description file for Vitis and PetaLinux
LabTools Project-File	*.lpr	Vivado Labtools Project File
MCS-File	*.mcs	Flash Configuration File with Boot-Image (MicroBlaze or FPGA part only)
MMI-File	*.mmi	File with BRAM-Location to generate MCS or BIT-File with *.elf content (MicroBlaze only)
Software-Application-File	*.elf	Software Application for Zynq or MicroBlaze Processor Systems

Prebuilt files (only on ZIP with prebuilt content)

Download

Reference Design is only usable with the specified Vivado/Vitis version. Do never use different Versions of Xilinx Software for the same Project.

Reference Design is available on:

- TE0714 "Test Board" Reference Design

Design Flow

Reference Design is available with and without prebuilt files. It's recommended to use TE prebuilt files for first launch.

Trenz Electronic provides a tcl based built environment based on Xilinx Design Flow.

See also:

- AMD Development Tools#XilinxSoftware-BasicUserGuides
- Vivado Projects - TE Reference Design
- Project Delivery.

The Trenz Electronic FPGA Reference Designs are TCL-script based project. Command files for execution will be generated with "_create_win_setup.cmd" on Windows OS and "_create_linux_setup.sh" on Linux OS.

TE Scripts are only needed to generate the vivado project, all other additional steps are optional and can also executed by Xilinx Vivado/Vitis GUI. For currently Scripts limitations on Win and Linux OS see: Project Delivery Currently limitations of functionality

Caution! Win OS has a 260 character limit for path lengths which can affect the Vivado tools. To avoid this issue, use Virtual Drive or the shortest possible names and directory locations for the reference design (for example "x:\<project folder>")

1. Run _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell:

_create_win_setup.cmd/_create_linux_setup.sh

```
-----------------------Set design paths---------------------------
-- Run Design with: _create_win_setup
-- Use Design Path: <absolute project path>
------------------------------------------------------------------
-----------------------TE Reference
Design-------------------------
------------------------------------------------------------------
-- (0)  Module selection guide, project creation...prebuilt export...
-- (1)  Create minimum setup of CMD-Files and exit Batch
-- (2)  Create maximum setup of CMD-Files and exit Batch
-- (3)  (internal only) Dev
-- (4)  (internal only) Prod
-- (c)  Go to CMD-File Generation (Manual setup)
-- (d)  Go to Documentation (Web Documentation)
-- (g)  Install Board Files from Xilinx Board Store (beta)
-- (a)  Start design with unsupported Vivado Version (beta)
-- (x)  Exit Batch (nothing is done!)
----
Select (ex.:'0' for module selection guide):
```

2. Press 0 and enter to start "Module Selection Guide"
3. Create project and follow instructions of the product selection guide, settings file will be configured automatically during this process.
    - optional for manual changes: Select correct device and Xilinx install path on "design_basic_settings.cmd" and create Vivado project with "vivado_create_project_guimode.cmd"

Note: Select correct one, see also Vivado Board Part Flow

4. Create hardware description file (.xsa file) for PetaLinux project and export to prebuilt folder

run on Vivado TCL (Script generates design and export files into "<project folder>\prebuilt\hardware\<short name>")

```
TE::hw_build_design -export_prebuilt
```

Using Vivado GUI is the same, except file export to prebuilt folder.

5. Generate Programming Files with Vitis
    a. Run on Vivado TCL:

Script generates applications and bootable files, which are defined in "sw_lib\apps_list.csv"

```
TE::sw_run_vitis -all
```

    b. The newly built application "\prebuilt\software\<short name>\hello_te0714.elf" gets copied into "\firmware\microblaze_0\"

c. Regenerate Vivado Project or Update Bitfile only, with new "hello_te0714.elf"

> ⚠ TCL scripts generate also platform project, this must be done manually in case GUI is used. See Vitis

Launch

Programming

> ⚠ Check Module and Carrier TRMs for proper HW configuration before you try any design.
>
> Reference Design is also available with prebuilt files. It's recommended to use TE prebuilt files for first launch.

Xilinx documentation for programming and debugging: Vivado/Vitis/SDSoC-Xilinx Software Programming and Debugging

Get prebuilt boot binaries

1. Run _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell
2. Press 0 and enter to start "Module Selection Guide"
    a. Select assembly version
    b. Validate selection
    c. Select create and open delivery binary folder

> ⓘ Note: Folder "<project folder>_binaries_<Article Name>" with subfolder "boot_<app name>" for different applications will be generated

QSPI-Boot mode

1. Connect JTAG and power on carrier with module
2. Open Vivado Project with "vivado_open_existing_project_guimode.cmd" or if not created, create with "vivado_create_project_guimode.cmd"

run on Vivado TCL (Script programs BOOT.bin on QSPI flash)
`TE::pr_program_flash -swapp hello_te0714`

3. Power your Board OFF and ON to start the application and see the output in the console

JTAG

Not used on this example.

Usage

1. Prepare HW like described on section Programming
2. Connect UART USB (most cases same as JTAG)
3. Select QSPI as Boot Mode

> Note: See TRM of the Carrier, which is used.

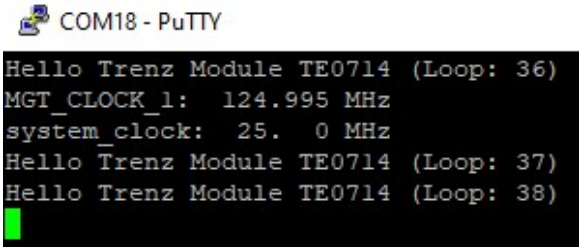
4. Power On PCB
   1. FPGA Loads Bitfile from Flash
   2. hello_te0714.elf application starts on MicroBlaze
   3. Hello Trenz will be printed on UART console

   info: Do not reboot, if Bitfile programming over JTAG is used as programming method.

   a. ### UART

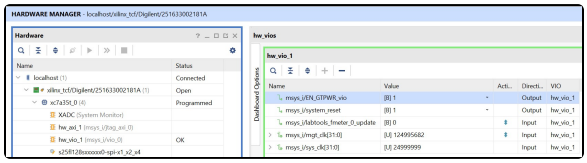
      Open Serial Console (e.g. putty)

      i. Speed: 9600
      ii. COM Port: Win OS, see device manager, Linux OS see dmesg |grep tty (UART is *USB1)



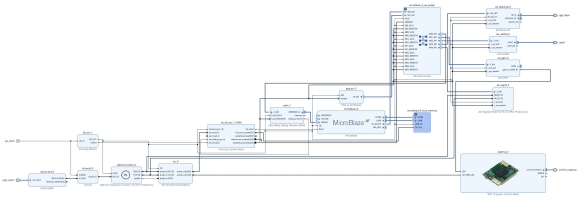
Vivado HW Manager

- Open Vivado HW Manager
- Add VIO to Dashboard
- Set Radix to unsigned integer for FMeterCLKs (fm_*). Note: Measurement is not accurate!
- Control:
  1. system Reset
  2. Enable MGT Power & Clock



System Design - Vivado

Block Design



Block Design

Constraints

Basic module constraints

_i_bitgen_common.xdc

```
#
# Default common settings that do not depend assembly variant
#
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property BITSTREAM.CONFIG.CONFIGRATE 66 [current_design]
set_property CONFIG_MODE SPIx4 [current_design]

set_property BITSTREAM.CONFIG.SPI_32BIT_ADDR NO [current_design]
set_property BITSTREAM.CONFIG.SPI_BUSWIDTH 4 [current_design]
set_property BITSTREAM.CONFIG.M1PIN PULLNONE [current_design]
set_property BITSTREAM.CONFIG.M2PIN PULLNONE [current_design]
set_property BITSTREAM.CONFIG.M0PIN PULLNONE [current_design]

set_property BITSTREAM.CONFIG.USR_ACCESS TIMESTAMP [current_design]

#check mgt clock routing
set_false_path -from [get_clocks mgt_clock1_clk_p] -to [get_clocks -
of_objects [get_pins msys_i/clk_wiz_1/inst/mmcm_adv_inst/CLKOUT0]]
set_false_path -from [get_pins {msys_i/labtools_fmeter_0/U0/FMETER_gen[1].
COUNTER_F_inst/bl.DSP48E_2/CLK}] -to [get_pins {msys_i/labtools_fmeter_0/U0
/F_reg[43]/D}]
set_false_path -from [get_pins {msys_i/labtools_fmeter_0/U0/FMETER_gen[1].
COUNTER_F_inst/bl.DSP48E_2/CLK}] -to [get_pins {msys_i/labtools_fmeter_0/U0
/F_reg[40]/D}]
set_false_path -from [get_clocks -of_objects [get_pins msys_i/clk_wiz_1
/inst/mmcm_adv_inst/CLKOUT0]] -to [get_clocks mgt_clock1_clk_p]
set_multicycle_path -from [get_pins msys_i/labtools_fmeter_0/U0/toggle_reg
/C] -to [get_pins {msys_i/labtools_fmeter_0/U0/FMETER_gen[1].COUNTER_F_inst
/bl.DSP48E_2/RSTINMODE}] 1
```

For 1.8V variants:

_i_bitgen_common18.xdc

```
set_property CONFIG_VOLTAGE 1.8 [current_design]
set_property CFGBVS GND [current_design]
```

For 3.3V variants:

_i_bitgen_common33.xdc

```
set_property CONFIG_VOLTAGE 3.3 [current_design]
set_property CFGBVS VCCO [current_design]
```

Design specific constraints

All others IOs are constraint in the Board Files.

Software Design - Vitis

For Vitis project creation, follow instructions from:

Vitis

Application

Template location: "<project folder>\sw_lib\sw_apps\"

Hello TE0714

Trenz Hello World example and frequency read as endless loop

Template location: \sw_lib\sw_apps\hello_te0714

The printed Text and the blinking of the red LED can be modified

Additional Software

No additional software is needed.

App. A: Change History and Legal Notices

Document Change History

To get content of older revision go to "Change History" of this page and select older document revision number.

Date	Document Revision	Authors	Description
Error rendering macro 'page-info' Ambiguous method overloading for method jdk.proxy241.$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy241.$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy241.$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.	• Added variants

confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.

confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.

confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.

lang. String, class com. atlassian . confluen ce.core. Content EntityOb ject]	lang. String, class com. atlassian . confluen ce.core. Content EntityOb ject]	lang. String, class com. atlassian . confluen ce.core. Content EntityOb ject]	
2022-10-17	v.2	Waldemar Hanemann	• Added VIO, JTAG2AXI Master, AXI 32REG IP • EN_GTPWR Pin control adjustment - tristate
2022-07-22	v.1	Waldemar Hanemann	• initial release
--	all	**Error renderi ng macro 'page-info'** Ambiguo us method overload ing for method jdk. proxy24 1.$Proxy 3496#ha sConten	--

tLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.

		lang. String, class com. atlassian . confluen ce.core. Content EntityOb ject] [interfac e com. atlassian .user. User, class java. lang. String, class com. atlassian . confluen ce.core. Content EntityOb ject]	

Document change history.

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Error rendering macro 'page-info'

Ambiguous method overloading for method jdk.proxy241.$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]