TE0711 Test Board

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Overview

This example contains a simple MicroBlaze Design running an endless loop application printing "Hello Trenz Module TE0711" and toggling the onBoard LED blink in order D1 to D4.

Refer to http://trenz.org/te0711-user-manual for the current online version of this manual and other available documentation.

Key Features

- Vitis/Vivado 2021.2
- MicroBlaze
- UART
- QSPI Flash
- LED

Revision History

Date	Vivado	Project Built	Authors	Description
2024-01-24	2023.2	TE0711-test_board_noprebuilt-vivado_2023.2-build_4_20240124092126.zip TE0711-test_board-vivado_2023.2-build_4_20240124092126.zip	Waldemar Hanemann	• 2023.2 update
2022-08-22	2021.2	TE0711-test_board-vivado_2021.2-build_15_20220822132519.zip TE0711-test_board_noprebuilt-vivado_2021.2-build_15_20220822132519.zip	Waldemar Hanemann	• 2021.2 update • document style update
2020-09-01	2019.2	TE0711-test_board-vivado_2019.2-build_14_20200901073500.zip TE0711-test_board_noprebuilt-vivado_2019.2-build_14_20200901073630.zip	John Hartfiel	• 2019.2 update

2017-12-07	2017.2	TE0711-test_board_noprebuilt-vivado_2017.2-build_05_20171207122944.zip TE0711-test_board-vivado_2017.2-build_05_20171207122644.zip	John Hartfiel	• initial release

Design Revision History

Release Notes and Know Issues

Issues	Description	Workaround	To be fixed version
No known issues	---	---	---

Known Issues

Requirements

Software

Software	Version	Note
Vitis	2023.2	needed, Vivado is included into Vitis installation

Software

Hardware

Basic description of TE Board Part Files is available on TE Board Part Files.

Complete List is available on "<project folder>\board_files*_board_files.csv"

Design supports following modules:

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMMC	Others	Notes
TE0711-01-35-2C	35_2c	REV01	NA	32MB	NA	NA	NA
TE0711-01-100-2C	100_2c	REV01	NA	32MB	NA	NA	NA
TE0711-01-35-2I	35_2i	REV01	NA	32MB	NA	NA	NA
TE0711-01-100-2I	100_2i	REV01	NA	32MB	NA	NA	NA
TE0711-01-S001	100_2i	REV01	NA	32MB	NA	NA	NA
TE0711-02-42C-1-A*	35_2c	REV02	NA	32MB	NA	NA	NA
TE0711-02-42I-1-A	35_2i	REV02	NA	32MB	NA	NA	NA
TE0711-02-72C-1-A	100_2c	REV02	NA	32MB	NA	NA	NA

TE0711-02-72I-1-A	100_2i	REV02	NA	32MB	NA	NA	NA
TE0711-02-S001	35_2i	REV02	NA	32MB	NA	NA	NA

*used as reference

Hardware Modules

Design supports following carriers:

Carrier Model	Notes
TE0701	
TE0703*	
TE0705	
TE0706	
TEBA0841	

*used as reference

Hardware Carrier

Additional HW Requirements:

Additional Hardware	Notes
USB Cable for JTAG/UART	Check Carrier Board and Programmer for correct type
XMOD Programmer	Carrier Board dependent, only if carrier has no own FTDI

Additional Hardware

Content

For general structure and usage of the reference design, see Project Delivery - AMD devices

Design Sources

Type	Location	Notes
Vivado	<project folder>\block_design <project folder>\constraints <project folder>\ip_lib <project folder>\board_files	Vivado Project will be generated by TE Scripts
Vitis	<project folder>\sw_lib	Additional Software Template for Vitis and apps_list.csv with settings automatically for Vitis app generation

Design sources

Additional Sources

Type	Location	Notes
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Additional design sources

Prebuilt

File	File-Extension	Description
BIF-File	*.bif	File with description to generate Bin-File
DebugProbes-File	*.ltx	Definition File for Vivado/Vivado Labtools Debugging Interface
Hardware-Platform-Description-File	*.xsa	Exported Vivado hardware description file for Vitis and PetaLinux
LabTools Project-File	*.lpr	Vivado Labtools Project File
MCS-File	*.mcs	Flash Configuration File with Boot-Image (MicroBlaze or FPGA part only)
MMI-File	*.mmi	File with BRAM-Location to generate MCS or BIT-File with *.elf content (MicroBlaze only)
Software-Application-File	*.elf	Software Application for Zynq or MicroBlaze Processor Systems

Prebuilt files (only on ZIP with prebuilt content)

Download

Reference Design is only usable with the specified Vivado/Vitis version. Do never use different Versions of Xilinx Software for the same Project.

Reference Design is available on:

- TE0711 "Test Board" Reference Design

Design Flow

Reference Design is available with and without prebuilt files. It's recommended to use TE prebuilt files for first launch.

Trenz Electronic provides a tcl based built environment based on Xilinx Design Flow.

See also:

- AMD Development Tools#XilinxSoftware-BasicUserGuides
- Vivado Projects - TE Reference Design
- Project Delivery.

The Trenz Electronic FPGA Reference Designs are TCL-script based project. Command files for execution will be generated with "_create_win_setup.cmd" on Windows OS and "_create_linux_setup.sh" on Linux OS.

TE Scripts are only needed to generate the vivado project, all other additional steps are optional and can also executed by Xilinx Vivado/Vitis GUI. For currently Scripts limitations on Win and Linux OS see: Project Delivery Currently limitations of functionality

> ⚠ **Caution!** Win OS has a 260 character limit for path lengths which can affect the Vivado tools. To avoid this issue, use Virtual Drive or the shortest possible names and directory locations for the reference design (for example "x:\<project folder>")

1. Run _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell:

_create_win_setup.cmd/_create_linux_setup.sh

```
-----------------------Set design paths---------------------------
-- Run Design with: _create_win_setup
-- Use Design Path: <absolute project path>
------------------------------------------------------------------
-----------------------TE Reference
Design--------------------------
------------------------------------------------------------------
-- (0)  Module selection guide, project creation...prebuilt export...
-- (1)  Create minimum setup of CMD-Files and exit Batch
-- (2)  Create maximum setup of CMD-Files and exit Batch
-- (3)  (internal only) Dev
-- (4)  (internal only) Prod
-- (c)  Go to CMD-File Generation (Manual setup)
-- (d)  Go to Documentation (Web Documentation)
-- (g)  Install Board Files from Xilinx Board Store (beta)
-- (a)  Start design with unsupported Vivado Version (beta)
-- (x)  Exit Batch (nothing is done!)
----
Select (ex.:'0' for module selection guide):
```

2. Press 0 and enter to start "Module Selection Guide"
3. Create project and follow instructions of the product selection guide, settings file will be configured automatically during this process.
   - optional for manual changes: Select correct device and Xilinx install path on "design_basic_settings.cmd" and create Vivado project with "vivado_create_project_guimode.cmd"

> ⚠ Note: Select correct one, see also Vivado Board Part Flow

4. Create hardware description file (.xsa file) and export to prebuilt folder

run on Vivado TCL (Script generates design and export files into "<project folder>\prebuilt\hardware\<short name>")

```
TE::hw_build_design -export_prebuilt
```

> ⓘ Using Vivado GUI is the same, except file export to prebuilt folder.

5. Generate Programming Files(mcs file for QSPI Flash) with Vitis
   a. Run on Vivado TCL:

Script generates applications and bootable files, which are defined in "sw_lib\apps_list.csv"

```
TE::sw_run_vitis -all
```

b. latest "hello_te0717.elf" application should reside in "\firmware\microblaze_0\" now
c. Regenerate Vivado Project or Update Bitfile only, with new "hello_te0717.elf" associated to the MicroBlaze Processor

> ⚠ TCL scripts generate also platform project, this must be done manually in case GUI is used. See Vitis

Launch

Programming

> ⚠ Check Module and Carrier TRMs for proper HW configuration before you try any design.
>
> Reference Design is also available with prebuilt files. It's recommended to use TE prebuilt files for first launch.

Xilinx documentation for programming and debugging: Vivado/Vitis/SDSoC-Xilinx Software Programming and Debugging

Get prebuilt boot binaries

1. Run _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell
2. Press 0 and enter to start "Module Selection Guide"
    a. Select assembly version
    b. Validate selection
    c. Select create and open delivery binary folder

> ⓘ Note: Folder "<project folder>_binaries_<Article Name>" with subfolder "boot_<app name>" for different applications will be generated

QSPI-Boot mode

1. Connect JTAG and power on carrier with module
2. Open Vivado Project with "vivado_open_existing_project_guimode.cmd" or if not created, create with "vivado_create_project_guimode.cmd"

run on Vivado TCL (Script programs BOOT.bin on QSPI flash)

```
TE::pr_program_flash -swapp hello_te0711
```

3. Power your Board OFF and ON or press the RESET button to start the application and see the output in the console

JTAG

Not used on this example.

Usage

1. Prepare HW like described on section Programming
2. Connect UART USB (most cases same as JTAG)
3. Select QSPI as Boot Mode (default on TE0711)

> Note: See TRM of the Carrier, which is used.

4. Power On PCB

   1. FPGA Loads Bitfile from Flash

   2. hello_te0711.elf application starts on MicroBlaze

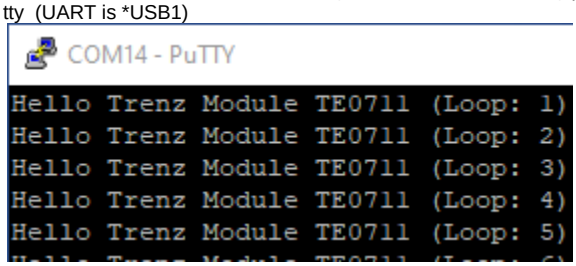
   3. Hello Trenz will be printed on UART console. Also the current CPLD Revision should be printed.

   info: Do not reboot, if Bitfile programming over JTAG is used as programming method.

   a. ## UART

      Open Serial Console (e.g. putty)

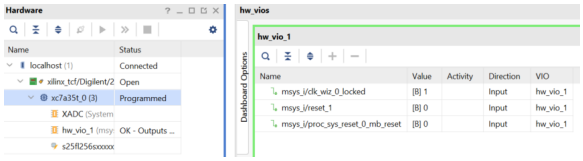
      i. Speed: 9600
      ii. COM Port: Win OS, see device manager, Linux OS see dmesg |grep tty (UART is *USB1)



Vivado HW Manager

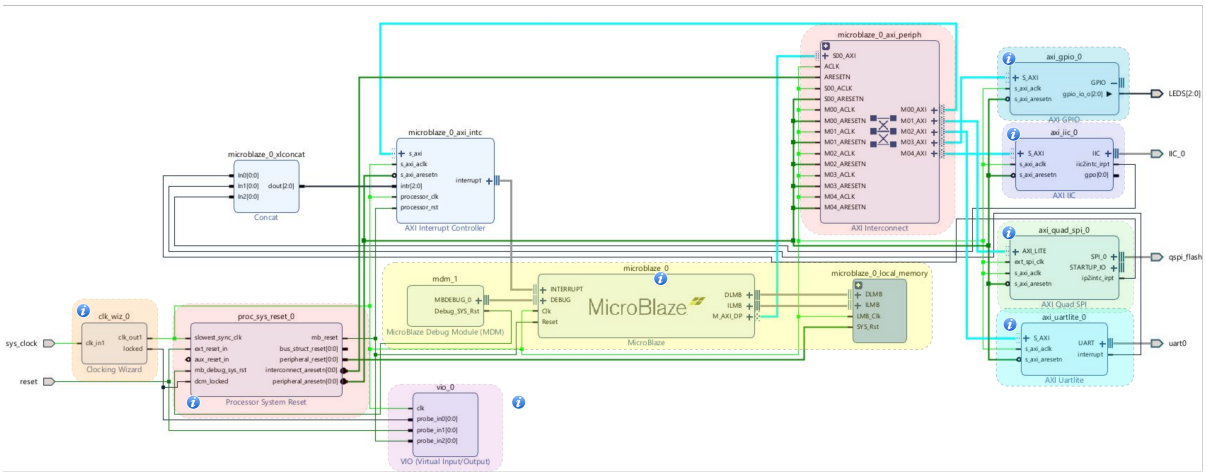
Open Vivado HW-Manager and add VIO signal to dashboard (*.ltx located on prebuilt folder)

- Control:
- Monitoring:
  - Active High External Reset
  - Active High Processor System Reset



System Design - Vivado

Block Design



info overlay

Constraints

Basic module constraints

_i_bitgen_common.xdc

```
#
# Default common settings that do not depend assembly variant
#
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property BITSTREAM.CONFIG.CONFIGRATE 66 [current_design]
set_property CONFIG_VOLTAGE 3.3 [current_design]
set_property CFGBVS VCCO [current_design]
set_property CONFIG_MODE SPIx4 [current_design]
set_property BITSTREAM.CONFIG.SPI_32BIT_ADDR YES [current_design]
set_property BITSTREAM.CONFIG.SPI_BUSWIDTH 4 [current_design]
set_property BITSTREAM.CONFIG.M1PIN PULLNONE [current_design]
set_property BITSTREAM.CONFIG.M2PIN PULLNONE [current_design]
set_property BITSTREAM.CONFIG.M0PIN PULLNONE [current_design]

set_property BITSTREAM.CONFIG.USR_ACCESS TIMESTAMP [current_design]
```

_i_bitgen.xdc

```
set_property BITSTREAM.CONFIG.UNUSEDPIN PULLDOWN [current_design]
```

Design specific constraints

_i_io.xdc

```
set_property PACKAGE_PIN A8 [get_ports {LEDS[0]}]
set_property PACKAGE_PIN L15 [get_ports {LEDS[1]}]
set_property PACKAGE_PIN R17 [get_ports {LEDS[2]}]
set_property IOSTANDARD LVCMOS18 [get_ports {LEDS[0]}]
set_property IOSTANDARD LVCMOS33 [get_ports {LEDS[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {LEDS[2]}]
set_property PULLDOWN true [get_ports reset]

## IIC Interface
set_property PACKAGE_PIN B8 [get_ports IIC_0_sda_io]
set_property PACKAGE_PIN D10 [get_ports IIC_0_scl_io]
set_property IOSTANDARD LVCMOS18 [get_ports IIC_0_scl_io]
set_property IOSTANDARD LVCMOS18 [get_ports IIC_0_sda_io]
```

Software Design - Vitis

For Vitis project creation, follow instructions from:

Vitis

Application

Template location: "<project folder>\sw_lib\sw_apps\"

Hello TE0711

Trenz Hello World example as endless loop. With version 2023.2 the first print is the current CPLD firmware revision (starting from revision 02, older revisions dont support i2c communication between cpld and fpga).

Also LED D1 to D4 are flashed in consecutive order. D1 to D3 are controlled over the GPIO IP Core and D4 over the I2C Interface to the CPLD. (see TE0711 CPLD)

Template location: \sw_lib\sw_apps\hello_te0711

The printed Text and the blinking of the red LED can be modified.

Additional Software

No additional software is needed.

App. A: Change History and Legal Notices

Document Change History

To get content of older revision go to "Change History" of this page and select older document revision number.

Date	Document Revision	Authors	Description
Error rendering macro 'page-info' Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.	v.11	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class	• 2023.2 release

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2022-08-22	v.10	Waldemar Hanemann	• 2021.2 release • document style update
2020-09-02	v.9	John Hartfiel	• 2019.2 release • Docu update
2018-11-30	v.8	John Hartfiel	• correction download link
2017-12-07	v.7	John Hartfiel	• 2017.2 release
--	all	**Error renderi ng macro 'page-info'** Ambiguo	--

us method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between:

		[interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]		

Document change history.

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Error rendering macro 'page-info'

Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]