TE0818 StarterKit

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Overview

Refer to http://wiki.trenz.org/te0818-info for the current online version of this manual and other available documentation.

Key Features

- Vitis/Vivado 2023.2
- TEBF0818
- Linux
- USB
- ETH
- MAC from EEPROM
- PCIe
- SATA
- SD
- I2C
- RGPIO
- Display Port (DP)
- user LED access
- Modified FSBL for Si5345 programming

Revision History

Date	Vivado	Project Built	Authors	Description
2024-03-08	2023.2	TE0818-StarterKit-vivado_2023.2-build_4_20240308103809.zip TE0818-StarterKit_noprebuilt-vivado_2023.2-build_4_20240308103809.zip	Manuela Strücker	• new assembly variants
2023-12-15	2023.2	TE0818-StarterKit-vivado_2023.2-build_3_20231215122410.zip TE0818-StarterKit_noprebuilt-vivado_2023.2-build_3_20231215122410.zip	Manuela Strücker	• 2023.2 release • new assembly variants
2023-08-15	2022.2	TE0818-StarterKit-vivado_2022.2-build_6_20230815120540.zip TE0818-StarterKit_noprebuilt-vivado_2022.2-build_6_20230815120540.zip	Manuela Strücker	• new assembly variants

2023-06-14	2022.2	TE0818-StarterKit-vivado_2022.2-build_2_20230619104156.zip TE0818-StarterKit_noprebuilt-vivado_2022.2-build_2_20230619104156.zip	Manuela Strücker	• 2022.2 release • new assembly variants
2023-02-14	2021.2.1	TE0818-StarterKit_noprebuilt-vivado_2021.2-build_20_20230214112518.zip TE0818-StarterKit-vivado_2021.2-build_20_20230214112518.zip	Manuela Strücker	• new assembly variants
2022-09-12	2021.2.1	TE0818-StarterKit_noprebuilt-vivado_2021.2-build_15_20220912092618.zip TE0818-StarterKit-vivado_2021.2-build_15_20220912092618.zip	Manuela Strücker	• update board part files compatible to Vivado 2021.2.1
2022-05-12	2021.2	TE0818-StarterKit_noprebuilt-vivado_2021.2-build_14_20220512120454.zip TE0818-StarterKit-vivado_2021.2-build_14_20220512120454.zip	Manuela Strücker	• new assembly variant
2022-02-24	2021.2	TE0818-StarterKit_noprebuilt-vivado_2021.2-build_11_20220224094436.zip TE0818-StarterKit-vivado_2021.2-build_11_20220224094436.zip	Manuela Strücker	• bugfix (read MAC from EEPROM)
2022-02-03	2021.2	TE0818-StarterKit_noprebuilt-vivado_2021.2-build_11_20220203074431.zip TE0818-StarterKit-vivado_2021.2-build_11_20220203074431.zip	John Hartfiel	• initial release

Design Revision History

Release Notes and Know Issues

Issues	Description	Workaround	To be fixed version
Xilinx Software	Incompatibility of board files for ZynqMP with eMMC activated between 2021.2 and 2021.2.1 patch, see Xilinx Forum Request	use corresponding board files for the Vivado versions	--

MAC from EEPROM	The MAC address stored in the EEPROM is not read out and initialised correctly during start-up. This is caused by two I2C expanders each switched to the same EEPROM with the same address i2cswitch@73 --> i2c@5 --> reg = <0x50> and i2cswitch@77 --> i2c@4 --> reg = <0x50>	Switching the second I2C expander (i2cswitch@77) to another channel in the fsbl solves the error during the start-up procedure.	**Solved** with 20220224 update

Known Issues

Requirements

Software

Software	Version	Note
Vitis	2023.2	needed, Vivado is included into Vitis installation
PetaLinux	2023.2	needed
Skyworks ClockBuilder Pro	---	optional Si5345A-B-GM is no longer supported by the latest Skyworks ClockBuilder Pro software.

Software

Hardware

Basic description of TE Board Part Files is available on TE Board Part Files.

Complete List is available on "<project folder>\board_files*_board_files.csv"

Design supports following modules:

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMMC	Others	Notes
TE0818-01-9BE21-A	9eg_1e_4gb	REV01	4GB	128MB	NA	NA	NA
TE0818-01-9BE21-AZ	9eg_1e_4gb	REV01	4GB	128MB	NA	NA	NA
TE0818-01-9BI41-X	9eg_1i_8gb	REV01	8GB	128MB	NA	NA	NA
TE0818-01-9GI21-A*	9eg_2i_4gb	REV01	4GB	128MB	NA	NA	NA
TE0818-01-9GI21-AK	9eg_2i_4gb	REV01	4GB	128MB	NA	NA	NA

TE0818-01-9GI81-A	9eg_2i_4gb	REV01	4GB	128MB	NA	NA	NA
TE0818-01-9GI81-AK	9eg_2i_4gb	REV01	4GB	128MB	NA	NA	NA
TE0818-01-BBE21-A	15eg_1e_4gb	REV01	4GB	128MB	NA	NA	NA
TE0818-01-BBE21-AZ	15eg_1e_4gb	REV01	4GB	128MB	NA	NA	NA
TE0818-01-BBE81-A	15eg_1e_4gb	REV01	4GB	128MB	NA	NA	NA
TE0818-01-BBE81-AK	15eg_1e_4gb	REV01	4GB	128MB	NA	NA	NA
TE0818-01-S001	6eg_1e_4gb	REV01	4GB	128MB	NA	NA	without PLL
TE0818-01-S002	9eg_2i_4gb	REV01	4GB	128MB	NA	NA	NA
TE0818-01-S003	9eg_2i_4gb	REV01	4GB	128MB	NA	NA	NA
TE0818-01-T001K	15eg_1e_4gb	REV01	4GB	128MB	NA	NA	NA
TE0818-01-T002K	9eg_2i_4gb	REV01	4GB	128MB	NA	NA	NA
TE0818-02-6BE81-A	6eg_1e_4gb	REV02	4GB	128MB	NA	NA	NA
TE0818-02-6BE81-AK	6eg_1e_4gb	REV02	4GB	128MB	NA	NA	NA
TE0818-02-9BE81-A	9eg_1e_4gb	REV02	4GB	128MB	NA	NA	NA
TE0818-02-9BE81-AK	9eg_1e_4gb	REV02	4GB	128MB	NA	NA	NA
TE0818-02-9GI81-A	9eg_2i_4gb	REV02	4GB	128MB	NA	NA	NA
TE0818-02-9GI81-AK	9eg_2i_4gb	REV02	4GB	128MB	NA	NA	NA
TE0818-02-BBE81-A	15eg_1e_4gb	REV02	4GB	128MB	NA	NA	NA
TE0818-02-BBE81-AK	15eg_1e_4gb	REV02	4GB	128MB	NA	NA	NA
TE0818-02-BGI81-A	15eg_2i_4gb	REV02	4GB	128MB	NA	NA	NA
TE0818-02-BGI81-AK	15eg_2i_4gb	REV02	4GB	128MB	NA	NA	NA
TE0818-02-S002	9eg_1i_8gb	REV02	8GB	128MB	NA	NA	NA

*used as reference

Hardware Modules

Note: Design contains also Board Part Files for TE0818 only configuration, this board part files are not used for this reference design.

Design supports following carriers:

Carrier Model	Notes
TEBF0818*	
TEBT0818	

*used as reference

Hardware Carrier

Additional HW Requirements:

Additional Hardware	Notes
Display Port Monitor	Optional HW Not all monitors are supported, also Adapter to other Standard can make trouble. Design was tested with **DELL U2412M**
USB Keyboard	Optional HW Can be used to get access to console which is show on Display Port
USB Stick	Optional HW USB was tested with USB memory stick
SATA Disk	Optional HW
PCIe Card	Optional HW
ETH cable	Optional HW Ethernet works with DHCP, but can be setup also manually
SD card	with fat32 partition

*used as reference

Additional Hardware

Content

For general structure and usage of the reference design, see Project Delivery - AMD devices

Design Sources

Type	Location	Notes
Vivado	<project folder>\block_design <project folder>\constraints <project folder>\ip_lib <project folder>\board_files	Vivado Project will be generated by TE Scripts
Vitis	<project folder>\sw_lib	Additional Software Template for Vitis and apps_list.csv with settings automatically for Vitis app generation
PetaLinux	<project folder>\os\petalinux	PetaLinux template with current configuration

Design sources

Additional Sources

Type	Location	Notes
SI5345	<project folder>\misc\PLL\	SI5345 Project with current PLL Configuration Si5345A-B-GM is no longer supported by the latest Skyworks Clockbuilder Pro software.
init.sh	<project folder>\misc\sd\	Additional Initialization Script for Linux

Additional design sources

Prebuilt

File	File-Extension	Description
BIF-File	*.bif	File with description to generate Bin-File
BIN-File	*.bin	Flash Configuration File with Boot-Image (Zynq-FPGAs)
BIT-File	*.bit	FPGA (PL Part) Configuration File
Boot Script-File	*.scr	Distro Boot Script file
DebugProbes-File	*.ltx	Definition File for Vivado/Vivado Labtools Debugging Interface
Diverse Reports	---	Report files in different formats
Device Tree	*.dts	Device tree (2 possible, one for u-boot and one for linux)
Hardware-Platform-Description-File	*.xsa	Exported Vivado hardware description file for Vitis and PetaLinux
LabTools Project-File	*.lpr	Vivado Labtools Project File
OS-Image	*.ub	Image with Linux Kernel (On Petalinux optional with Devicetree and RAM-Disk)
Software-Application-File	*.elf	Software Application for Zynq or MicroBlaze Processor Systems

Prebuilt files (only on ZIP with prebuilt content)

Download

Reference Design is only usable with the specified Vivado/Vitis/PetaLinux version. Do never use different Versions of Xilinx Software for the same Project.

Reference Design is available on:

- TE0818 "Starterkit" Reference Design

Design Flow

Reference Design is available with and without prebuilt files. It's recommended to use TE prebuilt files for first launch.

Trenz Electronic provides a tcl based built environment based on Xilinx Design Flow.

See also:

- AMD Development Tools#XilinxSoftware-BasicUserGuides
- Vivado Projects - TE Reference Design
- Project Delivery.

The Trenz Electronic FPGA Reference Designs are TCL-script based project. Command files for execution will be generated with "_create_win_setup.cmd" on Windows OS and "_create_linux_setup.sh" on Linux OS.

TE Scripts are only needed to generate the vivado project, all other additional steps are optional and can also executed by Xilinx Vivado/Vitis GUI. For currently Scripts limitations on Win and Linux OS see: Project Delivery Currently limitations of functionality

Caution! Win OS has a 260 character limit for path lengths which can affect the Vivado tools. To avoid this issue, use Virtual Drive or the shortest possible names and directory locations for the reference design (for example "x:\<project folder>")

1. Run _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell:

_create_win_setup.cmd/_create_linux_setup.sh

```
------------------------Set design paths---------------------------
-- Run Design with: _create_win_setup
-- Use Design Path: <absolute project path>
-------------------------------------------------------------------
------------------------TE Reference
Design--------------------------
-------------------------------------------------------------------
-- (0)  Module selection guide, project creation...prebuilt export...
-- (1)  Create minimum setup of CMD-Files and exit Batch
-- (2)  Create maximum setup of CMD-Files and exit Batch
-- (3)  (internal only) Dev
-- (4)  (internal only) Prod
-- (c)  Go to CMD-File Generation (Manual setup)
-- (d)  Go to Documentation (Web Documentation)
-- (g)  Install Board Files from Xilinx Board Store (beta)
-- (a)  Start design with unsupported Vivado Version (beta)
-- (x)  Exit Batch (nothing is done!)
----
Select (ex.:'0' for module selection guide):
```

2. Press 0 and enter to start "Module Selection Guide"
3. Create project and follow instructions of the product selection guide, settings file will be configured automatically during this process.

- optional for manual changes: Select correct device and Xilinx install path on "design_basic_settings.cmd" and create Vivado project with "vivado_create_project_guimode.cmd"

  > ⚠ Note: Select correct one, see also Vivado Board Part Flow
  >
  > Important: Use Board Part Files, which ends with *_tebf0818

4. Create hardware description file (.xsa file) for PetaLinux project and export to prebuilt folder

   run on Vivado TCL (Script generates design and export files into "<project folder>\prebuilt\hardware\<short name>")

   ```
   TE::hw_build_design -export_prebuilt
   ```

   > ⓘ Using Vivado GUI is the same, except file export to prebuilt folder.

5. Create and configure your PetaLinux project with exported .xsa-file, see PetaLinux KICKstart
   - use TE Template from "<project folder>\os\petalinux"
   - use exported .xsa file from "<project folder>\prebuilt\hardware\<short name>" . **Note:** HW Export from Vivado GUI creates another path as default workspace.
   - The build images are located in the "<plnx-proj-root>/images/linux" directory
6. Configure the **boot.scr** file as needed, see Distro Boot with Boot.scr
7. Generate Programming Files with Vitis
   a. Copy PetaLinux build image files to prebuilt folder
      - copy **u-boot.elf, system.dtb, bl31.elf**, **image.ub** and **boot.scr** from "<plnx-proj-root>/images/linux" to prebuilt folder

        > ⓘ "<project folder>\prebuilt\os\petalinux\<ddr size>" or "<project folder>\prebuilt\os\petalinux\<short name>"

   b. Generate Programming Files

      run on Vivado TCL (Script generates applications and bootable files, which are defined in "test_board\sw_lib\apps_list.csv")

      ```
      TE::sw_run_vitis -all
      TE::sw_run_vitis (optional; Start Vitis from Vivado GUI or start with TE Scripts on Vivado TCL)
      ```

      > ⚠ TCL scripts generate also platform project, this must be done manually in case GUI is used. See Vitis

Generate Programming Files with Petalinux (alternative), see PetaLinux KICKstart

Launch

For basic board setup, LEDs... see: TEBF0818 Getting Started

Programming

> ⚠ Check Module and Carrier TRMs for proper HW configuration before you try any design.
>
> Reference Design is also available with prebuilt files. It's recommended to use TE prebuilt files for first launch.

Xilinx documentation for programming and debugging: Vivado/Vitis/SDSoC-Xilinx Software Programming and Debugging

Get prebuilt boot binaries

1. Run _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell
2. Press 0 and enter to start "Module Selection Guide"
    a. Select assembly version
    b. Validate selection
    c. Select create and open delivery binary folder

> ⓘ Note: Folder "<project folder>_binaries_<Article Name>" with subfolder "boot_<app name>" for different applications will be generated

QSPI-Boot mode

Option for **Boot.bin** on QSPI Flash

1. Connect **JTAG** and power on carrier with module
2. Open Vivado Project with "vivado_open_existing_project_guimode.cmd" or if not created, create with "vivado_create_project_guimode.cmd"

run on Vivado TCL (Script programs BOOT.bin on QSPI flash)
`TE::pr_program_flash -swapp hello_te0818`

3. Set Boot Mode to **QSPI-Boot.**
    - Depends on Carrier, see carrier TRM.
    - TEBF0818 change automatically the Boot Mode to SD, if SD is inserted, optional CPLD Firmware without Boot Mode changing for microSD Slot is available on the download area

SD-Boot mode

1. Copy **image.ub, boot.src** and **Boot.bin** on **SD**
    - use files from "<project folder>_binaries_<Article Name>\boot_linux" from generated binary folder, see: Get prebuilt boot binaries
    - or use prebuilt file location, see "<project folder>\prebuilt\file_location.txt"
2. Set Boot Mode to SD-Boot.
    - Depends on Carrier, see carrier TRM.
3. Insert SD-Card in SD-Slot.

JTAG

Not used on this example.

Usage

1. Prepare HW like described on section Programming
2. Connect UART USB (most cases same as JTAG)
3. Select SD Card as Boot Mode (or QSPI - depending on step 1)

> Note: See TRM of the Carrier, which is used.

> Starting with Petalinux version 2020.1, the industry standard "Distro-Boot" boot flow for U-Boot was introduced, which significantly expands the possibilities of the boot process and has the primary goal of making booting much more standardised and predictable.
> The boot options described above describe the common boot processes for this hardware; other boot options are possible.
> For more information see Distro Boot with Boot.scr

4. (Optional with TEBF0818) Insert PCIe Card (detection depends on Linux driver. Only some basic drivers are installed)
5. (Optional with TEBF0818) Connect SATA Disc
6. (Optional with TEBF0818) Connect Display Port Monitor (List of usable Monitors: https://www.xilinx.com/support/answers/68671.html)
7. (Optional with TEBF0818) Connect Network Cable
8. Power On PCB

    1. ZynqMP Boot ROM loads FSBL from SD/QSPI into OCM,

    2. FSBL init the PS, programs the PL using the bitstream and loads PMU, ATF and U-boot from SD/QSPI into DDR,

    3. U-boot loads Linux (**image.ub**) from SD/QSPI/... into DDR

Linux

1. Open Serial Console (e.g. putty)
    - Speed: 115200
    - select COM Port

    > Win OS, see device manager, Linux OS see dmesg |grep tty (UART is *USB1)

2. Linux Console:

```
# password disabled
petalinux login: root
Password: root
```

> Note: Wait until Linux boot finished

3. You can use Linux shell now.

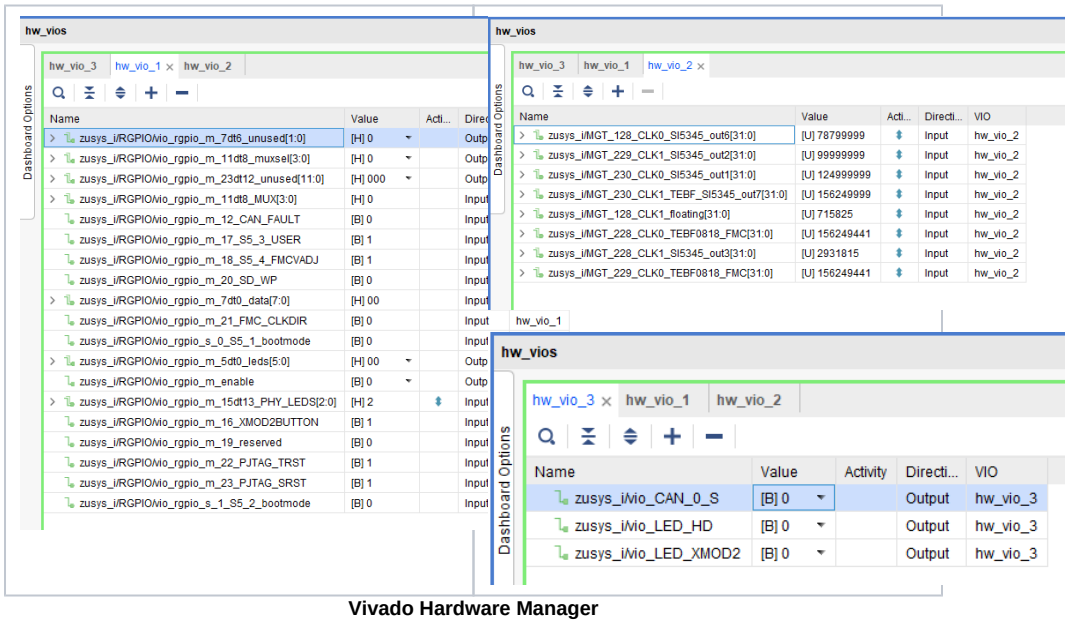
```
i2cdetect -y -r 0        (check I2C 0 Bus, replace 0 with other bus
number is also possible)
dmesg | grep rtc        (RTC check)
udhcpc                                  (ETH0 check)
lsusb                                  (USB check)
lspci              (PCIe check)
```

4. Option Features
    - Webserver to get access to ZynqMP
        - insert IP on web browser to start web interface
    - init.sh scripts
        - add init.sh script on SD, content will be load automatically on startup (template included in "<project folder>\misc\SD")

Vivado HW Manager

Open Vivado HW-Manager and add VIO signal to dashboard (*.ltx located on prebuilt folder)

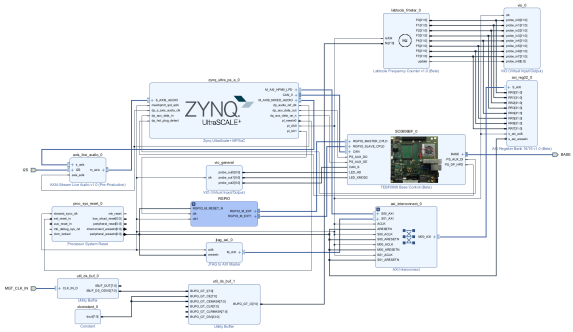
- RGPIO Interface (**Important**: CPLD Firmware REV07 or newer is needed) for Control and Monitoring:
    - Set Enable to send Write date over RGPIO interface.
        - **CPLD** Description: TEBF0818 CPLD
            - Buttons, LEDs, Status...
- Control:
    - LEDs: XMOD 2 (without green dot) and HD LED are accessible.
    - CAN_S



Vivado Hardware Manager

System Design - Vivado

Block Design



Block Design

PS Interfaces

Activated interfaces:

Type	Note
DDR	
QSPI	MIO
SD0	MIO
SD1	MIO
CAN0	EMIO
I2C0	MIO
PJTAG0	MIO
UART0	MIO
GPIO0	MIO
SWDT0..1	
TTC0..3	
GEM3	MIO
USB0	MIO/GTP
PCIe	MIO/GTP
SATA	GTP
Display Port	EMIO/GTP

PS Interfaces

Constraints

Basic module constraints

_i_bitgen.xdc

```
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property BITSTREAM.CONFIG.UNUSEDPIN PULLNONE [current_design]
```

Design specific constraints

_i_io.xdc

```
#System Controller IP
#LED_HD SC0 J3:C13
#LED_XMOD SC17 J3:B19
#CAN RX SC19 J3:B23
#CAN TX SC18 J3:B22
#CAN S  SC16 J3:B18


#HDIO_SC0    J14
set_property PACKAGE_PIN J14 [get_ports BASE_sc0]
#HDIO_SC5    G13
set_property PACKAGE_PIN G13 [get_ports BASE_sc5]
#HDIO_SC6    J15
set_property PACKAGE_PIN J15 [get_ports BASE_sc6]
#HDIO_SC7    K15
set_property PACKAGE_PIN K15 [get_ports BASE_sc7]
#HDIO_SC10   A15
set_property PACKAGE_PIN A15 [get_ports BASE_sc10_io]
#HDIO_SC11   B15
set_property PACKAGE_PIN B15 [get_ports BASE_sc11]
#HDIO_SC12   C13
set_property PACKAGE_PIN C13 [get_ports BASE_sc12]
#HDIO_SC13   C14
set_property PACKAGE_PIN C14 [get_ports BASE_sc13]
#HDIO_SC14   E13
set_property PACKAGE_PIN E13 [get_ports BASE_sc14]
#HDIO_SC15   E14
set_property PACKAGE_PIN E14 [get_ports BASE_sc15]
#HDIO_SC16   A13
set_property PACKAGE_PIN A13 [get_ports BASE_sc16]
#HDIO_SC17   B13
set_property PACKAGE_PIN B13 [get_ports BASE_sc17]
#HDIO_SC18   A14
set_property PACKAGE_PIN A14 [get_ports BASE_sc18]
#HDIO_SC19   B14
set_property PACKAGE_PIN B14 [get_ports BASE_sc19]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc0]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc5]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc6]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc7]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc10_io]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc11]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc12]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc13]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc14]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc15]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc16]
```

```
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc17]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc18]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc19]


# Audio Codec
#LRCLK                  J3:49 B47_L9_N
#BCLK                  J3:51 B47_L9_P
#DAC_SDATA        J3:53 B47_L7_N
#ADC_SDATA        J3:55 B47_L7_P

#LRCLK G14
set_property PACKAGE_PIN G14 [get_ports I2S_lrclk ]
#BCLK G15
set_property PACKAGE_PIN G15 [get_ports I2S_bclk ]
#DAC_SDATA E15
set_property PACKAGE_PIN E15 [get_ports I2S_sdin ]
#ADC_SDATA F15
set_property PACKAGE_PIN F15 [get_ports I2S_sdout ]
set_property IOSTANDARD LVCMOS18 [get_ports I2S_lrclk ]
set_property IOSTANDARD LVCMOS18 [get_ports I2S_bclk ]
set_property IOSTANDARD LVCMOS18 [get_ports I2S_sdin ]
set_property IOSTANDARD LVCMOS18 [get_ports I2S_sdout ]

# MGTs
#   F25  MGT_128_CLK0_P -> U5,45 -> Si5345 -> out6
#   F26  MGT_128_CLK0_N -> U5,44 -> Si5345 -> out6
#   D25  MGT_128_CLK1_P -> B2B,J2-A7 -> floating
#   D26  MGT_128_CLK1_N -> B2B,J2-A6 -> floating

#   R8   MGT_228_CLK0_P -> B2B,J3-B27 -> TEBF0818-01_FMC_J5E-D5
#   R7   MGT_228_CLK0_N -> B2B,J3-B26 -> TEBF0818-01_FMC_J5E-D4
#   N8   MGT_228_CLK1_P -> U5,35 -> Si5345 -> out3
#   N7   MGT_228_CLK1_N -> U5,34 -> Si5345 -> out3

#   L8   MGT_229_CLK0_P -> B2B,J3-C26 -> TEBF0818-01_FMC_J5E-B21
#   L7   MGT_229_CLK0_N -> B2B,J3-C25 -> TEBF0818-01_FMC_J5E-B20
#   J8   MGT_229_CLK1_P -> U5,31 -> Si5345 -> out2
#   J7   MGT_229_CLK1_N -> U5,30 -> Si5345 -> out2

#   G8   MGT_230_CLK0_P -> U5,28 -> Si5345 -> out1
#   G7   MGT_230_CLK0_N -> U5,27 -> Si5345 -> out1
#   E8   MGT_230_CLK1_P -> B2B,J3-D27 -> TEBF0818-01_CLK7_P -> B2B,J2-D5 -
> U5,51 -> Si5345 -> out7
#   E7   MGT_230_CLK1_N -> B2B,J3-D26 -> TEBF0818-01_CLK7_N -> B2B,J2-D6 -
> U5,50 -> Si5345 -> out7

set_property PACKAGE_PIN F25 [get_ports {MGT_CLK_IN_clk_p[0]}]
set_property PACKAGE_PIN D25 [get_ports {MGT_CLK_IN_clk_p[1]}]
set_property PACKAGE_PIN R8  [get_ports {MGT_CLK_IN_clk_p[2]}]
set_property PACKAGE_PIN N8  [get_ports {MGT_CLK_IN_clk_p[3]}]
set_property PACKAGE_PIN L8  [get_ports {MGT_CLK_IN_clk_p[4]}]
set_property PACKAGE_PIN J8  [get_ports {MGT_CLK_IN_clk_p[5]}]
set_property PACKAGE_PIN G8  [get_ports {MGT_CLK_IN_clk_p[6]}]
set_property PACKAGE_PIN E8  [get_ports {MGT_CLK_IN_clk_p[7]}]
```

Software Design - Vitis

For Vitis project creation, follow instructions from:

Vitis

Application

Template location: "<project folder>\sw_lib\sw_apps\"

zynqmp_fsbl

TE modified 2023.2 FSBL

General:

- Modified Files: xfsbl_main.c, xfsbl_hooks.h/.c, xfsbl_board.h/.c (search for 'TE Mod' on source code)
- Add Files: te_xfsbl_hooks.h/.c (for hooks and board)
- General Changes:
    - Display FSBL Banner and Device Name

Module Specific:

- Add Files: all TE Files start with te_*
    - Si5345 Configuration
    - OTG+PCIe Reset over MIO
    - I2C MUX for EEPROM MAC

zynqmp_pmufw

Xilinx default PMU firmware.

hello_te0818

Hello TE0818 is a Xilinx Hello World example as endless loop instead of one console output.

u-boot

U-Boot.elf is generated with PetaLinux. Vitis is used to generate Boot.bin.

Software Design - PetaLinux

For PetaLinux installation and project creation, follow instructions from:

- PetaLinux KICKstart

Config

Start with **petalinux-config** or **petalinux-config --get-hw-description**

Changes:

- select SD default instead of eMMC:
    - CONFIG_SUBSYSTEM_PRIMARY_SD_PSU_SD_1_SELECT=y
- add new flash partition for bootscr and sizing
    - CONFIG_SUBSYSTEM_FLASH_PSU_QSPI_0_BANKLESS_PART0_SIZE=0xA00000

        - CONFIG_SUBSYSTEM_FLASH_PSU_QSPI_0_BANKLESS_PART1_SIZE=0x2000000
        - CONFIG_SUBSYSTEM_FLASH_PSU_QSPI_0_BANKLESS_PART2_SIZE=0x40000
        - CONFIG_SUBSYSTEM_FLASH_PSU_QSPI_0_BANKLESS_PART3_NAME="bootscr"
        - CONFIG_SUBSYSTEM_FLASH_PSU_QSPI_0_BANKLESS_PART3_SIZE=0x80000
- Identification
    - CONFIG_SUBSYSTEM_HOSTNAME="Trenz"
    - CONFIG_SUBSYSTEM_PRODUCT="TE0818_TEBF0818"

U-Boot

Start with **petalinux-config -c u-boot**

Changes:

- MAC from eeprom together with uboot and device tree settings:
    - CONFIG_ENV_OVERWRITE=y
    - CONFIG_NET_RANDOM_ETHADDR is not set
- Boot Modes:
    - CONFIG_QSPI_BOOT=y
    - CONFIG_SD_BOOT=y
    - CONFIG_ENV_IS_IN_FAT is not set
    - CONFIG_ENV_IS_IN_NAND is not set
    - CONFIG_ENV_IS_IN_SPI_FLASH is not set
    - CONFIG_SYS_REDUNDAND_ENVIRONMENT is not set
    - CONFIG_BOOT_SCRIPT_OFFSET=0x2A40000
- Identification
    - CONFIG_IDENT_STRING=" TE0818_TEBF0818"

Change platform-top.h:

```
#no changes
```

Device Tree

project-spec\meta-user\recipes-bsp\device-tree\files\system-user.dtsi

```
 /include/ "system-conf.dtsi"


/*------------------ gtr --------------------*/

//https://xilinx-wiki.atlassian.net/wiki/spaces/A/pages/18841716
/Zynq+Ultrascale+MPSOC+Linux+SIOU+driver

/ {
  refclk3:psgtr_dp_clock {
          compatible = "fixed-clock";
          #clock-cells = <0x00>;
          clock-frequency = <27000000>;
  };

  refclk2:psgtr_pcie_usb_clock {
          compatible = "fixed-clock";
          #clock-cells = <0x00>;
          clock-frequency = <100000000>;
  };
```

```
  refclk1:psgtr_sata_clock {
          compatible = "fixed-clock";
          #clock-cells = <0x00>;
          clock-frequency = <150000000>;
  };

  //refclk0:psgtr_unused_clock {
  //        compatible = "fixed-clock";
  //        #clock-cells = <0x00>;
  //        clock-frequency = <100000000>;
  //};
};

&psgtr {
  clocks = <&refclk1 &refclk2 &refclk3>;
  /* ref clk instances used per lane */
  clock-names = "ref1\0ref2\0ref3";
};



/*------------------ SD --------------------*/
&sdhci0 {
    // disable-wp;
    no-1-8-v;
};

&sdhci1 {
    // disable-wp;
    no-1-8-v;
};


/*------------------- USB --------------------*/
&dwc3_0 {
    status = "okay";
    dr_mode = "host";
    snps,usb3_lpm_capable;
    snps,dis_u3_susphy_quirk;
    snps,dis_u2_susphy_quirk;
    phy-names = "usb2-phy","usb3-phy";
    maximum-speed = "super-speed";
};


/*------------------ ETH PHY --------------------*/
&gem3 {
    /delete-property/ local-mac-address;
    phy-handle = <&phy0>;

    nvmem-cells = <ð0_addr>;
    nvmem-cell-names = "mac-address";

    phy0: phy0@1 {
        device_type = "ethernet-phy";
        reg = <1>;
    };
};
```

```
/*----------------- SATA PHY --------------------*/
&sata {

     ceva,p0-burst-params = <0x13084a06>;
     ceva,p0-cominit-params = <0x18401828>;
     ceva,p0-comwake-params = <0x614080e>;
     ceva,p0-retry-params = <0x96a43ffc>;
     ceva,p1-burst-params = <0x13084a06>;
     ceva,p1-cominit-params = <0x18401828>;
     ceva,p1-comwake-params = <0x614080e>;
     ceva,p1-retry-params = <0x96a43ffc>;

};


/*-------------------- QSPI ----------------------*/
&qspi {
    #address-cells = <1>;
    #size-cells = <0>;
    status = "okay";
    flash0: flash@0 {
        compatible = "jedec,spi-nor";
        reg = <0x0>;
        #address-cells = <1>;
        #size-cells = <1>;

        spi-rx-bus-width = <4>;
        spi-tx-bus-width = <4>;
        spi-max-frequency = <90000000>;
    };
};


/*------------------ I2C --------------------*/
&i2c0 {
    i2cswitch@73 { // u
        compatible = "nxp,pca9548";
        #address-cells = <1>;
        #size-cells = <0>;
        reg = <0x73>;
        i2c-mux-idle-disconnect;
        i2c@0 { // MCLK TEBF0818 SI5338A, 570FBB000290DG_unassembled
            reg = <0>;
        };
        i2c@1 { // SFP TEBF0818 PCF8574DWR
            reg = <1>;
        };
        i2c@2 { // PCIe
            reg = <2>;
        };
        i2c@3 { // SFP1 TEBF0818
            reg = <3>;
        };
        i2c@4 {// SFP2 TEBF0818
            reg = <4>;
        };
        i2c@5 { // TEBF0818 EEPROM
            reg = <5>;
            eeprom: eeprom@50 {
                compatible = "microchip,24aa025", "atmel,24c02";
                reg = <0x50>;
```

```
                #address-cells = <1>;
                #size-cells = <1>;
                eth0_addr: eth-mac-addr@FA {
                  reg = <0xFA 0x06>;
                };
            };
        };
        i2c@6 { // TEBF0818 FMC
            reg = <6>;
        };
        i2c@7 { // TEBF0818 USB HUB
            reg = <7>;
        };
    };
    i2cswitch@77 { // u
        compatible = "nxp,pca9548";
        reg = <0x77>;
        i2c-mux-idle-disconnect;
        i2c@0 { // TEBF0818 PMOD P1
            reg = <0>;
        };
        i2c@1 { // i2c Audio Codec
            reg = <1>;
            /*
            adau1761: adau1761@38 {
                compatible = "adi,adau1761";
                reg = <0x38>;
            };
            */
        };
        i2c@2 { // TEBF0818 Firefly A
            reg = <2>;
        };
        i2c@3 { // TEBF0818 Firefly B
            reg = <3>;
        };
        i2c@4 { //Module PLL Si5338 or SI5345
            reg = <4>;
        };
        i2c@5 { //TEBF0818 CPLD
            reg = <5>;
        };
        i2c@6 { //TEBF0818 Firefly PCF8574DWR
            reg = <6>;
        };
        i2c@7 { // TEBF0818 PMOD P3
            reg = <7>;
        };
    };
};
```

Kernel

Start with **petalinux-config -c kernel**

Changes:

- Only needed to fix JTAG Debug issue:

    - # CONFIG_CPU_FREQ is not set
- Support PCIe memory card
    - CONFIG_NVME_CORE=y
    - CONFIG_BLK_DEV_NVME=y
    - # CONFIG_NVME_MULTIPATH is not set
    - # CONFIG_NVME_VERBOSE_ERRORS is not set
    - # CONFIG_NVME_HWMON is not set
    - # CONFIG_NVME_AUTH is not set
    - CONFIG_NVME_TARGET=y
    - # CONFIG_NVME_TARGET_PASSTHRU is not set
    - # CONFIG_NVME_TARGET_LOOP is not set
    - # CONFIG_NVME_TARGET_FC is not set
    - # CONFIG_NVME_TARGET_TCP is not set
    - # CONFIG_NVME_TARGET_AUTH is not set
    - CONFIG_SATA_AHCI=y
    - CONFIG_SATA_MOBILE_LPM_POLICY=0

Rootfs

Start with **petalinux-config -c rootfs**

Changes:

- For web server app:
    - CONFIG_busybox-httpd=y
- For additional test tools only:
    - CONFIG_i2c-tools=y
    - CONFIG_packagegroup-petalinux-utils=y (util-linux,cpufrequtils,bridge-utils,mtd-utils, usbutils,pciutils,canutils,i2c-tools,smartmontools,e2fsprogs)
- For auto login:
    - CONFIG_imagefeature-serial-autologin-root=y

FSBL patch (alternative for vitis fsbl trenz patch)

See "<project folder>\os\petalinux\project-spec\meta-user\recipes-bsp\embeddedsw"

> ⚠ te_* files are identical to files in "<project folder>\sw_lib\sw_apps\zynqmp_fsbl\src" except for the PLL files (SI5345) which depend on PLL revision. The PLL files may have to be copied again manually into the appropriate petalinux folder "<project folder>\os\petalinux\project-spec\meta-user\recipes-bsp\embeddedsw\fsbl-firmware\git\lib\sw_apps\zynqmp_fsbl\src"

Applications

See "<project folder>\os\petalinux\project-spec\meta-user\recipes-apps\"

startup

Script App to load init.sh from SD Card if available.

webfwu

Webserver application suitable for ZynqMP access. Need busybox-httpd

Additional Software

SI5345

File location "<project folder>\misc\PLL\Si5345_*\Si5345-*.slabtimeproj"

General documentation how you work with this project will be available on Si5345

Si5345A-B-GM is no longer supported by the latest Skyworks Clockbuilder Pro software.

App. A: Change History and Legal Notices

Document Change History

To get content of older revision go to "Change History" of this page and select older document revision number.

Date	Document Revision	Authors	Description
Error rendering macro 'page-info' Ambiguous method overloading for method jdk.proxy241.$Proxy3496#hasContentLevelPermission	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy241.$Proxy3496#hasContentLevelPermission	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy241.$Proxy3496#hasContentLevelPermission	• new assembly variants

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class com. atlassian . confluence.core. ContentEntityObject] [interface com. atlassian .user. User, class java. lang. String, class com. atlassian . confluence.core. ContentEntityObject]	class com. atlassian . confluence.core. ContentEntityObject] [interface com. atlassian .user. User, class java. lang. String, class com. atlassian . confluence.core. ContentEntityObject]	class com. atlassian . confluence.core. ContentEntityObject] [interface com. atlassian .user. User, class java. lang. String, class com. atlassian . confluence.core. ContentEntityObject]	
2023-12-18	v.22	Thomas Friedrich	• 2023.2 release • new assembly variants
2023-06-21	v.16	Manuela Strücker	• 2022.2 release • new assembly variants
2023-04-13	v.14	Manuela Strücker	• new assembly variants

2022-11-21	v.11	Manuela Strücker	• update board part files compatible to Vivado 2021.2.1
2022-09-06	v.9	Manuela Strücker	• new assembly variant
2022-03-10	v.6	Manuela Strücker	• update chapter QSPI-Boot mode • update chapter Usage • update SI5345
2022-02-24	v.3	Manuela Strücker	• bugfix (read MAC from EEPROM)
2022-02-03	v.2	John Hartfiel	• initial release
--	all	**Error renderi ng macro 'page-info'** Ambiguo us method overload ing for method jdk. proxy24 1.$Proxy 3496#ha sConten tLevelPe rmission . Cannot resolve	--

which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian

		. confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	

Document change history.

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Error rendering macro 'page-info'

Ambiguous method overloading for method jdk.proxy241.$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]