TE0710 CPLD

Table of contents

Overview

Firmware for PCB.**CPLD** with designator **U4**. CPLD Device in Chain: LCMX02-256HC

Feature Summary

- JTAG routing
- Reset
- LED sequencing
- USER IO
- I2C Interface

Firmware Revision and supported PCB Revision

See Document Change History

Product Specification

Port Description

Name	Direction	Pin	Pullup/down	Bank Power	Description
DONE	in	13	UP	LVCMOS33	FPGA DONE signal
EN1	in	16	UP	LVCMOS33	B2B Enable Pin - low active
F_TCK	out	28	-	LVCMOS33	JTAG FPGA
F_TDI	out	27	-	LVCMOS33	JTAG FPGA
F_TDO	in	23	-	LVCMOS33	JTAG FPGA
F_TMS	out	25	-	LVCMOS33	JTAG FPGA
JTAGSEL	in	26	NONE	LVCMOS33	Enable JTAG access to CPLD for Firmware update (zero: JTAG routed to module, one: CPLD access)
BOOTMODE	in	11	UP	LVCMOS33	B2B Boot Mode Pin
NOSEQ	in	12	UP	LVCMOS33	B2B NOSEQ Pin
PG_ALL	in	10	UP	LVCMOS33	Power good - low active, from power monitor U23
PGOOD	out	14	UP	LVCMOS33	B2B PGOOD
PROG_B	out	17	UP	LVCMOS33	FPGA PROG_B Reset

SC_nRST	in	8	UP	LVCMOS33	B2B Reset - low active
SYSLED1	out	9	NONE	LVCMOS33	Green LED D2
SYSLED2	out	5	NONE	LVCMOS33	Red LED D1
TCK	in	30	NONE	LVCMOS33	JTAG B2B
TDI	in	32	DOWN	LVCMOS33	JTAG B2B
TDO	out	1	NONE	LVCMOS33	JTAG B2B
TMS	in	29	DOWN	LVCMOS33	JTAG B2B
ULI_2	out	20	UP	LVCMOS15	FPGA Bank 35 Pin J5 - I2C CLOCK Pin to FPGA
ULI_CPLD	out	4	NONE	LVCMOS33	J1 (Ultra Small Surface Mount Coax)
ULI_SYSTEM	in	21	UP	LVCMOS15	FPGA Bank 35 Pin G3 - I2C DATA Pin to FPGA or input for UFL

Functional Description

JTAG

JTAG signals routed directly through the CPLD to FPGA. Access between CPLD and FPGA can be multiplexed via *JTA GEN* (logical one for CPLD, logical zero for FPGA) on JM1-89.

Reset

PROG_B is triggered by *SC_nRST* or *PG_ALL* or *EN1* after power on delay.

Power

PGOOD is '0' when *PG_ALL or EN1* is '0', else high impedance.

USER IO

Various signals are connected to an I2C register.

I2C GPIO_input register Bit 15 downto Bit 9 contain *SC_nRST*, *BOOTMODE*, *PGOOD*, *EN1*, *DONE*, *PG_ALL* and *NOS EQ*.

Their state can be read from FPGA side over I2C.

ULI_SYSTEM serves as the I2C data pin but is also connected to *ULI_CPLD*.

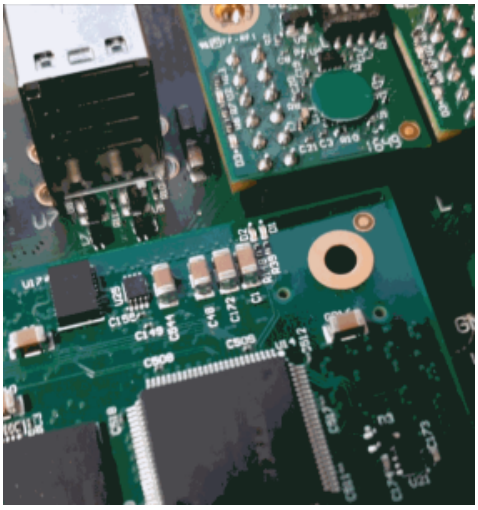
USER IO

MODE_SC1 is connected to a I2C Register bit. GPIO_input(18). Its state can be read from FPGA side over I2C.

UIO is connected to *UFL* but also serves as the I2C data pin.

LED

RED LED D1 (*SYSLED2*) shows a certain blinking pattern in case one of the status signals is active, otherwise it can be controlled via I2C from FPGA side or is simply OFF.

Blink sequence	Priority	Condition	Description
******** 	highest	SC_nRST= LOW (low active)	external reset from carrier is pressed
*******o			blink sequence not used
******oo			blink sequence not used
*****ooo		PG_ALL is zero	One of the power rails of the internal Voltages DCDCs is down
****oooo		EN1 is zero	B2B enable Pin is active (low active), coming from the carrier
***ooooo			blink sequence not used
**oooooo			blink sequence not used

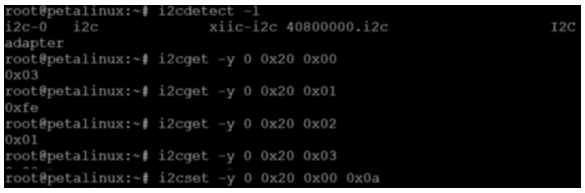
*ooooooo  		DONE = '0'	FPGA not programmed. No design on QSPI Flash?
continuously ON	lowest	software controlled command via I2C Interface. LED = GPIO_output (1) when GPIO_output(0) = 0	Set bit GPIO_output(0) LOW to control the LED with GPIO_output(1).
continuously OFF			If none of the above condition is met

GREEN LED D2 (*SYSLED1*) software controlled command via I2C Interface or is simply OFF.

Blink sequence	Condition	Description
continuously ON	software controlled command via I2C Interface. LED = GPIO_output(3) when GPIO_output(2) = 0	Set bit GPIO_output(2) LOW to control the LED with GPIO_output(3).
continuously OFF		If none of the above condition is met

I2C Interface

This subsystem provides 2 x 32-bit (segmented in eight 8-bit) of general purpose parallel input and output (I/O) expansion for the I2C bus protocol. Address of this I2C device is 0x20. This module contains eight 8-bit registers for reading and writing (GPIO_input[7:0] to GPIO_input[31:24] and GPIO_output[7:0] to GPIO_output[31:24]) separately with address 0x00 to 0x03. These registers can be accessed with I2C commands on a standalone application or, more simply, from petalinux running on the Microblaze. Refer to TE0710 reference design (test board).



Four registers can be read and four can be written.

GPIO_input(7 downto 0)	readable	0x00	contains the CPLD Firmware Revision (not the PCB revision)
GPIO_input(15 downto 8)	readable	0x01	*SC_nRST*, *BOOTMODE*, *PGOOD*, *EN1*, *DONE*, *PG_ALL, NOSEQ, '0'*
GPIO_input(23 downto 16)	readable	0x02	contains: NOSEQ state in bit 16.
GPIO_input(31 downto 24)	readable	0x03	empty
GPIO_output(7 downto 0)	writeable	0x00	Bit 1 to 3 are mapped to SYSLED1 and SYSLED2. Write '1' to Bit 1 and Bit 3 to turn on the LED D1 and D2.
GPIO_output(15 downto 8)	writeable	0x01	not mapped
GPIO_output(23 downto 16)	writeable	0x02	Bit 16 is mapped to NOSEQ if no reset occurs
GPIO_output(31 downto 24)	writeable	0x03	not mapped

Appx. A: Change History and Legal Notices

Revision Changes

changes Firmware REV02(old version) to REV03:

- Signals are renamed according to the schematic.
- NOSEQ pin is added.
- LED function changed. New blinking pattern for critical signal states
- I2C to GPIO slave added
- SC_nRST, BOOTMODE, PGOOD, EN1, DONE, PG_ALL, NOSEQ signals can be read from I2C
- CPLD_REVISION as generic parameter added
- NOSEQ defined as INOUT
- ULI_SYSTEM and ULI_2 pins defined as I2C pins. Added PullUps for I2C. ULI_SYSTEM is still also connected to ULI_CPLD

Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

Date	Document Revision	CPLD Firmware Revision	Supported PCB Revision	Authors	Description	Firmware Release

Error r Ambigu	**ge-info'** **Error rendering macro 'page-info'** ding for method jdk.proxy279.$Proxy4022#h Ambiguous method overloading for method jdk.pr	REV03	REV03	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPe	• REV02, Firmware released 2024-02-15	• SC-PGM-TE0710-03_SC0710-03_2024021 5.zip
22 Sept 2022	v.5	REV01	REV02	John Hartfiel	• some typo • Newer Preliminary CPLD version with some bugfixes for TE0706 usage: Design Note 20210519 TE0710-02 CPLD Firmware	
23 Mar 2018	v.3	REV01	REV02	John Hartfiel	• REV01 , Firmware released 2015-04-17	
2018-03-21	v.1	REV01	REV02	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPe	• Initial release	
	All			**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPe		

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Error rendering macro 'page-info'

Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]