TEC0330 CPLD beta

Teblerafecontents

Firmware for PCB CPLD with designator U5: LCMX02-1200HC

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Port Description

Name / opt. VHD Name	Direction	Pin	Pullup/Down	Bank Power	Description
Button	in	77		LVCMOS33	Button S2 active low
LED1	out	76		LVCMOS33	green LED D1
LTM1_ALERT	in	65		LVCMOS33	Control Interface to DC- DC converters U3 and U4 / curr ently_not_used
LTM2_ALERT	in	64		LVCMOS33	Control Interface to DC- DC converters U3 and U4 / curr ently_not_used
LTM_SCL	out	67		LVCMOS33	Control Interface to DC- DC converters U3 and U4 - DC DC regulator LT M4676 I2C
LTM_SDA	inout	66		LVCMOS33	Control Interface to DC- DC converters U3 and U4 - DC DC regulator LT M4676 I2C
PLL_SCL	out	14		LVCMOS18	PLL SI5338 I2C Interface
PLL_SDA	inout	15		LVCMOS18	PLL SI5338 I2C Interface

DDR3_SCL	out	43	LVCMOS33	DDR3 I2C Interface
DDR3_SDA	inout	42	LVCMOS33	DDR3 I2C Interface
FMC_SCL	out	49	LVCMOS33	FMC Connector I2C Interface
FMC_SDA	inout	48	LVCMOS33	FMC Connector I2C Interface
EN_1V8	out	58	LVCMOS33	Power-on sequence and monitoring - ENABLE Power regulator EP53F8QI U20
PG_1V8	in	59	LVCMOS33	Power-on sequence and monitoring - Power Good Power regulator EP53F8QI U20
EN_1V8_FMC	out	60	LVCMOS33	Power-on sequence and monitoring - ENABLE Power regulator EN6347QI U7
PG_1V8_FMC	in	61	LVCMOS33	Power-on sequence and monitoring - Power Good Power regulator EN6347QI U7
EN_3V3	out	51	LVCMOS33	Power-on sequence and monitoring - ENABLE Power regulator EN634 7QI U15
PG_3V3	in	57	LVCMOS33	Power-on sequence and monitoring - Power Good Power regulator EP53F8QI U15
FEX_0_P	in	1	LVCMOS18	goes to LED
FEX_0_N	out	2	LVCMOS18	FMC Power Good - FMC_PG_M2C
FEX_1_P	in	3	LVCMOS18	Control interface to clock synthesizer U9 - LMK_SCK
FEX_1_N	in	4	LVCMOS18	Control interface to clock synthesizer U9 - LMK_SDIO
FEX_2_P	out	9	LVCMOS18	Control interface to clock synthesizer U9 - LMK

FEX_2_N	in	10	LVCMOS18	Control interface to clock synthesizer U9 - LMK
FEX_3_P	in	12	LVCMOS18	Control interface to clock synthesizer U9 - LMK_CS
FEX_3_N	in	13	LVCMOS18	Control interface to clock synthesizer U9 - LMK_SYNC
FEX_4_N	out	21	LVCMOS18	PCIe_RST
FEX_4_P	in	20	LVCMOS18	Control interface to clock synthesizer U9 - LMK_RESET
FEX_5_P	out	16	LVCMOS18	F1SENSE
FEX_5_N	in	17	LVCMOS18	F1PWM
FEX_DIR	out	18	LVCMOS18	FMC_PRESENT
EX0_P		84	LVCMOS33	User I/O / curren tly_not_used
EX0_N		83	LVCMOS33	User I/O / curren tly_not_used
EX1_P		88	 LVCMOS33	User I/O / curren tly_not_used
EX1_N		87	LVCMOS33	User I/O / curren tly_not_used
EX2_P		97	LVCMOS33	User I/O / curren tly_not_used
EX2_N		96	 LVCMOS33	User I/O / curren tly_not_used
EX3_P		40	 LVCMOS33	User I/O / curren tly_not_used
EX3_N		41	 LVCMOS33	User I/O / curren tly_not_used
EX4_P		29	 LVCMOS33	User I/O / curren tly_not_used
EX4_N		30	 LVCMOS33	User I/O / curren tly_not_used
PCIe_RST_in	in	37	LVCMOS33	PCIe control line RESET
LMK_CS	out	53	LVCMOS33	Control interface to clock synthesizer U9 - FEX_3_P
LMK_SCK	out	74	LVCMOS33	Control interface to clock synthesizer U9 - FEX_1_P
LMK_SDIO	inout	75	LVCMOS33	Control interface to clock synthesizer U9 - FEX_1_N when FEX_2_N='0' else 'Z';

	LMK_RESET	out	54	LVCMOS33	Control interface to clock synthesizer U9 - FEX_4_P
	LMK_SYNC	out	52	LVCMOS33	Control interface to clock synthesizer U9 - FEX_3_N
	LMK_STAT0	inout	62	LVCMOS33	Control interface to clock synthesizer U9 / currently_not_us ed
	LMK_STAT1	inout	63	LVCMOS33	Control interface to clock synthesizer U9 / currently_not_us ed
	FPGA_IIC_SCL	in	25	LVCMOS18	FPGA I2C Interface
	FPGA_IIC_SDA	out	24	LVCMOS18	FPGA I2C Interface
	FPGA_IIC_DIR	in	19	LVCMOS18	FPGA I2C Interface
	F1PWM	out	98	LVCMOS33	Fan PWM control J4
F1SENSE		in	99	LVCMOS33	Fan PWM control J4
	FMC_PG_C2M	out	69	LVCMOS33	FMC Connector Control lines
	FMC_PG_M2C	in	68	LVCMOS33	FMC Connector Control lines
	FMC_PRESENT	in	70	LVCMOS33	FMC Connector Control lines
	DONE	in	7	LVCMOS18	FPGA programming control and state
	PROG_B	out	8	LVCMOS18	FPGA programming control and state
	dummy	out	34	LVCMOS33	dummy pin - not connected

Functional Description

More information can be found in the TEC0330 TRM.

Power

EN_1V8, EN_3V3 and EN_FMC_VADJ will be set simultaneously to '1' at start-up.

PG signals will not be evaluated.

Reset

PROG_B is '0' when Button S2 is pressed, otherwise '1'.

LED

LED	STATUS	Condition	User defined
LED1 D1 (Green)	ON	Button S2 Pressed	
LED1 D1 (Green)	Blink fast	Button S2 not pressed, DONE=0	
LED1 D1 (Green)	FEX_0_P	Button S2 not pressed, DONE=1	FEX_0_P

Appx. A: Change History

Revision Changes

Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

Date		Document Revision	CPLD Firmware Revision	Supported PCB Revision	Authors	Description	
			REV01	REV05		Initial release	
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Appx. B: Legal Notices

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REACH, RoHS and WEEE

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Users of electrical and electronic equipment in private households are required not to dispose of waste electrical and electronic equipment as unsorted municipal waste and to collect such waste electrical and electronic equipment separately. By the 13 August 2005, Member States shall have ensured that systems are set up allowing final holders and distributors to return waste electrical and electronic equipment at least free of charge. Member States shall ensure the availability and accessibility of the necessary collection facilities. Separate collection is the precondition to ensure specific treatment and recycling of waste electrical and electronic equipment and is necessary to achieve the chosen level of protection of human health and the environment in the European Union. Consumers have to actively contribute to the success of such collection and the return of waste electrical and electronic equipment. Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.

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Ambiguous method overloading for method jdk. proxy241.\$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user. ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core. ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class