

TEC0330 CPLD beta

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Firmware for PCB CPLD with designator U5: LCMX02-1200HC

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Port Description

Name / opt. VHD Name	Direction	Pin	Pullup/Down	Bank Power	Description
Button	in	77		LVC MOS33	Button S2 active low
LED1	out	76		LVC MOS33	green LED D1
LTM1_ALERT	in	65		LVC MOS33	Control Interface to DC-DC converters U3 and U4 / currently_not_used
LTM2_ALERT	in	64		LVC MOS33	Control Interface to DC-DC converters U3 and U4 / currently_not_used
LTM_SCL	out	67		LVC MOS33	Control Interface to DC-DC converters U3 and U4 - DC DC regulator LT M4676 I2C
LTM_SDA	inout	66		LVC MOS33	Control Interface to DC-DC converters U3 and U4 - DC DC regulator LT M4676 I2C
PLL_SCL	out	14		LVC MOS18	PLL SI5338 I2C Interface
PLL_SDA	inout	15		LVC MOS18	PLL SI5338 I2C Interface

DDR3_SCL	out	43		LVC MOS33	DDR3 I2C Interface
DDR3_SDA	inout	42		LVC MOS33	DDR3 I2C Interface
FMC_SCL	out	49		LVC MOS33	FMC Connector I2C Interface
FMC_SDA	inout	48		LVC MOS33	FMC Connector I2C Interface
EN_1V8	out	58		LVC MOS33	Power-on sequence and monitoring - ENABLE Power regulator EP53F8QI U20
PG_1V8	in	59		LVC MOS33	Power-on sequence and monitoring - Power Good Power regulator EP53F8QI U20
EN_1V8_FMC	out	60		LVC MOS33	Power-on sequence and monitoring - ENABLE Power regulator EN6347QI U7
PG_1V8_FMC	in	61		LVC MOS33	Power-on sequence and monitoring - Power Good Power regulator EN6347QI U7
EN_3V3	out	51		LVC MOS33	Power-on sequence and monitoring - ENABLE Power regulator EN6347QI U15
PG_3V3	in	57		LVC MOS33	Power-on sequence and monitoring - Power Good Power regulator EP53F8QI U15
FEX_0_P	in	1		LVC MOS18	goes to LED
FEX_0_N	out	2		LVC MOS18	FMC Power Good - FMC_PG_M2C
FEX_1_P	in	3		LVC MOS18	Control interface to clock synthesizer U9 - LMK_SCK
FEX_1_N	in	4		LVC MOS18	Control interface to clock synthesizer U9 - LMK_SDIO
FEX_2_P	out	9		LVC MOS18	Control interface to clock synthesizer U9 - LMK

FEX_2_N	in	10		LVC MOS18	Control interface to clock synthesizer U9 - LMK
FEX_3_P	in	12		LVC MOS18	Control interface to clock synthesizer U9 - LMK_CS
FEX_3_N	in	13		LVC MOS18	Control interface to clock synthesizer U9 - LMK_SYNC
FEX_4_N	out	21		LVC MOS18	PCIe_RST
FEX_4_P	in	20		LVC MOS18	Control interface to clock synthesizer U9 - LMK_RESET
FEX_5_P	out	16		LVC MOS18	F1SENSE
FEX_5_N	in	17		LVC MOS18	F1PWM
FEX_DIR	out	18		LVC MOS18	FMC_PRESENT
EX0_P		84		LVC MOS33	User I/O / currently_not_used
EX0_N		83		LVC MOS33	User I/O / currently_not_used
EX1_P		88		LVC MOS33	User I/O / currently_not_used
EX1_N		87		LVC MOS33	User I/O / currently_not_used
EX2_P		97		LVC MOS33	User I/O / currently_not_used
EX2_N		96		LVC MOS33	User I/O / currently_not_used
EX3_P		40		LVC MOS33	User I/O / currently_not_used
EX3_N		41		LVC MOS33	User I/O / currently_not_used
EX4_P		29		LVC MOS33	User I/O / currently_not_used
EX4_N		30		LVC MOS33	User I/O / currently_not_used
PCIe_RST_in	in	37		LVC MOS33	PCIe control line RESET
LMK_CS	out	53		LVC MOS33	Control interface to clock synthesizer U9 - FEX_3_P
LMK_SCK	out	74		LVC MOS33	Control interface to clock synthesizer U9 - FEX_1_P
LMK_SDIO	inout	75		LVC MOS33	Control interface to clock synthesizer U9 - FEX_1_N when FEX_2_N='0' else 'Z';

LMK_RESET	out	54		LVC MOS33	Control interface to clock synthesizer U9 - FEX_4_P
LMK_SYNC	out	52		LVC MOS33	Control interface to clock synthesizer U9 - FEX_3_N
LMK_STAT0	inout	62		LVC MOS33	Control interface to clock synthesizer U9 / currently_not_used
LMK_STAT1	inout	63		LVC MOS33	Control interface to clock synthesizer U9 / currently_not_used
FPGA_IIC_SCL	in	25		LVC MOS18	FPGA I2C Interface
FPGA_IIC_SDA	out	24		LVC MOS18	FPGA I2C Interface
FPGA_IIC_DIR	in	19		LVC MOS18	FPGA I2C Interface
F1PWM	out	98		LVC MOS33	Fan PWM control J4
F1SENSE	in	99		LVC MOS33	Fan PWM control J4
FMC_PG_C2M	out	69		LVC MOS33	FMC Connector Control lines
FMC_PG_M2C	in	68		LVC MOS33	FMC Connector Control lines
FMC_PRESENT	in	70		LVC MOS33	FMC Connector Control lines
DONE	in	7		LVC MOS18	FPGA programming control and state
PROG_B	out	8		LVC MOS18	FPGA programming control and state
dummy	out	34		LVC MOS33	dummy pin - not connected

Functional Description

More information can be found in the TEC0330 TRM.

Power

EN_1V8, EN_3V3 and EN_FMC_VADJ will be set simultaneously to '1' at start-up.

PG signals will not be evaluated.

Reset

PROG_B is '0' when Button S2 is pressed, otherwise '1'.

LED

LED	STATUS	Condition	User defined
LED1 D1 (Green)	ON	Button S2 Pressed	---
LED1 D1 (Green)	Blink fast	Button S2 not pressed, DONE=0	---
LED1 D1 (Green)	FEX_0_P	Button S2 not pressed, DONE=1	FEX_0_P

Appx. A: Change History

Revision Changes

Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

Date	Document Revision	CPLD Firmware Revision	Supported PCB Revision	Authors	Description
		REV01	REV05		<ul style="list-style-type: none">Initial release
Error rendering macro 'page-info'	Error rendering macro 'page-info'			Error rendering macro 'page-info'	
Ambiguous method overloading for method jdk.proxy241.\$Proxy3496#hasContentLevel	Ambiguous method overloading for method jdk.proxy241.\$Proxy3496#hasContentLevel			Ambiguous method overloading for method jdk.proxy241.\$Proxy3496#hasContentLevel	
	All				<ul style="list-style-type: none">Error rendering macro 'page-info'Ambiguous method overloading for method jdk.proxy241.\$Proxy3496#hasContentLevel

Appx. B: Legal Notices

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Please also note our data protection declaration at <https://www.trenz-electronic.de/en/Data-protection-Privacy>

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REACH, RoHS and WEEE

REACH

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Users of electrical and electronic equipment in private households are required not to dispose of waste electrical and electronic equipment as unsorted municipal waste and to collect such waste electrical and electronic equipment separately. By the 13 August 2005, Member States shall have ensured that systems are set up allowing final holders and distributors to return waste electrical and electronic equipment at least free of charge. Member States shall ensure the availability and accessibility of the necessary collection facilities. Separate collection is the precondition to ensure specific treatment and recycling of waste electrical and electronic equipment and is necessary to achieve the chosen level of protection of human health and the environment in the European Union. Consumers have to actively contribute to the success of such collection and the return of waste electrical and electronic equipment. Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.

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Error rendering macro 'page-info'

Ambiguous method overloading for method jdk.

proxy241.\$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]