TE0818 TRM

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Overview

The Trenz Electronic TE0818 is an industrial grade MPSoC SOM integrating an AMD Zynq UltraScale+ MPSoC, DDR4 SDRAM with 64-Bit width data bus connection, SPI Boot Flash memory for configuration and operation, transceivers and powerful switch-mode power supplies for all on-board voltages. A large number of configurable I/Os is provided via rugged high-speed stacking connections in a compact 5.2 cm x 7.6 cm form factor.

Refer to http://trenz.org/te0818-info for the current online version of this manual and other available documentation.

Key Features

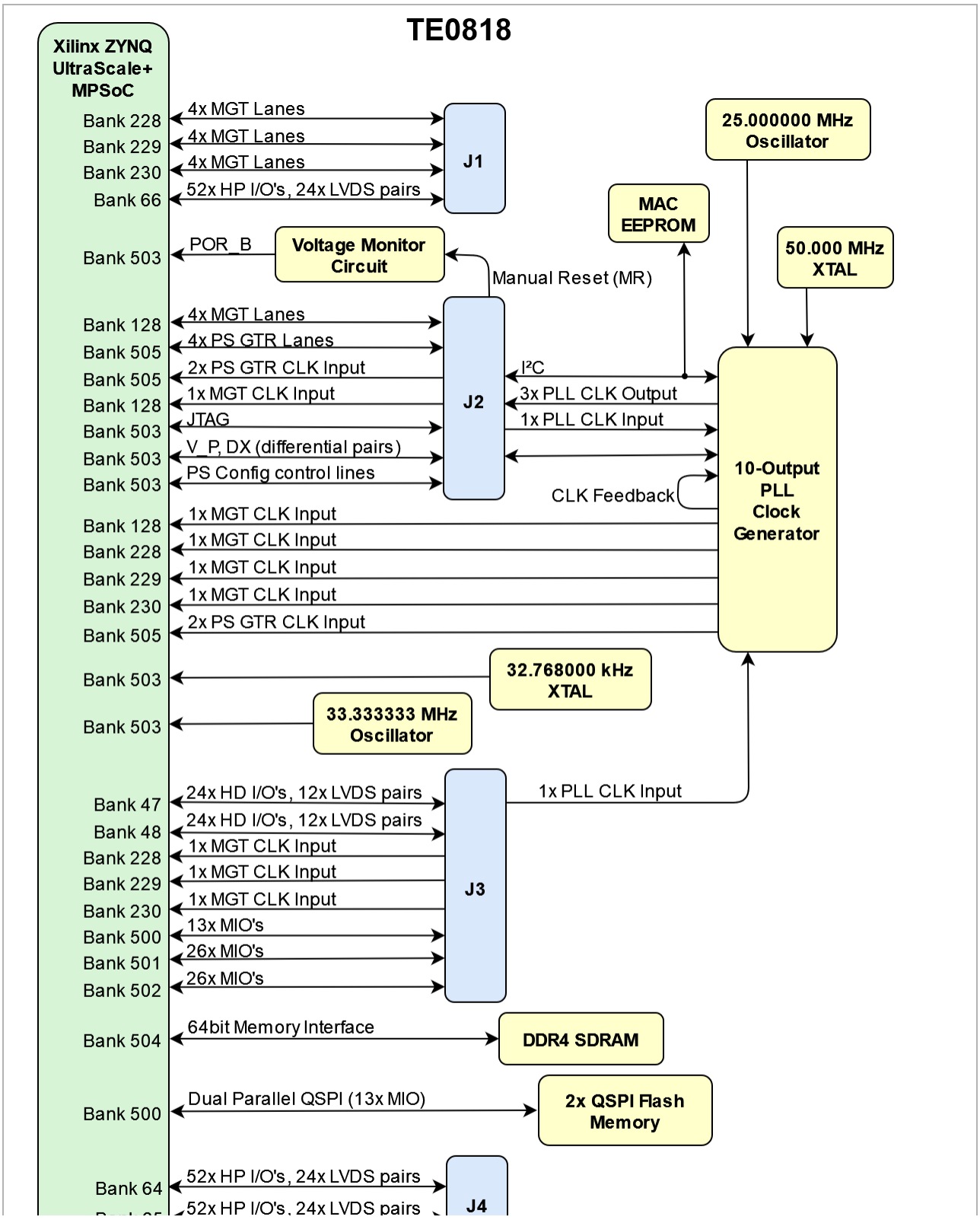
- **SoC**
  - Device: ZU6 / ZU9 / ZU15 [1]
  - Engine: CG / EG [1]
  - Speedgrade: -1 / -2 [1]
  - Temperature Range: Extended / Industrial [1]
  - Package: FFVC900
- **RAM/Storage**
  - 4 GByte DDR4 SDRAM [2]
  - 2 x 64 MByte Serial Flash [3]
  - EEPROM with MAC address
- **On Board**
  - Oscillator
- **Interface**
  - 4 x B2B Connector (ADM6)
    - up to 204 PL IO
      - HP: 156
      - HD: 48
    - up to 65 PS MIO
    - 4 GTR
    - 1 GTH
    - I2C, JTAG, CONFIG
- **Power**
  - 3.3 V Power Supply via B2B Connector needed [4].
- **Dimension**
  - 76 mm x 52 mm
- **Notes**

[1] Please, take care of the possible assembly options. Furthermore, check whether the power supply is powerful enough for your FPGA design.

[2] Up to 32 GByte are possible with a maximum bandwidth of 2400 MBit/s.

[3] Please, take care of the possible assembly options.

[4] Dependent on the assembly option a higher input voltage may be possible


TE0818
Xilinx ZYNQ UltraScale+ MPSoC
Bank 228
Bank 229
Bank 230
Bank 66
Bank 503
Bank 128
Bank 505
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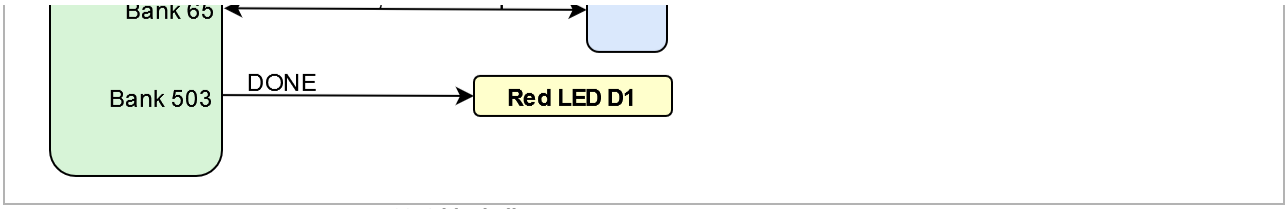
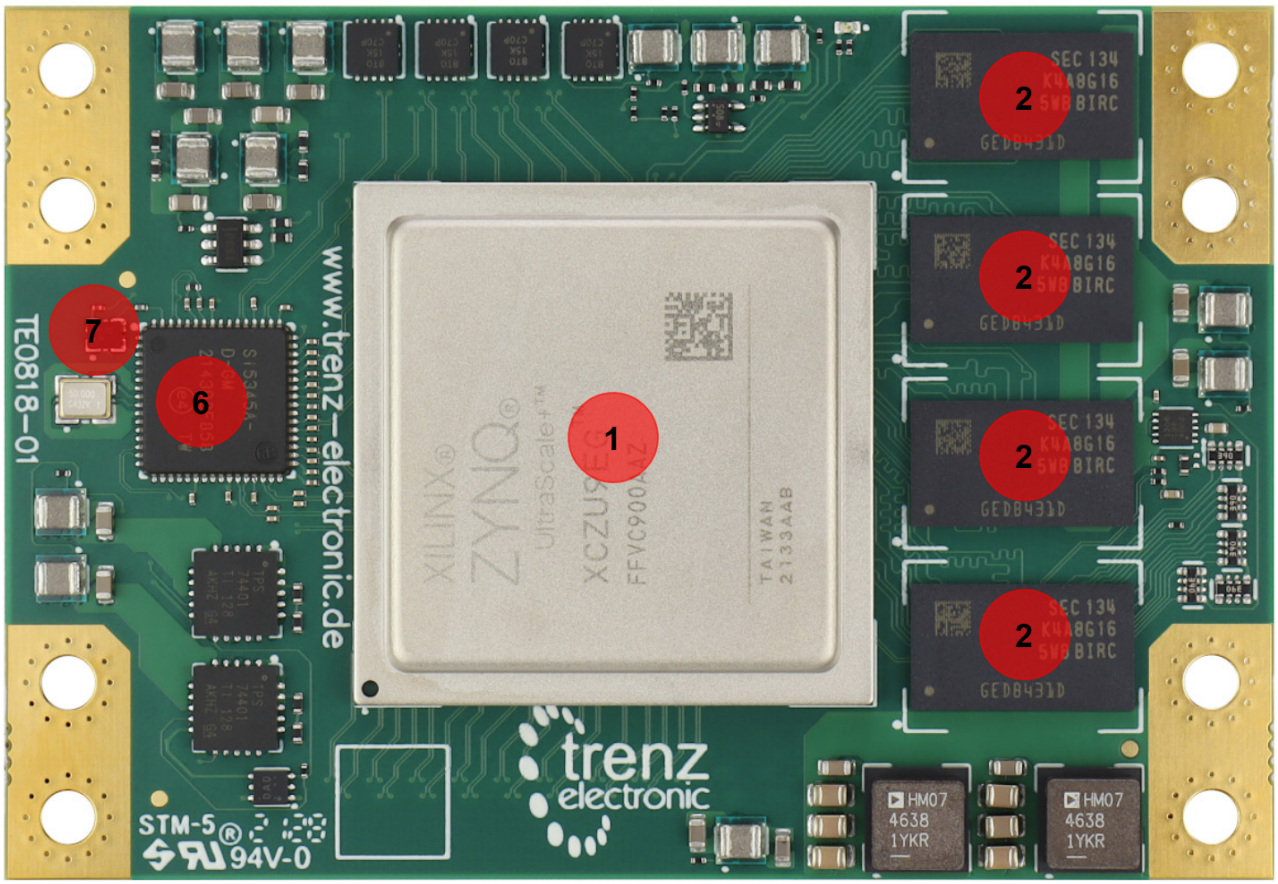
Bank 503
Bank 128
Bank 228
Bank 229
Bank 230
Bank 505
Bank 503
Bank 503
Bank 47
Bank 48
Bank 228
Bank 229
Bank 230
Bank 500
Bank 501
Bank 502
Bank 504
Bank 500
Bank 64
4x MGT Lanes
4x MGT Lanes
4x MGT Lanes
52x HP I/O's, 24x LVDS pairs
J1
25.000000 MHz Oscillator
MAC EEPROM
50.000 MHz XTAL
POR_B
Voltage Monitor Circuit
Manual Reset (MR)
4x MGT Lanes
4x PS GTR Lanes
2x PS GTR CLK Input
1x MGT CLK Input
JTAG
V_P, DX (differential pairs)
PS Config control lines
J2
I²C
3x PLL CLK Output
1x PLL CLK Input
CLK Feedback
10-Output PLL Clock Generator
1x MGT CLK Input
1x MGT CLK Input
1x MGT CLK Input
1x MGT CLK Input
2x PS GTR CLK Input
32.768000 kHz XTAL
33.333333 MHz Oscillator
24x HD I/O's, 12x LVDS pairs
24x HD I/O's, 12x LVDS pairs
1x MGT CLK Input
1x MGT CLK Input
1x MGT CLK Input
13x MIO's
26x MIO's
26x MIO's
J3
1x PLL CLK Input
64bit Memory Interface
DDR4 SDRAM
Dual Parallel QSPI (13x MIO)
2x QSPI Flash Memory
52x HP I/O's, 24x LVDS pairs
J4



TE0818 block diagram

Main Components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TE0818-01
XILINX
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UltraScale+
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STM-5
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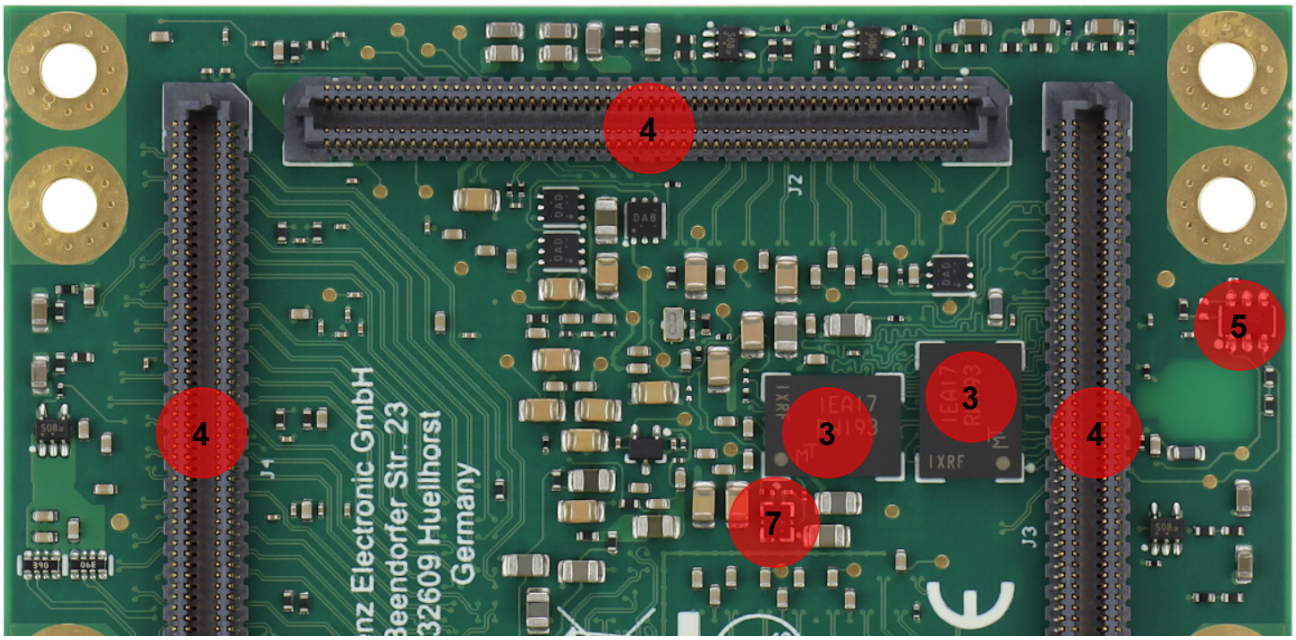
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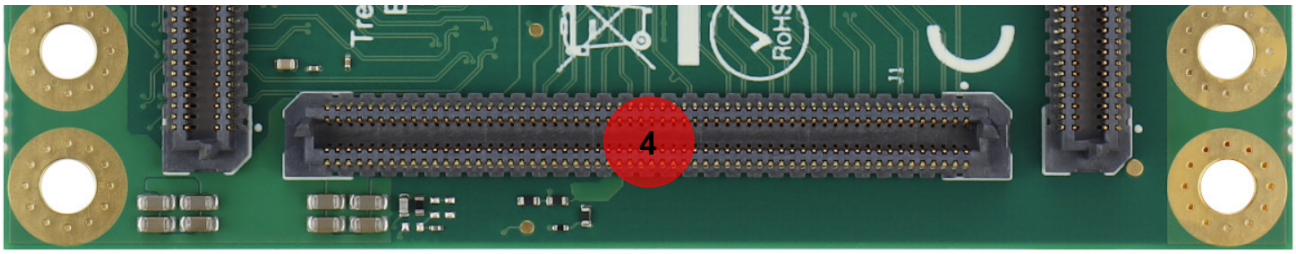
J2
J3
nz Electronic GmbH
Beendorfer Str. 23
32609 Huellhorst
Germany



TExxxx main components

1. SoC, U1
2. DDR4, U2, U3, U9, U12
3. Quad SPI Flash, U7, U17
4. Connector, J1, J2, J3, J4
5. EEPROM, U4
6. Clock Generator, U5
7. Oscillator, U25, U32

Initial Delivery State

Storage device name	Content
DDR4 SDRAM	not programmed
Quad SPI Flash	not programmed
EEPROM	not programmed besides factory programmed MAC address
Programmable Clock Generator	not programmed

Initial delivery state of programmable devices on the module

Signals, Interfaces and Pins

Connectors

Connector Type	Designator	Interface	IO CNT	Notes
B2B	J1	MGT PL	12 x MGT (RX /TX)	
B2B	J1	HP	52 SE / 24 DIFF	
B2B	J2	MGT PS	2 x MGT CLK	
B2B	J2	CLK	DIFF CLK	
B2B	J2	MGT PL	4 x MGT (RX /TX)	
B2B	J2	MGT PS	4 x MGT (RX /TX)	
B2B	J2	CFG	JTAG	
B2B	J2	CFG	MODE	
B2B	J3	HD	48 SE / 24 DIFF	
B2B	J3	MGT PL	3 x MGT CLK	

B2B	J3	CLK	DIFF CLK	
B2B	J3	MIO	65 GPIO	
B2B	J4	HP	104 SE / 48 DIFF	

Board Connectors

Test Points

Test Point	Signal	Notes	Revision Notes
TP1	PLL_SCL	pulled-up to PS_1V8	
TP2	PLL_SDA	pulled-up to PS_1V8	
TP3	LP_DCDC		
TP4	DCDCIN		
TP5	GND		
TP6	TCK		
TP7	PL_DCIN		
TP8	GND		
TP9	GT_DCDC		
TP10	GND		
TP11	TDI		
TP12	TDO		
TP13	TMS		
TP14	PS_1V8		
TP15	1V25_REF	REF3312AIDCKT (U33) ouput voltage	No Net Name for REV01.
TP16	FP_0V85		
TP17	DDR_2V5		
TP18	DDR_PLL		
TP19	PL_VCCINT		
TP20	AUX_R		
TP21	AVTT_R		
TP22	AUX_L		
TP23	DDR4-TEN		Only REV02.
TP24	AVCC_R		
TP25	PLL_SDA	pulled-up to PS_1V8	Only REV02.
TP26	AVTT_L		
TP27	PLL_SCL	pulled-up to PS_1V8	Only REV02.
TP28	AVCC_L		
TP29	LP_DCDC		Only REV02.
TP30	PS_PLL		

TP31	PS_AVTT		
TP32	LP_0V85		
TP33	PS_AUX		
TP34	PS_AVCC		
TP35	DCDCIN		Only REV02.
TP36	POR_B		
TP37	PL_DCIN		Only REV02.
TP38	GT_DCDC		Only REV02.
TP39	PS_1V8		Only REV02.
TP40	1V25_REF		Only REV02.
TP41	FP_0V85		Only REV02.
TP42	DDR_2V5		Only REV02.
TP43	DDR_PLL		Only REV02.
TP44	PL_VCCINT		Only REV02.
TP45	AUX_R		Only REV02.
TP46	AVTT_R		Only REV02.
TP47	AUX_L		Only REV02.
TP48	AVCC_R		Only REV02.
TP49	AVTT_L		Only REV02.
TP50	AVCC_L		Only REV02.
TP51	PS_PLL		Only REV02.
TP52	PS_AVTT		Only REV02.
TP53	LP_0V85		Only REV02.
TP54	PS_AUX		Only REV02.
TP55	PS_AVCC		Only REV02.
TP56	DDR_1V2		Only REV02.
TP57	DDR_1V2		Only REV02.
TP58	SI_PLL_1V8		Only REV02.
TP59	SI_PLL_1V8		Only REV02.
TP60	PL_GT2_1V35		Only REV02.
TP61	PL_GT2_1V35		Only REV02.
TP62	PL_GT2_1V05		Only REV02.
TP63	PL_GT2_1V05		Only REV02.
TP64	PL_GT_1V35		Only REV02.
TP65	PL_GT_1V35		Only REV02.
TP66	PL_GT_1V05		Only REV02.
TP67	PL_GT_1V05		Only REV02.
TP68	3.3VIN		Only REV02.
TP69	3.3VIN		Only REV02.
TP70	DCDC_2V0		Only REV02.

TP71	DCDC_2V0		Only REV02.
TP72	PS_GT_1V0		Only REV02.
TP73	PS_GT_1V0		Only REV02.
TP74	PL_1V8		Only REV02.
TP75	PL_1V8		Only REV02.
TP76	VREFA		Only REV02.
TP77	VREFA		Only REV02.
TP78	VTT		Only REV02.
TP79	VTT		Only REV02.

Test Points Information

On-board Peripherals

Chip/Interface	Designator	Connected To	Notes
DDR4 SDRAM	U2, U3, U9, U12	SoC - PS	
Quad SPI Flash	U7, U17	SoC - PS	Booting.
EEPROM	U4	B2B - J2	
Clock Generator	U5	SoC, B2B	
Oscillator	U25	Clock Generator	25 MHz
Oscillator	U32	SoC	33.333333 MHz

On board peripherals

Configuration and System Control Signals

Connector+Pin	Signal Name	Direction[1)]	Description
J1.A45	POR_OVERRIDE	IN	Override power-on reset delay [2)].
J2.A30	PG_PLL_1V8	OUT	SI_PLL_1V8 power rail powered-up.
J2.A31	ERR_OUT	OUT	PS error indication [2)].
J2.A34	ERR_STATUS	OUT	PS error status [2)].
J2.A35	LP_GOOD	OUT	Low-power domain powered-up. Pulled up to 3.3VIN.

J2.A36	PLL_SCL	IN	I2C clock. Pulled up to PS_1V8.
J2.A37	PLL_SDA	IN/OUT	I2C data. Pulled up to PS_1V8.
J2.A40	PG_GT_L	OUT	Left GTH Transceivers powered-up.
J2.A41	EN_PSGT	IN	Enable GTR transceiver power-up.
J2.A44 / J2.A45 / J2.A46 / J2.A47	TCK / TDI / TDO / TMS	Signal-dependent	JTAG configuration and debugging interface. JTAG reference voltage: PS_1V8
J2.B29	PG_PSGT	OUT	GTR transceivers powered-up.
J2.B30	PROG_B	IN/OUT	Power-on reset [2]. Pulled-up to PS_1V8.
J2.B33	SRST_B	IN	System reset [2]. Pulled-up to PS_1V8.
J2.B34	INIT_B	IN/OUT	Initialization completion indicator after POR [2]. Pulled-up to PS_1V8.
J2.B37	PG_PL	OUT	Programmable logic powered-up.
J2.B38	EN_FPD	IN	Enable full-power domain power-up.
J2.B41	PG_FPD	OUT	Full-power domain powered-up.
J2.B42	EN_LPD	IN	Enable low-power domain power-up.
J2.B45	PG_DDR	OUT	DDR power supply powered-up.
J2.B46	DONE	OUT	PS done signal [2]. Pulled-up to PS_1V8.
J2.B47	EN_DDR	IN	Enable DDR power-up.
J2.C30	EN_GT_L	IN	Enable left GTH transceiver power-up.
J2.C31	MR	IN	Manual reset.
J2.C32	PLL_SEL0	IN	PLL clock selection.
J2.C33	PLL_RST	IN	PLL reset. Pulled-up to PS_1V8.
J2.C35	EN_PL	IN	Enable programable logic power-up.
J2.C36	EN_GT_R	IN	Enable right GTH transceiver power-up.
J2.C37	PLL_FDEC	IN	PLL Frequency decrementation.

J2.C44 / J2.C45 / J2.C46 / J2.C47	MODE3..0	IN	Boot mode selection [2]: • JTAG • QUAD-SPI (32 Bit) • SD1 (2.0) • eMMC (1.8 V) • SD1 LS (3.0) Supported Modes depends also on used Carrier.
J2.D29	EN_PLL_PWR	IN	Enable PLL power supply.
J2.D30	PLL_FINC	IN	PLL Frequency incrementation.
J2.D31	PLL_LOLn	OUT	Loss of lock status.
J2.D32	PLL_SEL1	IN	PLL clock selection.
J2.D33	PG_GT_R	OUT	Right GTH Transceivers powered-up.
J2.D37	PSBATT	IN	PS RTC Battery supply voltage [2] [3].
J2.D38	PUDC_B	IN	Configuration pull-ups setting [2]. Pulled-up to PL_1V8.
J2.D45 / J2.D46	DX_P / DX_N	-	SoC temperatur sensing diode pins [2].

[1] Direction:

- IN: Input from the point of view of this board.
- OUT: Output from the point of view of this board.

[2] See UG1085 for additional information.

[3] See Recommended Operating Conditions.

Controller signal.

Power and Power-On Sequence

Power Rails

Power Rail Name/ Schematic Name	Connector + Pin	Direction[1]	Notes
VCCO_66	J1.A32 / J1.A33	IN	
VREF_66	J1.A41	IN	
3.3VIN	J1.A54 / J1.A55 / J1.B55 / J1.B56	IN	
PL_1V8	J1.C32 / J1.C33 / J1.D33 / J1.D34	OUT	
PL_DCIN	J1.C56 / J1.C57 / J1.C58 / J1.C59 / J1.C60 / J1. D56 / J1.D57 / J1.D58 / J1.D59 / J1.D60	IN	

LP_DCDC	J2.A50 / J2.A51 / J2.A52 / J2.B50 / J2.B51 / J2.B52 / J2.C50 / J2.C51 / J2.C52 / J2.D50 / J2.D51 / J2.D52	IN	
DCDCIN	J2.A57 / J2.A58 / J2.A59 / J2.A60 / J2.B57 / J2.B58 / J2.B59 / J2.B60 / J2.C57 / J2.C58 / J2.C59 / J2.C60 / J2.D57 / J2.D58 / J2.D59 / J2.D60 /	IN	
PS_BATT	J2.D37	IN	
DDR_1V2	J2.D47	OUT	
PS_1V8	J2.C34 / J2.D34 / J3.A56 / J3.B56 / J3.C56 / J3.D56	OUT	
PLL_3V3	J3.A55	IN	
GT_DCDC	J3.A59 / J3.A60 / J3.B59 / J3.B60 / J3.C59 / J3.C60 / J3.D59 / J3.D60 /	IN	
VCCO_48	J3.C7 / J3.C8 / J3.D8 / J3.D9	IN	
VCCO_47	J3.C19 / J3.C20 / J3.D20 / J3.D21	IN	
VCCO_64	J4.B21 / J4.B39	IN	
VREF_64	J4.B30	IN	
VCCO_65	J4.C21 / J4.C39	IN	
VREF_65	J4.C30	IN	

[1] Direction:

- IN: Input from the point of view of this board.
- OUT: Output from the point of view of this board.

Module power rails.

Recommended Power up Sequencing

The power up sequencing highly depends on the use case. In general, it should be possible to enable /disable the processing system (PS) / programmable logic (PL) independently. Furthermore, within the processing logic it should be possible to enable/disable only low-power domain and/or low-power and full-power domain. Additionally, usage of GTR for PS side and GTH for PL side should be possible. GTH transceivers on left and right side are usable independently. Because of this flexibility the needed parts of the following table needs to be selected individually. For detailed information take a look into schematics.

Sequence	Net name	Recommended Voltage Range	Pull-up/down	Description	Notes
0	-	-	-	Configuration signal setup.	See Configuration and System Control Signals.
1 [1]	PSBATT	1.2 V ... 1.5 V	-	Battery connection.	Battery Power Domain usage. When not used, tie to GND.

1	3.3VIN	3.3 V (± 5 %)	-	Management power supply.	Management module power supply. 0.5 A recommended.
GTH / GTR Transceiver clocking (Only necessary in cases where the PLL clock is used for GTH / GTR.):					
1 [1)]	GT_DCDC	3.3 V (± 5 %) [2)]		GTH transceiver power supply.	Main module power supply for GTH / GTY transceiver. 5 A recommended. Power consumption depends mainly on design and cooling solution.
1 [1)]	EN_PLL_PWR	-	PU [3)], 3.3VIN	PLL power enable.	
1 [1)]	PG_PLL_1V8	-	PU [3)], 3.3VIN	PLL power good status.	
1 [1)]	PLL_3V3	3.3 V (± 5 %)		PLL power supply	
2	Processing System (PS):			Procedure for PS starting.	
2.1	Low-power domain:			Bring-up for low-power domain PS.	
2.1.1	LP_DCDC	3.3 V (± 5 %) [2)]	-	Low-power domain power supply.	Main module power supply for low-power domain. 5.5 A recommended. Power consumption depends mainly on design and cooling solution.
2.1.2	EN_LPD	-	PU [3)], 3.3VIN	Low-power domain power enable.	
2.1.3	LP_GOOD	-	PU [3)], 3.3VIN	Low-power domain power good status.	Module power-on sequencing for low-power domain finished.
2.2	Full-power domain:			Bring-up for full-power domain PS.	Full-power PS domain needs powered low-power PS domain.
2.2.1	DCDCIN	3.3 V (± 5 %) [2)]		Full-power domain and GTR transceiver power supply.	Main module power supply for full-power domain. 7 A recommended. Power consumption depends mainly on design and cooling solution.
2.2.2	EN_FPD	3.3 V	-	Full-power domain power enable.	

2.2.3	PG_FPD	-	PU [3], 3.3VIN	Full-power domain power good status.	Module power-on sequencing for full-power domain finished.
2.2.4	EN_DDR	3.3 V	-	DDR memory power enable.	
2.2.5	PG_DDR		PU [3], 3.3VIN	DDR memory power good status.	Module power-on sequencing for DDR memory finished.
2.3	GTR Transceiver			Procedure for GTR transceiver starting.	PS transceiver usage needs powered PS (low- and full-power domain).
2.3.1	EN_PSGT	3.3 V	-	GTR transceiver power enable.	
2.3.2	PG_PSGT	-	PU [3], 3.3VIN	GTR transceiver power good status.	Module power-on sequencing for GTR transceiver finished.
2	Programmable Logic (PL)			Procedure for PL starting.	PS and PL can be started independently.
2.1	PL_DCIN	3.3 V (± 5 %) [2]	-	Programmable logic power supply.	Main module power supply for programmable logic. 12 A recommended. Power consumption depends mainly on design and cooling solution.
2.2	EN_PL	-	PU [3], 3.3VIN	Programmable logic power enable.	
2.3	PG_PL	-	PU [3], 3.3VIN	Programmable logic power good status.	Module power-on sequencing for programmable logic finished. Periphery and variable bank voltages can be enabled on carrier.
2.4	VCCO_47 / VCCO_48 / VCCO_64 / VCCO_65 / VCCO_66	[4]	-	Module bank voltages.	Enable bank voltages after PG_PL deassertion.
3	GTH / GTY Transceiver			Procedure for GTH / GTY transceiver starting.	PL transceiver usage needs powered PL and low-power PS domain.

3.1	GT_DCDC	3.3 V (± 5 %) [2]	-	GTH transceiver power supply.	Main module power supply for GTH transceiver. 5 A recommended. Power consumption depends mainly on design and cooling solution.
3.2	EN_GT_L / EN_GT_R	3.3 V	-	GTH / GTY left / right transceiver power enable.	Transceivers on left / right side can be used independently.
3.3	PG_GT_L / PG_GT_R	-	PU [3], 3.3VIN	GTH / GTY transceiver power good status.	

[1] (optional)

[2] Dependent on the assembly option a higher input voltage may be possible.

[3] (on module)

[4] See DS925 for additional information.

Baseboard Design Hints

Board to Board Connectors

5.2 x 7.6 cm UltraSoM+ modules use four Samtec AcceleRate HD High-Density Slim Body Arrays on bottom side.

- 4x ADM6-60-01.5-L-4-2 (240 pins, 60 per row)
  - Mates with ADF6-60-03.5-L-4-2

5.2 x 7.6 cm UltraSoM+ carrier use four Samtec AcceleRate HD High-Density Slim Body Arrays on top side.

- 4x ADF6-60-03.5-L-4-2 (160-pins)
  - Mates with ADM6-60-01.5-L-4-2

Features

- Board-to-Board Connector 240-pins, 60 contacts per row
- 0.025" (0.635 mm) pitch
- Data Rate: max 56 Gbps
- Mates with: ADM6/APF6
- Insulator Material: LCP, Black
- Contact Material: Copper Alloy
- Plating: Au or Sn over 50 µ" (1.27 µm) N
- Operating Temperature Range: -55 ºC to +125 ºC
- PCIe 5.0 capable: Yes
- Lead-Free Solderable: Yes
- RoHS Compliant: Yes

Connector Stacking height

When using the standard type on baseboard and module, the mating height is 5 mm.

Other mating heights are possible by using connectors with a different height:

Order number	REF number	Samtec Number	Type	Contribution to stacking height	Comment
30095	REF-30095	ADM6-60-01.5-L-4-2	Module connector	1.5 mm	Standard connector used on modules
31137	REF-31137	ADF6-60-03.5-L-4-2	Baseboard connector	3.5 mm	Standard connector used on carrier

Connectors.

Connector Speed Ratings

The AcceleRate HD High-Density connector speed rating depends on the stacking height; please see the following table:

Stacking height	Speed rating
5 mm	56 Gbps

Speed rating.

Current Rating

Current rating of Samtec AcceleRate HD High-Density B2B connectors is 1.34 A per pin (4 pins powered)

Connector Mechanical Ratings

- Shock: 100G, 6 ms Sine
- Vibration: 7.5G random, 2 hours per axis, 3 axes total

Manufacturer Documentation

File	Modified
PDF File 20200225_hsc_adm6-xx-01p5-xxx-4-a_adf6-xx-03p5-xxx-4-a.pdf	10 01, 2022 by Martin Rohrmüller
PDF File adf6.pdf	10 01, 2022 by Martin Rohrmüller
PDF File ADF6-XXX-XX.X-XXX-X-X-X-FOOTPRINT.PDF	10 01, 2022 by Martin Rohrmüller
PDF File adf6-xxx-xx.x-xxx-x-x-x-xr-mkt.pdf	10 01, 2022 by Martin Rohrmüller
PDF File adx6 mated document.pdf	10 01, 2022 by Martin Rohrmüller

Download All

Technical Specifications

Absolute Maximum Ratings *)

Power Rail Name/ Schematic Name	Description	Min	Max	Unit
LP_DCDC	Micromodule Power	-0.300	6.0	V
DCDCIN	Micromodule Power	-0.300	7.0	V
GT_DCDC	Micromodule Power	-0.300	6.0	V
PL_DCIN	Micromodule Power	-0.300	7.0	V
3.3VIN	Micromodule Power	-0.300	3.600	V
PLL_3V3	PLL power supply	-0.500	3.8	V
PS_BATT	RTC / BBRAM	-0.500	2.000	V
VCCO_47	HD IO Bank power supply	-0.500	3.400	V
VCCO_48	HD IO Bank power supply	-0.500	3.400	V
VCCO_64	HP IO Bank power supply	-0.500	2.000	V
VCCO_65	HP IO Bank power supply	-0.500	2.000	V
VCCO_66	HP IO Bank power supply	-0.500	2.000	V
VREF_64	Bank input reference voltage	-0.500	2.000	V
VREF_65	Bank input reference voltage	-0.500	2.000	V
VREF_66	Bank input reference voltage	-0.500	2.000	V

Module absolute maximum ratings

*) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Condition. Exposure to absolute-maximum rated conditions for extended periods may affect device reliability.

Recommended Operating Conditions

This TRM is generic for all variants. Temperature range can be differ depending on the assembly version. Voltage range is mostly the same during variants (exceptions are possible, depending on custom request).

Operating temperature range depends also on customer design and cooling solution. Please contact us for options.

- Variants of modules are described here: Article Number Information
- Modules with commercial temperature grade are equipped with components that cover at least the range of 0°C to 75°C
- Modules with extended temperature grade are equipped with components that cover at least the range of 0°C to 85°C
- Modules with industrial temperature grade are equipped with components that cover at least the range of -40°C to 85°C
- The actual operating temperature range will depend on the FPGA / SoC design / usage and cooling and other variables.

Parameter	Min	Max	Units	Reference Document
LP_DCDC 1)	3.201	3.399	V	

DCDCIN [1)]	3.135	3.465	V	
GT_DCDC [1)]	3.201	3.399	V	
PL_DCIN [1)]	3.135	3.465	V	
3.3VIN	3.135	3.465	V	
PLL_3V3	3.201	3.399	V	
PS_BATT	1.200	1.500	V	See FPGA datasheet.
VCCO_47	1.164	3.399	V	See FPGA datasheet.
VCCO_48	1.164	3.399	V	See FPGA datasheet.
VCCO_64	0.970	1.854	V	See FPGA datasheet.
VCCO_65	0.970	1.854	V	See FPGA datasheet.
VCCO_66	0.970	1.854	V	See FPGA datasheet.
VREF_64	0.6	1.2	V	See FPGA datasheet.
VREF_65	0.6	1.2	V	See FPGA datasheet.
VREF_66	0.6	1.2	V	See FPGA datasheet.

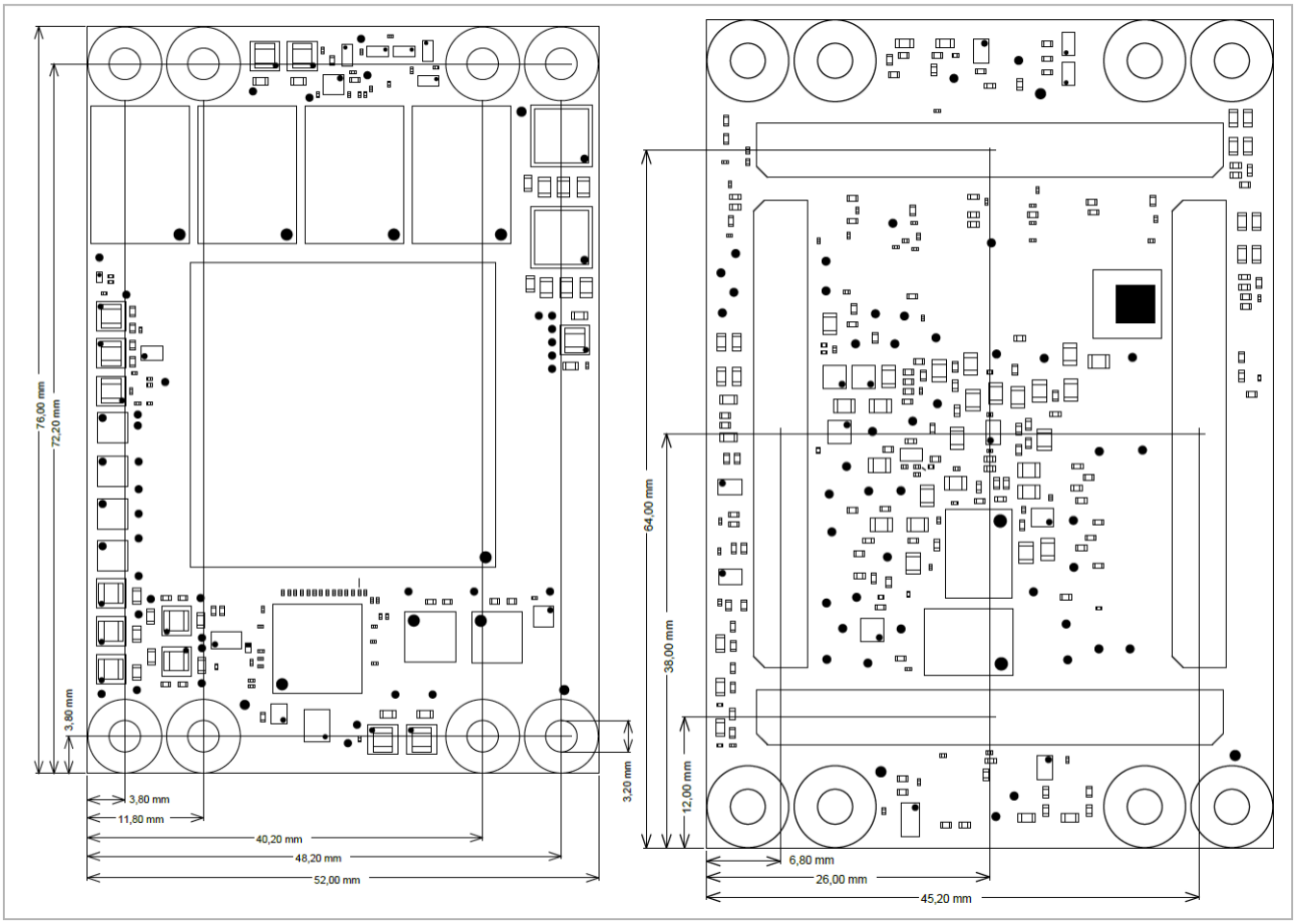
[1)] Higher values may possible. For more information consult schematic and according datasheets.

Recommended operating conditions.

Physical Dimensions

- Module size: 76 mm × 52 mm. Please download the assembly diagram for exact numbers.
- Mating height with standard connectors: 5 mm.

PCB thickness: 1.6 mm (± 10 %).



Physical Dimension

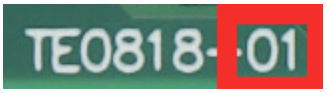
Currently Offered Variants

Trenz shop TE0818 overview page	
English page	German page

Trenz Electronic Shop Overview

Revision History

Hardware Revision History



Board hardware revision number.

Date	Revision	Changes	Documentation Link
-	REV02	1. Added capacitors C178, C187, C188, C189 (470nF) to VTT net. 2. Added U18/ U37 compensation network: R119, C190, C191. R118 is optional jumper and is installed when using the internal compensation network. External compensation network is used by default. 3. Connected all DDR4 TEN pins together and pulled them down with resistor R120 and added testpoint TP23. 4. Added testpoints TP25, TP27, TP29, TP35, TP37...TP79. 5. Changed capacitor C112 size from 0402 to 0201 and voltage rating from 16 V to 10 V. 6. Changed ferrid beads from MPZ0603S121HT000 to BLM15PX800SZ1D for L1, L2, L3, L4, L5, and L7. 7. Changed ferrid beads from MPZ1608S221A to BLM15PX800SZ1D for L6 and L8. 8. Added diode D2 between U41 pin 3 net MR and voltage rail 3.3VIN. 9. Modified trace length. 10. Updated documentation overviews.	REV02
-	REV01	First Production Release	REV01

Hardware Revision History

Hardware revision number can be found on the PCB board together with the module model number separated by the dash.

Document Change History

Date	Revision	Contributor	Description

Error rendering macro 'page-info' Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.	• Added power supply PLL_3V3 in table "Recommended Power up Sequencing". • Fix typo.

Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class

Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class

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com.atlassian.confluence.core.ContentEntityObject]	com.atlassian.confluence.core.ContentEntityObject]	com.atlassian.confluence.core.ContentEntityObject]	
2023-09-20	v.16	ED	• Updated for REV02
2023-01-12	v.13	ED	• Initial Document
--	all	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which	• --

method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.

		confluence.core.ContentEntityObject][interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	

Document change history.

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Users of electrical and electronic equipment in private households are required not to dispose of waste electrical and electronic equipment as unsorted municipal waste and to collect such waste electrical and electronic equipment separately. By the 13 August 2005, Member States shall have ensured that systems are set up allowing final holders and distributors to return waste electrical and electronic equipment at least free of charge. Member States shall ensure the availability and accessibility of the necessary collection facilities. Separate collection is the precondition to ensure specific treatment and recycling of waste electrical and electronic equipment and is necessary to achieve the chosen level of protection of human health and the environment in the European Union. Consumers have to actively contribute to the success of such collection and the return of waste electrical and electronic equipment. Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.

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