MicroBlaze Linux

min_linux

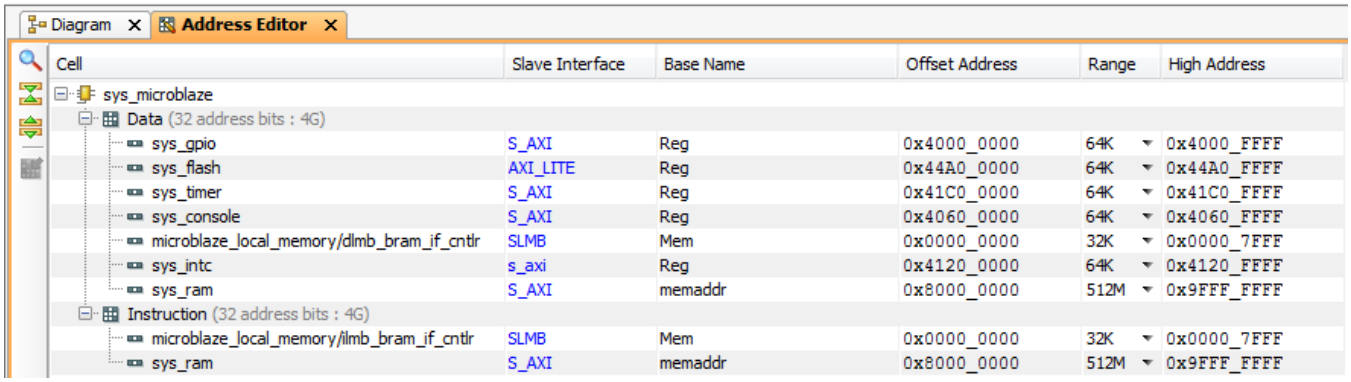
This is a minimal MicroBlaze based system that can boot Linux and is fully ready for integration into Xilinx Petalinux. This design will be provided for all Modules that can support it (except ZYNQ based ones). Primary requirement is external memory (32MByte or more). This design does fit into any 7 Series FPGA except Artix A15T.

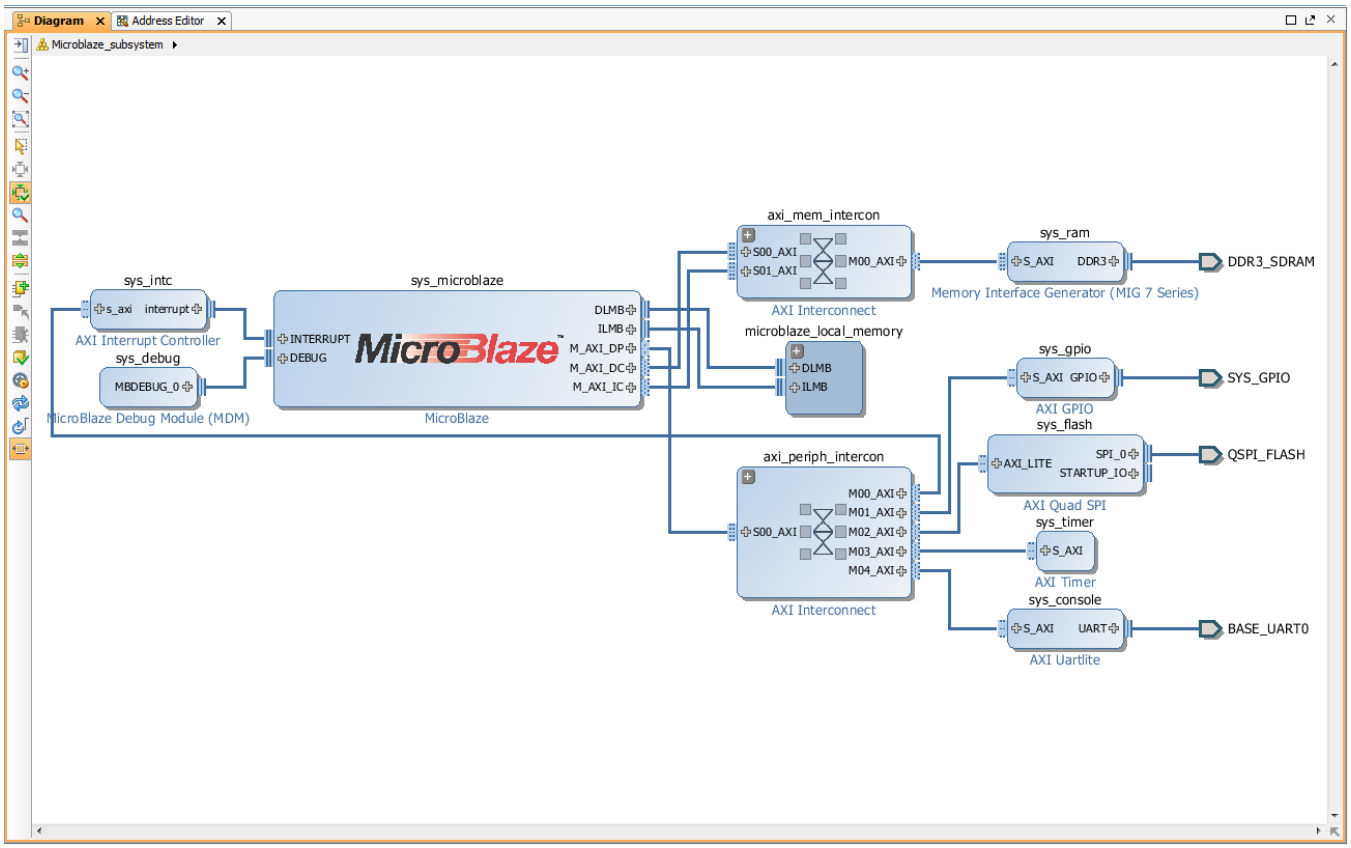
List of supported modules

- TE0710
- TE0712
- TE0713

The goal for this minimal Linux system is to provide standard hardware that can be used with same software images without the need to recompile or customize them.

IP Core	Base address	Interrupt	Board Part Interface	Notes
MicroBlaze				Configured with low end Linux option
MIG	0x8000_0000		DDR3_SDRAM	Configured as per Module settings
LMB_RAM	0x0000_0000			For FS-BOOT, 8K minimum size
MDM		n/a		Configured without JTAG UART
AXI_INTC	0x4120_0000			
AXI_TIMER	0x41C0_0000	0		32 bit mode Dual Channel Mode
AXI_UARTLITE	0x4060_0000	1	BASE_UART0	Configured with 115200 baud
AXI_QUAD_SPI	0x44A0_0000	2	QSPI_FLASH	Connected to on-board Flash, standard mode
AXI_GPIO	0x4000_0000	not used	SYS_GPIO	





Minimal Linux capable System Block Diagram.

It is possible to use same unmodified fs-boot.elf, u-boot-s.bin and image.ub as long as the hardware matches the requirements.

umin_linux

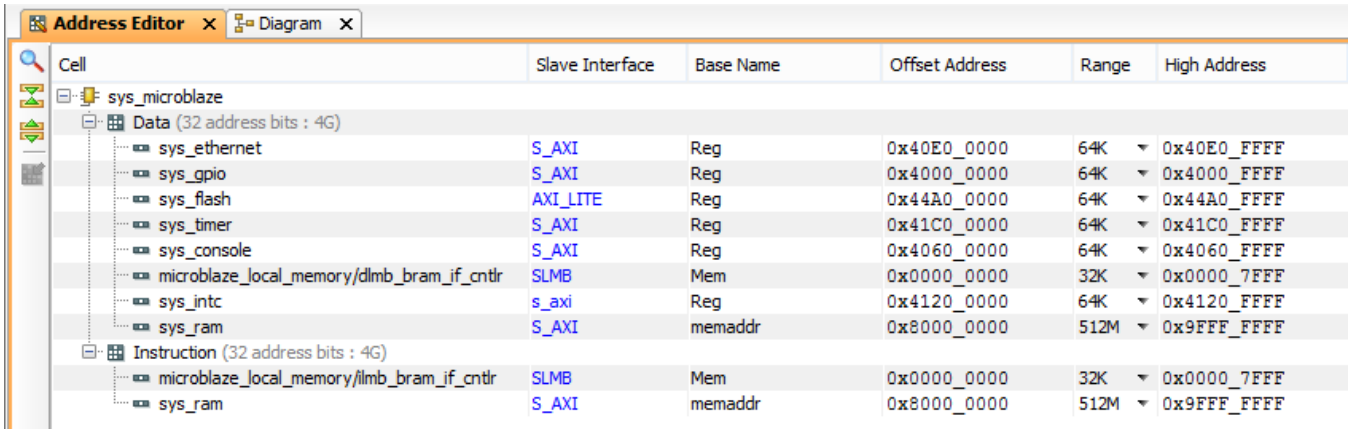
This Design is based on min_linux further reducing the peripherals and functions: Debug and GPIO are removed. This design does fit into any Xilinx 7 series FPGA including A15T. On A15T device the design takes almost all logic resources, adding one more AXI peripheral would most likely go over 100% utilization. It is provided just show the utilization of the bare-minimal Microblaze-MMU system capable to run full Linux.

FPGA	Slice used %	FF used %
A15T	98%	
A35T	49%	
A50T		
A75T		
A100T		
A200T		

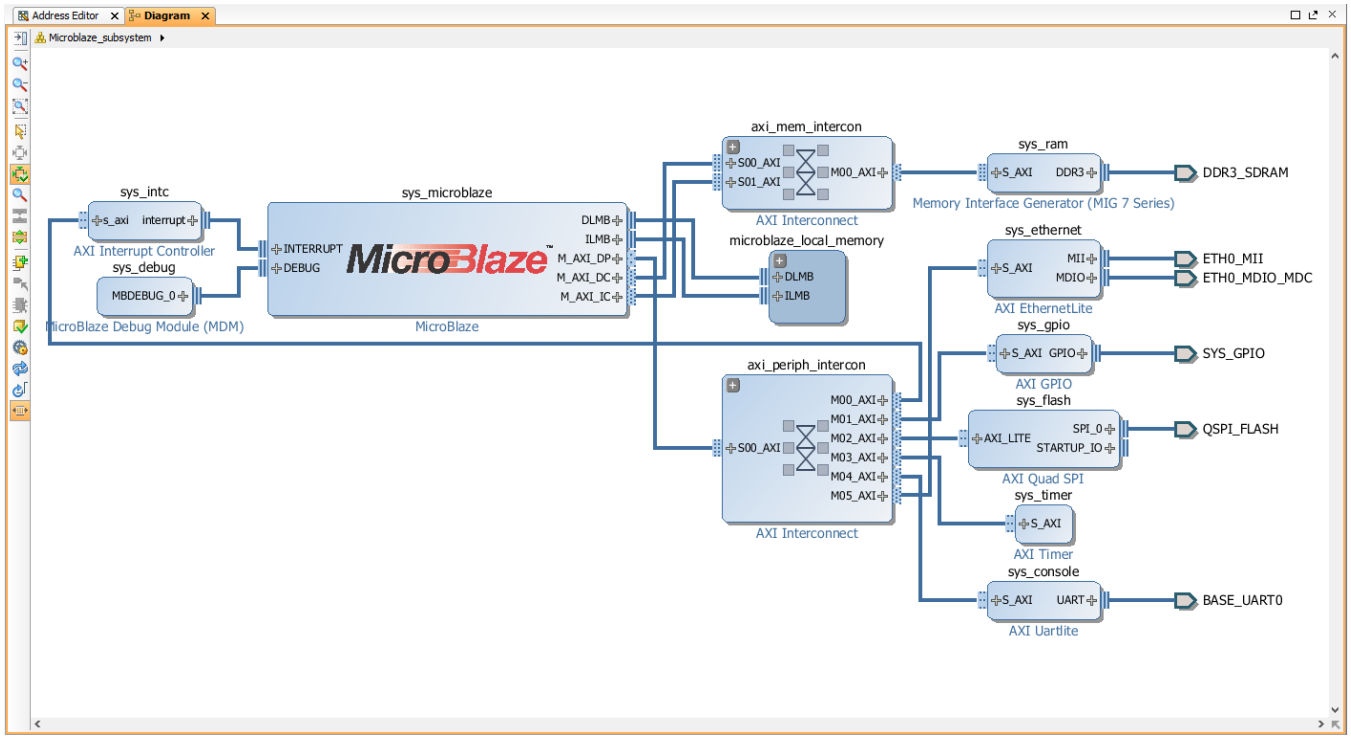
min_linux_eth

This Design is based on min_linux, adding AXI_Ethernetlite IP Core.

IP Core	Base address	Interrupt	Board Part Interface	Notes
AXI_Ethernetlite	0x40E0_0000	3	sys_ethernet	on TE0710 is connectd to MII, on TE0712 ist connected with the core "MII to RMII" to RMII



TE0710 uses MII Interface



TE0712 uses RMII Interface