Blinky

As not all modules have user LED's on FPGA pins, blinky designs include some different variants.

LED Type	Connected to	Comments
MIO LED	Zynq PS MIO GPIO pin	Can be controlled by software, direct control from FPGA fabric not possible (not without software assistance).
FPGA LED	FPGA I/O pin	Can be controlled directly from FPGA logic. Can be controlled from Zynq ARM software if EMIO GPIO output is routed to the FPGA pin with LED. Pin location defined with XDC constraints.
DONE LED	FPGA Done pin (also on Zynq devices)	Can be controlled from FPGA using USRACCESSE2 primitive, no XDC constraint needed. Can also be controlled from PS ARM code using EMIO GPIO to UACCESSE2 routing.

Design name	Clock source	LED Used	Blinks, if:
blinky_onchip	FPGA internal	Primary LED on the module	FPGA is configured
blinky_sysled	Primary FPGA clock	Primary LED on the module	Main clock is toggling
blinky_gtclk	Primary GT Clock	Primary LED on the module	Primary GT clock is toggling
blinky_onchip_done	FPGA internal	FPGA Done LED	FPGA is configured
blinky_gtclk_done	Primary GT Clock	FPGA Done LED	Primary GT clock is toggling