EFUSE_USER

Introduction

The Trenz Electronic teCORE™ IP "EFUSE_USER" is designed to provide simple access to Xilinx EFUSE_USR Primitive from Vivado IPI This IP Core is only a IP Wrapper around the primitive.

teCORE™ IP Facts Table	
Supported Device Family	Zynq® -7000, 7 Series, UltraScale, UltraScale+
Supported User Interfaces	AXI4-Stream
Resources	EFUSE_USR
Provided with Core	
Documentation	Product Guide
Design Files	VHDL Source Code
Tested Design Flows	
Design Entry	Vivado® Design Suite, IP Integrator
Simulation	Vivado Simulator
Synthesis	Vivado Synthesis
Support	
Provided by Trenz Electronic GmbH	

Overview

Feature Summary

- Wrapper for EFUSE_USR Primitive
- AXI4-Stream master for output or
- Direct 32 bit output port

Applications

- Data acquisition

Licensing

Product Specification

Performance

The following sections detail the performance of the core.

Maximum Frequencies

Maximum Frequency is not applicable as this core provide only static output values.

Latency

Latency is not applicable as this core provide only static output values.

Throughput

Throughput is not applicable as this core provide only static output values.

Resource Utilization

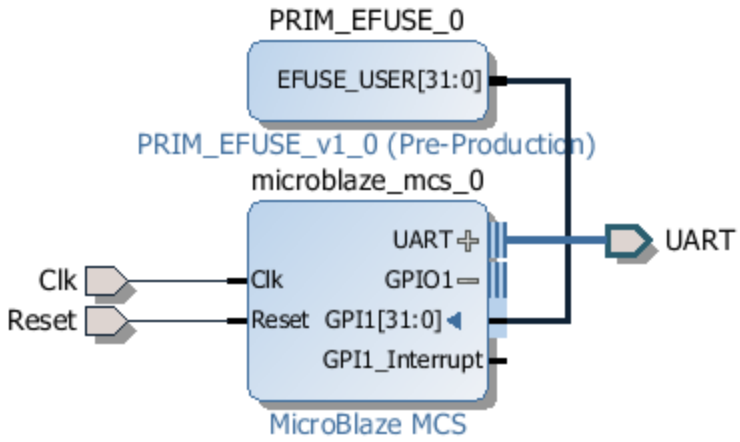
This core does not use any dedicated I/O or CLK resources.

LUTs	FFs	EFUSE_USR
0	0	1

Use Cases

The EFUSE_USR IP Core can be used with Zynq PS or MicroBlaze or MicroBlaze MCS.

MicroBlaze MCS



EFUSE value can be read from MCS Input port.

MicroBlaze AXI4-Stream

EFUSE value can be read using MicroBlaze special instructions.