

Modified TE0703 for Microchip Getting Started

Modified TE0703 with TEM0007

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Modification to use TEM0007 with Standard 4x5 TE0703 carrier. Carrier without modifications will be [TE B2000](#) in the future

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TEM0007 module is a Microchip PolarFire SoC module. For more information about this module refer to [TEM0007 TRM](#)

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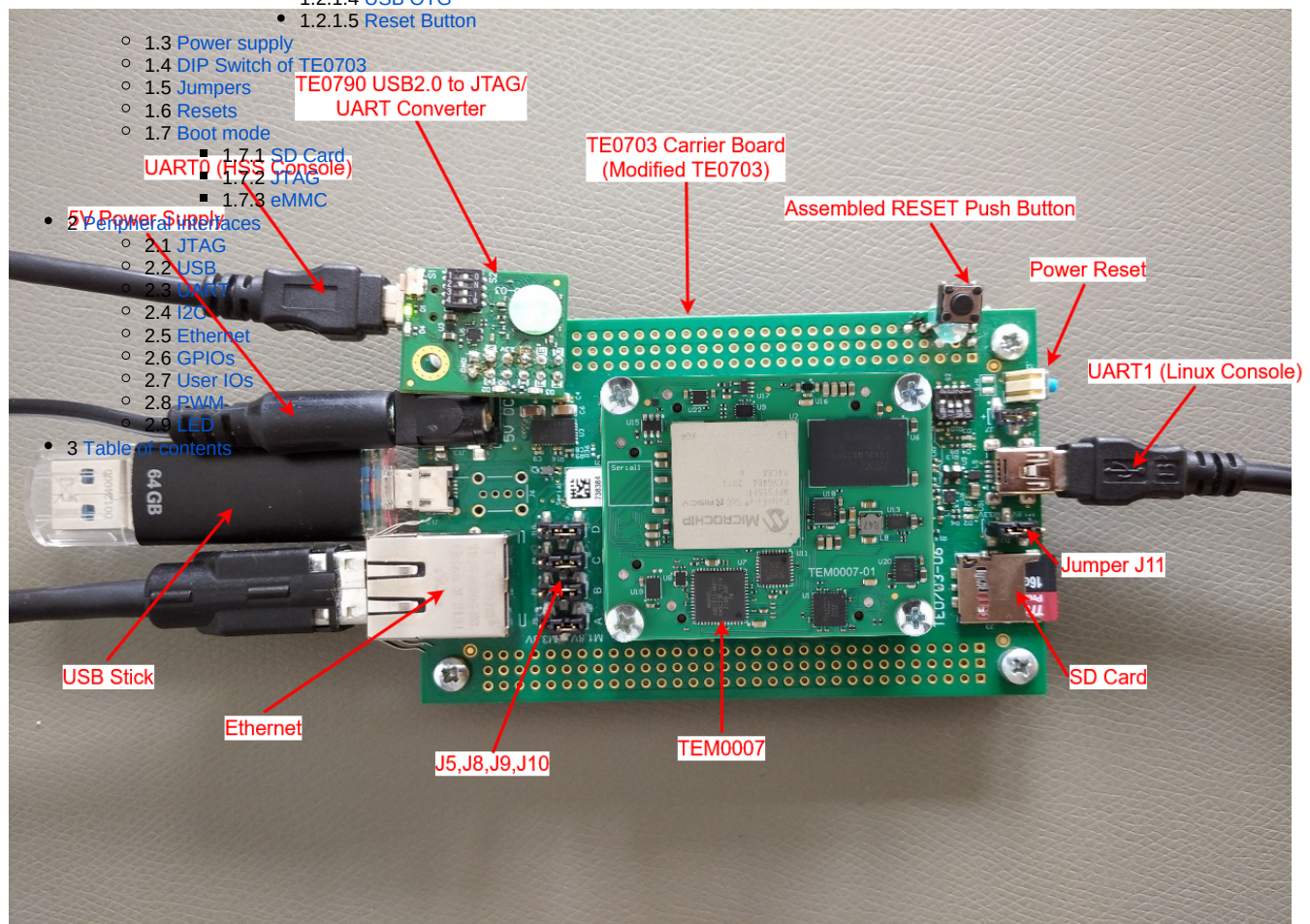
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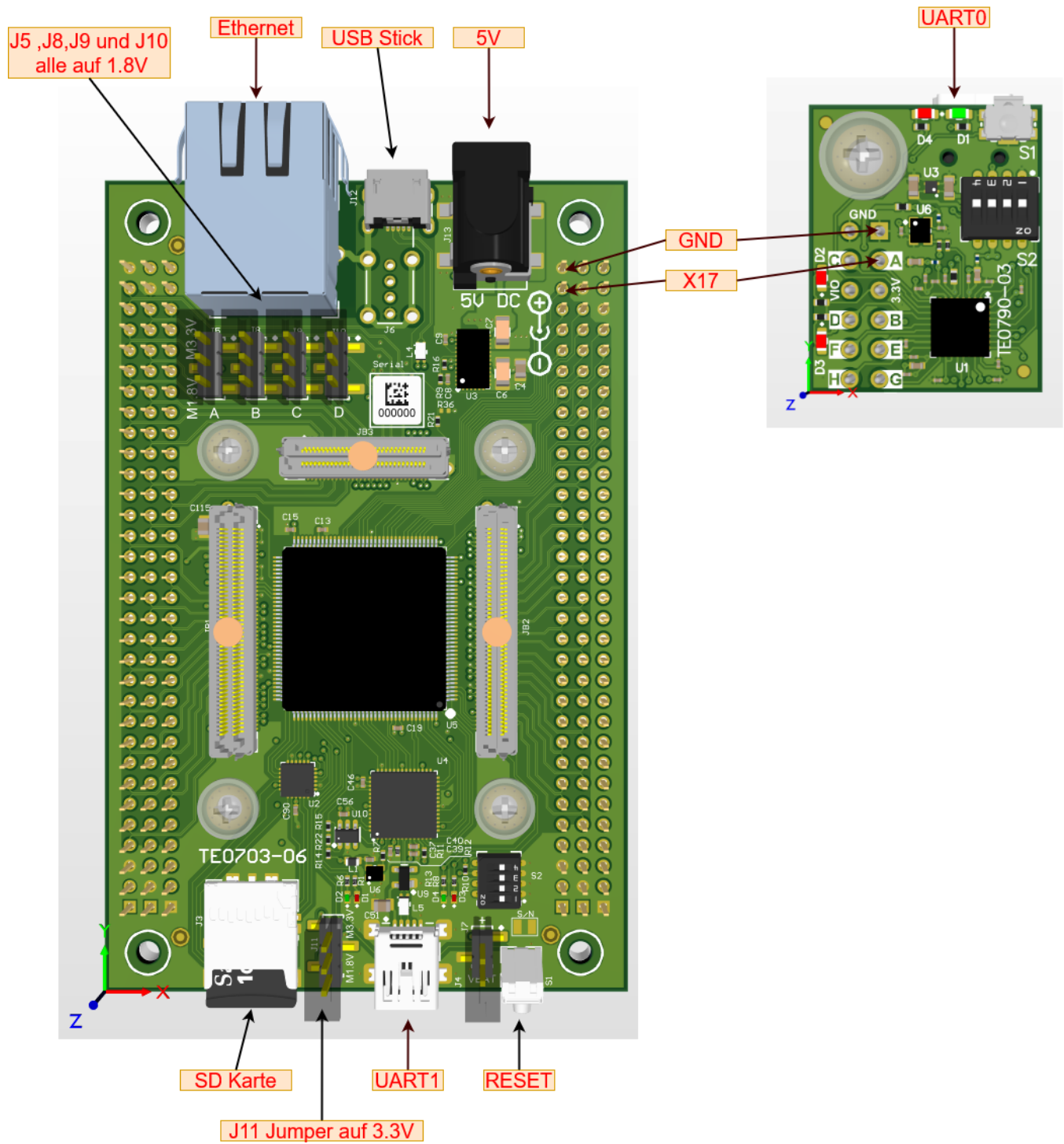
Hardware overview

Required Hardware

Hardware	Quantity	Note
TEM0007	1	Microchip Polarfire SoC Module
Modified TE0703	1	Carrier board Modified TE0703: • FTDI Firmware • Added second uart (uart0) • Additional Reset push button
TE0790	1	Universal USB2.0 to JTAG /UART
Mini USB Cable	2	
RJ45 Ethernet Cable	1	
USB Stick	1	
Heatsink	1	

Modification TE0703

It is necessary to modify the TE0703 carrier board for using TEM0007 module. In the following will be in detail discussed the modification of TE0703 carrier board.



SD Jumper

Jumper J11 must be set to 3.3V.



Set SD card voltage

XMOD UART(HSS)

It is recommended to use second UARD interface to see the HSS console. The UART pins must be connected to XMOD module (TE0790). The TE0790 is a universal USB2.0 to JTAG/UART converter. For more information about this module refer to [TE0790 TRM](#)

For this purpose see the following table:

TE0703 Pin	Schematic label	TE0790 Pin	Schematic label	Description
J2A-Pin A31 (TXD)	X17	J2-Pin 3 (RXD)	A	
J2A-Pin A30 (RXD)	X16	J2-Pin 5 (TXD)	B	This connection does not need to be connected if no data has to be entered in HSS console.
J2A-Pin A32 (GND)	---	J2-Pin 1	---	

Dip switch of TE0790 module must be set according to the following table:

TE0790 (XMOD)	S2-1	S2-2	S2-3	S2-4
S2 Dip Switch Status	ON	OFF	ON	ON

JTAG FTDI

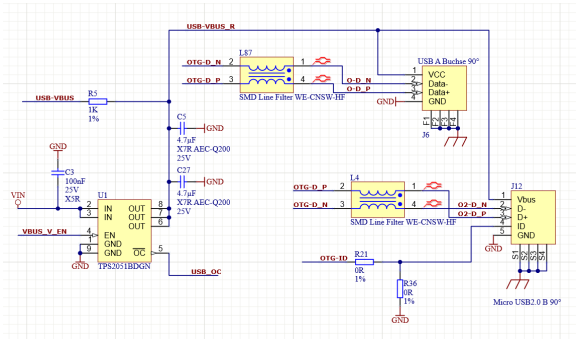
Driver of FTDI chip must be reprogrammed. It must be mached with microchip FPGAs.

USB OTG

The following components of the TE0703 must be changed , if these don't exist on the board or other component is soldered :

Component	Artikel Nummer	Value	Designator (Desoldering)	Designator (Soldering)	Description
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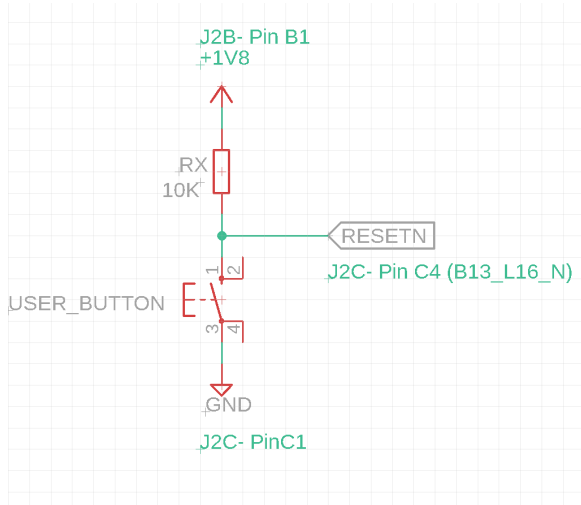
USB connector	27235	---	J6	J12	Micro USB2 B 90°
Choke	24514	---	L87	L4	SMD Line Filter WE-CNSW-HF
Resistor	22752	1k 1%	R5	R5	
Capacitor	26238	4.7uf 25V	C5	C5	X7R AEC-Q200
Capacitor	26238	4.7uf 25V	C27	C27	X7R AEC-Q200



USB schematic

Reset Button

It is installed a power reset button. But it is recommended to have a soft reset button optional. The recommended schematic consists of a push button with a pulled up resistor as shown:



Reset Schematic



Assembled Reset push button

Pin	TE0703 Schematic label	Description
3.3V	J2B- Pin B1	VG96 female header vertical
GND	J2C-Pin C1	VG96 female header vertical
RESETN	J2C-Pin C4	VG96 female header vertical

Power supply

Supply voltage	Current	Designator	Description
5V	2A*	J13 on the carrier board	

*Current is dependent on design and the used heatsink. This value is recommend value.

DIP Switch of TE0703

In this case S2 dip switch of the carrier board TE0703 can be used for JTAG setting only and it will not be used to select boot mode.

S2-1	S2-2	S2-3	S2-4	Description
CM1	CM0	JTAGEN	MIO0	

S2-2	S2-3	CM0	JTAGEN	Description
OFF	OFF	1	1	Access to TE0703 CPLD
OFF	ON	1	0	Access to CPLD of TEM0007
ON	OFF	0	1	Access to TE0703 CPLD
ON	ON	0	0	Access to FPGA of TEM0007

Jumpers

Jumper	related net	Allowed to set on	Description
J7	VBAT	---	Unnecessary
J11	VCCA pin of voltage level shifter chip (TXS02612RTWR)	3.3V	If this jumper set to 1.8V , SD card will not work.
J5	VCCIOA	---	Unnecessary

J8	VCCIOB	1.8V / 3.3V	This jumper can be set to 1.8V or 3.3V.
J9	VCCIOC	---	Unnecessary
J10	VCCIOD	Only 1.8V	Set to 1.8V

Resets

There are one reset push button on the board. Second reset button can be added on the board as optional reset.

Signal	Push button	FPGA Pin	Schematic label	New design label	Connected to	Access on the carrier board via	Description
RESET (RESIN)	S1	H7	DEVRST_N	---	TPS3106K33 DBV chip RSTVDD Pin / CPLD of TEM0007 via B2B connector (SC_RESET / MR_n)	S1	This bush button is soldered already on the carrier board. This reset signal does not exist in Libero design. This reset signal resets FPGA via CPLD Firmware of TEM0007 module. By pushing S1 (RESIN) push button will set DEVRST_N to low.
RESETN	User button	H13	B1_GPIO185_N	RESETN	JM2-Pin 73	JB2-pin 74 / J2C-C4	User button does not exist on the carrier board. User button should be soldered by the user himself. (Optional) This button should be pulled up via a 10k resistor.

Boot mode

SD Card

This module supports SD card boot mode. There is no dip switch to select boot mode. The selection between SD card or other boot mode will be done in HSS. TEM0007 module supports SD card boot mode and JTAG boot mode.

JTAG

This boot mode does not exist in the reference design. In the future this boot mode can be used in the reference design.

eMMC

TEM0007 does not support eMMC boot mode.

Peripheral interfaces

JTAG

FTDI chip is used in the TEM0007 module for conversion USB to UART/JTAG interfaces. This chip needs driver to put this chip in operation. User does not need additional programmer more.

USB

USB Connector	Designator	Connected to	Description
USB2.0 mini usb	J12	FT2232H FTDI Chip	This interface is used to access to UART1 or JTAG interface.
USB2.0 mini usb	J6	USB3320C-EZK USB PHY Chip on the TEM0007 module	It is used to connect external USB device same as USB Stick.

UART

There is two UART interfaces.

UART	Design label	FPGA Pin	Schematic label	Connected to	Access on the carrier board via	Interface for	Baud rate	Description
UART0	MMUART_0_TXD	C2 (TXD)	UART_CON_TX	JM1-Pin 99	JB1-Pin 100 / J2A-Pin 31 (TXD)	HSS (Hardware System Service)	115200	There is no connector on the TE0703 carrier board PCB REV06. In this case user should connect these pins to USB to JTAG /UART converter same as TE0790. (Crosstalk)
	MMUART_0_RXD	D3 (RXD)	UART_CON_RX	JM1-Pin 97	JB1-Pin 98 / J2A-Pin 30 (RXD)			
UART1	MMUART_1_TXD	H5 (TXD)	UART_TX	JM1-Pin 85	JB1-Pin 86 / J4 Mini USB connector	Linux console / Bare metal interface	115200	
	MMUART_1_RXD	H2 (RXD)	UART_RX	JM1-Pin 92	JB1-Pin 91 / J4 Mini USB connector			
UART2	MMUART_2_TXD_M2F	B22 (TXD)	B1_GPIO22_N	JM2-Pin 36	JB2-Pin 35	Optional for customer	----	This UART interface is an optional

	MMUART_2_RXD_F2M	C22 (RXD)	B1_GPIO23_P	JM2-Pin 44	JB2-Pin 43			UART interface for customer. It is necessary to provide other required features same as design in linux to put this interface in application.
UART3	MMUART_3_TXD_M2F	D21 (TXD)	B1_GPIO22_P	JM2-Pin 52	JB2-Pin 51	Optional for customer	----	This UART interface is an optional UART interface for customer. It is necessary to provide other required features same as design in linux to put this interface in application.
	MMUART_3_RXD_F2M	B21 (RXD)	B1_GPIO21_P	JM2-Pin 38	JB2-Pin 37			
COREUAR Tapb	COREUAR_T_TX	A7 (TXD)	B1_GPIO17_3_P	JM1-Pin 65	JB1-Pin 66	Additional UART interface	Depends on system clock frequency. $Baud_rate = clk / (Baudval+1)^{16}$ and $Baudval = (clk / (1+Baudrate)) - 1$	This UART interface works via COREUAR Tapb in Libero. This UART interface is an optional UART interface for customer. It is necessary to provide other required features same as design in linux to put this interface in application.
	COREUAR_T_RX	H15 (RXD)	B1_GPIO7_N	JM2-Pin 66	JB2-Pin 65			
UART4	USER_UAR_T4_TX	B20 (TXD)	B1_GPIO19_P	JM2-Pin 46	JB2-Pin 45	Additional UART interface	----	This UART interface is an optional UART interface for customer. It is necessary to provide other required features same as design in linux to put this interface in application.
	USER_UAR_T4_RX	A21 (RXD)	B1_GPIO20_N	JM2-Pin 32	JB2-Pin 31			
	USER_UAR_T4_INT	A20 (INT)	B1_GPIO20_P	JM2-Pin 34	JB2-Pin 33			

I2C	FPGA Pin	Schematic label	New design label	Connected to	Access on the carrier board via	Description
I2C0	A3 (SCL)	I2C_CON_SCL	I2C_0_SCL	JM1-Pin 95	JB1-Pin 96 (SCL)	In the reference design is connected no device on the module or carrier. Therefore in linux cosole exists this interface but by typing i2cdetect command no device will be find.
	E3 (SDA)	I2C_CON_SDA	I2C_0_SDA	JM1-Pin 93	JB1-Pin 94 (SDA)	
I2C1	C1 (SCL)	I2C_SCL	I2C_1_SCL	EEPROM chip U10 SCL pin	No Access	In the reference design is used this i2c to access EEPROM on the TEM0007 module. (Address 0x50)
	B1 (SDA)	I2C_SDA	I2C_1_SDA	EEPROM chip U10 SDA pin	No Access	
USER_I2C0	B8 (SCL)	B1_GPIO175_N	USER_I2C0_SCL	JM1-Pin 62	JB1-Pin 61	This additional i2c interface in generated via COREI2C. This I2C interface is an optional i2c interface for customer. It is necessary to provide other required features same as design in linux to put this interface in application.
	A8 (SDA)	B1_GPIO175_P	USER_I2C0_SDA	JM1-Pin 60	JB1-Pin 59	
USER_I2C1	F10 (SCL)	B1_GPIO180_N	USER_I2C1_SCL	JM2-Pin 85	JB2-Pin 86	This additional i2c interface in generated via COREI2C. This I2C interface is an optional i2c interface for customer. It is necessary to provide other required features same as design in linux to put this interface in application.
	B9 (SDA)	B1_GPIO179_N	USER_I2C1_SDA	JM1-Pin 68	JB1-Pin 67	

Ethernet

Signal	FPGA Pin	Schematic label	New design label	Connected to	Access on the carrier board via	Description
MAC_0_MDIO	J3	ETH_MDIO	MAC_0_MDIO	Ethernet Phy Chip (Marvell 88E1512-A0-NNP2I000) Pin 8	No Access	
MAC_0_MDO	H6	ETH_MDO	MAC_0_MDO	Ethernet Phy Chip (Marvell 88E1512-A0-NNP2I000) Pin 7	No Access	

GPIOs

GPIO	FPGA Pin	Schematic label	Connected to	Access on the carrier board via	Description
GPIO_1_16 (ETH_PHY_RESET)	E5	ETH_RST	Marvell 88E1512-A0-NNP2I000 ethernet phy chip reset pin (Pin 16 RESETn)	No Access	
GPIO_1_17 (USB_PHY_RESET)	E4	OTG-RST	Microchip USB3320C-EZK USB phy chip reset pin (Pin 27 RESETB)	No Access	
GPIO_1_20	B3	GPIO1	B2B JM1-Pin 91	B2B JB1-Pin 92	
GPIO_1_23	D4	GPIO0	B2B JM1-Pin 87	B2B JB1-Pin 88	
GPIO_2_2	D9	GPIO174_P	JM1-Pin 69	JB1-Pin 70	
GPIO_2_3	D6	GPIO168_N	JM1-Pin 88	JB1-Pin 87	
GPIO_2_4	C6	GPIO171_P	JM1-Pin 83	JB1-Pin 84	
GPIO_2_5	H17	GPIO8_N	JM2-Pin 62	JB2-Pin 61	
GPIO_2_7	B5	GPIO170_N	JM1-Pin 70	JB1-Pin 69	
GPIO_2_8	C5	GPIO170_P	JM1-Pin 72	JB1-Pin 71	
GPIO_2_9	C4	GPIO169_P	JM1-Pin 77	JB1-Pin 78	
GPIO_2_10	F11	GPIO181_N	JM2-Pin 65	JB2-Pin 66	
GPIO_2_11	F16	GPIO11_N	JM2-Pin 41	JB2-Pin 42	
GPIO_2_12	D14	GPIO2_N	JM1-Pin 46	JB1-Pin 45	
GPIO_2_13	E14	GPIO9_N	JM2-Pin 57	JB2-Pin 58	
GPIO_2_14	B4	GPIO169_N	JM1-Pin 75	JB1-Pin 76	
GPIO_2_15	G17	GPIO8_P	JM2-Pin 64	JB2-Pin 63	

User IOs

Input	FPGA Pin	Schematic label	New design label	Connected to	Access on the carrier board via	Description
USER_IN0	V19	B0_HSIO72_N	USER_IN0	JM3-Pin 42	JB3-Pin 41	

Output	FPGA Pin	Schematic label	New design label	Connected to	Access on the carrier board via	Description
USER_OUT0	AB19	B0_HSIO70_P	USER_OUT0	JM3-Pin 60	JB3-Pin 59	

PWM

Signal	FPGA Pin	Schematic label	New design label	Connected to	Access on the carrier board via	Description
PWM	E11	B1_GPIO183_N	USER_PWM0	JM1-Pin 82	JB1-Pin 81 / J1C-Pin C4	This PWM generator is an optional feature for customer. It is necessary to provide other required features same as design in linux to put PWM generator in application.

LED

Unfortunately on the TEM0007 module exists no LED. But the LEDs on the TE0703 can be used for various purposes. For the no edited CPLD Firmware code of TE0703 the LEDs have the following functions as shown in this table:

LED	Prio. 0: Power	Prio. 1: Module CPLD access*	Prio. 2	Description
LED1 (D1-red)	Blink, if Power Good is low	ON	FTDI UART RX	
LED2 (D2-green)	Blink, if Power Good is low	ON	FTDI UART TX	
LED3 (D3-red)	OFF	ON	User defined with B2B Pin JB2-99	
LED4 (D4-green)	OFF	ON	User defined with B2B Pin JB2-90	

PHY LEDs (green /orange)	Blink orange, if Power Good is low	Blink Green and orange	-----	
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* Attention: LED1,2,3,4 are on, if S2-2 is set to OFF. If S2-3 is OFF, TE0703 is in chain!