

# TEI0006 Test Board

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Quartus Design with NIOS V/m and software example "simple\_socket\_server" and "hello\_tei0006".

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Refer to <http://trac.ti.com/te0006/info> for the online version of this manual and other available documentation.

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## Key Features

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Date	Quartus	Project Built	Authors	Description
2024-01-09	22.4 Pro	TEI0006-test_board- it-quartus_22.4.0- 20240109135625.zip	Thomas Dück	<ul style="list-style-type: none"><li>Fixed bugs in TE scripts</li></ul>
2023-12-04	22.4 Pro	TEI0006- test_board_noprebui lt-quartus_22.4.0- 20231204134534.zip	Thomas Dück	<ul style="list-style-type: none"><li>update to Quartus Prime Pro 22.4</li><li>TE scripts update</li><li>new assembly variants</li></ul>
2023-04-13	20.4 Pro	TEI0006- test_board_noprebui lt-quartus_20.4.0- 20230411171022.zip	Thomas Dück	<ul style="list-style-type: none"><li>change "Serial Flash Controller II" IP Core to "QUAD SPI Controller II" IP Core</li><li>bugfix offset value of hex file</li></ul>

2021-06-15	20.4 Pro	TEI0006-test_board_noprebui lt-quartus_20.4.0- 20210615142627.zip  TEI0006-test_board- quartus_20.4.0- 20210615142455.zip	Thomas Dück	<ul style="list-style-type: none"> <li>• update to Quartus Prime Pro 20.4</li> <li>• TE scripts update</li> <li>• new assembly variants</li> </ul>
2020-10-19	19.4 Pro	TEI0006-test_board_noprebui lt-quartus_19.4.0- 20201019101920.zip  TEI0006-test_board- quartus_19.4.0- 20201019101840.zip	Thomas Dück	<ul style="list-style-type: none"> <li>• script update</li> <li>• bugfixes</li> </ul>
2020-05-13	19.4 Pro	TEI0006-test_board_noprebui lt-quartus_19.4.0- 20200513124953.zip  TEI0006-test_board- quartus_19.4.0- 20200513125247.zip	Thomas Dück	<ul style="list-style-type: none"> <li>• TE scripts update</li> </ul>
2020-03-09	19.4 Pro	TEI0006-test_board- quartus_19.4- 20200309134933.zip TEI0006- test_board_noprebui lt-quartus_19.4- 20200309135555.zip	Thomas Dück	<ul style="list-style-type: none"> <li>• initial release</li> </ul>

#### Design Revision History

## Release Notes and Know Issues

Issues	Description	Workaround	To be fixed version
No known issues	---	---	---

#### Known Issues

## Requirements

### Software

Software	Version	Note
Quartus Prime Pro	22.4	Nios V/m license is needed. For more information see: <a href="#">Intel Nios V Processors</a>
Ashling RiscFree IDE for Intel FPGAs	22.4	needed

#### Software

### Hardware

Complete List is available on <project folder>/board\_files/\*\_devices.csv

Design supports following modules:

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	Others	Notes
TEI0006-03-220-5I*	220_5I_2GB	REV03 REV02 REV01	2GB	128MB	--	--
TEI0006-03-APC13-R	APC13R	REV03	128MB	128MB	--	without ETH PHY
TEI0006-03-ANC13-R	ANC13R	REV03	128MB	128MB	--	without ETH PHY
TEI0006-03-ALC13-R	ALC13R	REV03	128MB	128MB	--	without ETH PHY
TEI0006-03-ALC13	ALC13	REV03	128MB	128MB	--	--
TEI0006-04-ALC13A	ALC13	REV04	128MB	128MB	--	--
TEI0006-04-ALE13A	ALE13	REV04	128MB	128MB	--	--
TEI0006-04-ANE13A	ANE13	REV04	128MB	128MB	--	--
TEI0006-04-APE23A	APE23	REV04	2GB	128MB	--	--
TEI0006-04-API23A	API23	REV04	2GB	128MB	--	--
TEI0006-04-S004	API23R	REV04	2GB	128MB	--	without ETH PHY
TEI0006-04-S005	APE23	REV04	2GB	128MB	--	--
TEI0006-04-S006	BPI23	REV04	2GB	128MB	--	--
TEI0006-04-S007	APE23R	REV04	2GB	128MB	--	without ETH PHY

\*used as reference

#### Hardware Modules

Design supports following carriers:

Carrier Model	Notes
TEIB0006*	

\*used as reference

#### Hardware Carrier

Additional HW Requirements:

Additional Hardware	Notes
USB cable for JTAG/UART	Check Carrier Board and Programmer for correct type
RJ45 ethernet cable	connect carrier board to network

## Additional Hardware

## Content

For general structure and of the reference design, see [Project Delivery - Intel devices](#)

## Design Sources

Type	Location	Notes
Quartus	<project folder>/source_files /quartus	Quartus project will be generated by TE Scripts
	<project folder>/source_files /<Board Part Short Name> /quartus	optional, source files for specific assembly variants
Software	<project folder>/source_files /software	Additional software will be generated by TE Scripts

### Design sources

## Prebuilt

File	File-Extension	Description
SOPC Information File	*.sopcinfo	File with description of the .qsys file to create software for the target hardware
SRAM Object File	*.sof	Ram configuration file
JTAG indirect configuration file	*.jic	Flash configuration file
Diverse Reports	---	Report files in different formats
Software-Application-File	*.elf	Software application for NIOS II processor system

### Prebuilt files (only on ZIP with prebuilt content)

## Download

Reference Design is only usable with the specified Quartus version. Do never use different versions of Quartus software for the same project.

Reference Design is available on:

- [TEI0006 "Test Board" Reference Design](#)

## Design Flow



Reference Design is available with and without prebuilt files. It's recommended to use TE prebuilt files for first launch.

Trenz Electronic provides a tcl based built environment based on Quartus Design Flow.

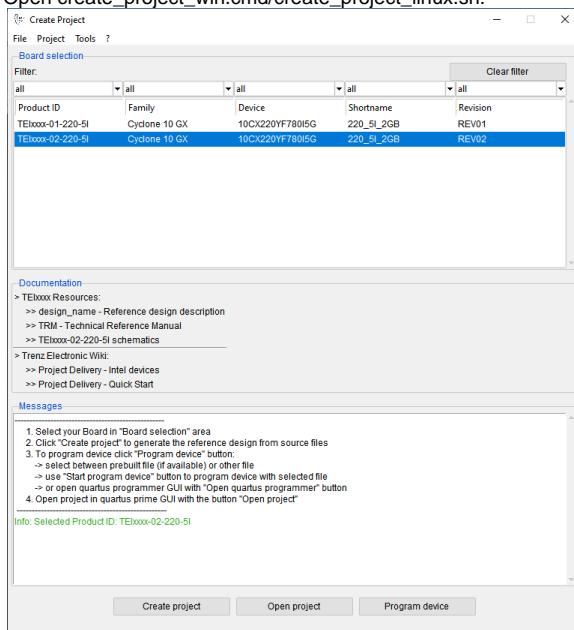
See also:

- [Project Delivery - Intel devices](#)

The Trenz Electronic FPGA Reference Designs are TCL-script based projects. To create a project, open a project or program a device execute "create\_project\_win.cmd" on Windows OS and "create\_project\_linux.sh" on Linux OS.

TE Scripts are only needed to generate the quartus project, all other additional steps are optional and can also be executed by Intel Quartus/SDK GUI. For currently Scripts limitations on Win and Linux OS see: [Project Delivery - Intel devices](#) [Currently limitations of functionality](#)

1. Open create\_project\_win.cmd/create\_project\_linux.sh:



'Create Project' GUI example

2. Select Board in "Board selection"
3. Click on "Create project" button to create project
  - a. (optional for manual changes) Select correct quartus installation path in "<project folder>/settings/design\_basic\_settings.tcl"

## Launch

## Programming



Check Module and Carrier TRMs for proper HW configuration before you try any design.

Reference Design is also available with prebuilt files. It's recommended to use TE prebuilt files for first launch.

## Get prebuilt boot binaries

1. Run create\_project\_win.cmd/create\_project\_linux.sh
2. Select a Module in 'Board selection'
3. Click on the 'Export prebuilt files' button

- a. Folder `<project folder>/_binaries_<Article Name>` with subfolder `boot_linux` will be generated and opened

## QSPI

1. Connect JTAG and power on carrier with module
2. Open `create_project_win.cmd/create_project_linux.sh`
3. Select correct board in "Board selection"
4. Click on "Program device" button
  - a. if prebuilt files are available: select "Program prebuilt file"
  - b. using own generated programming file: select "Program other file" and click on "Browse ..." to open own generated programming file
  - c. (optional) click on "Open programmer GUI" to program device with Quartus programmer GUI
5. Click on "Start program device" button

## JTAG

Not used on this Example.

## Usage

1. Prepare HW like described on section [Programming](#)
2. Connect UART USB (most cases same as JTAG)
3. Connect your board to the network
4. Power on PCB

## UART

1. Open Serial Console (e.g. PuTTY)
  - a. select COM Port



Win OS: see device manager

Linux OS: see `ls -l dev/serial/by-id` (UART is \*USB1)

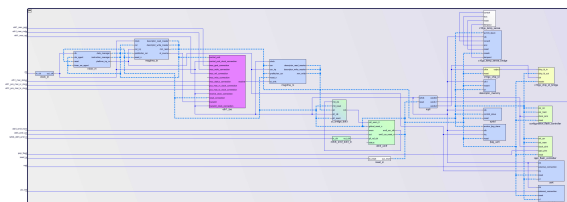
- b. Speed: 115200
2. Press reset button
3. Console output depends on used Software project, see [Software Design - SDK#Application](#)

## System Design - Quartus

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### Block Design

The block design may differ depending on the assembly variant.



Block Design - NIOS\_test\_board.qsys

**Block Design - Platform Designer**

# Software Design - SDK

## Application

Used software project depends on board assembly variant. Template location: <project folder>/source\_files/software/

### hello\_tei0006

Hello TEI0006 is a Hello World example as endless loop instead of one console output.

### simple\_socket\_server

Software example "Simple Socket Server" from eclipse (modified source files for TEI0006 board).

- If DHCP Server is not available:
  1. Open software project in sdk gui (e.g. Ashling RiscFree IDE for Intel FPGAs 22.4) and set in the main.c file the varaibles:
    - .use\_dhcp = !DEF\_TRUE
    - .ipv4\_addr\_str = <your static IP address>
    - .ipv4\_gateway\_str =<your gateway>
  2. Rebuild the software project and download the \*.elf file to the device.
  3. Open the command shell and enter "telnet <ip\_address> 80" to connect to the simple socket server

# Appx. A: Change History and Legal Notices

## Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

Date	Document Revision	Authors	Description
Error rendering macro 'page-info' Ambiguous method overload	Error rendering macro 'page-info' Ambiguous method overload	Error rendering macro 'page-info' Ambiguous method overload	<ul style="list-style-type: none"><li>• update to Quartus Prime Pro 22.4</li><li>• new assembly variants</li></ul>

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2023-04-13	v.12	Thomas Dück	• Design files update

2021-07-26	v.10	Thomas Dück	<ul style="list-style-type: none"> <li>• update to Quartus Prime Pro 20.4</li> <li>• new assembly variants</li> <li>• document style update</li> <li>• script update</li> </ul>
2020-10-19	v.6	Thomas Dück	<ul style="list-style-type: none"> <li>• script update</li> <li>• bugfixes</li> </ul>
2020-05-13	v.5	Thomas Dück	<ul style="list-style-type: none"> <li>• Design files update</li> </ul>
2020-03-18	v.4	Thomas Dück	<ul style="list-style-type: none"> <li>• initial release 19.4</li> </ul>
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Document change history

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#### **Error rendering macro 'page-info'**

Ambiguous method overloading for method jdk.

proxy279.\$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]