

# TEM0007 CPLD

## Overview

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Firmware for PCB CPLD with designator U1: LCMXO2-256HC-4SG32I

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## Feature Summary

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## Firmware Revision and supported PCB Revision

See Document [Change History](#)

## Product Specification

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## Port Description

Name / opt. VHD Name	Direction	Pin	Pullup/Down	Bank Power	Description
TDO	out	1	NONE	3.3V	JTAG TDO signal connected to FTDI chip via B2B connector
TDI	in	32	UP	3.3V	JTAG TDI signal connected to FTDI chip via B2B connector
TCK	in	30	NONE	3.3V	JTAG TCK signal connected to FTDI chip via B2B connector
TMS	in	29	UP	3.3V	JTAG TMS signal connected to FTDI chip via B2B connector
F_TDO	in	4	NONE	1.8V	JTAG TDO signal connected to FPGA
F_TDI	out	20	NONE	1.8V	JTAG TDI signal connected to FPGA
F_TCK	out	5	DOWN	1.8V	JTAG TCK signal connected to FPGA
F_TMS	out	21	NONE	1.8V	JTAG TMS signal connected to FPGA

EN_1V8	out	28	NONE	3.3V	Enable signal for U20 DC-DC converter 3.3V/1.8V
EN_2V5	out	27	NONE	3.3V	Enable signal for U21 DC-DC converter 3.3V/2.5V
EN_3V3	out	8	NONE	3.3V	Enable signal for U14 3.3V power switch
EN_1V0	out	9	NONE	3.3V	Enable signal for U13 DC-DC converter 3.3V/1.0V
EN_LPDDR4	out	10	NONE	3.3V	Enable signal for U18 DC-DC converter 3.3V/1.1V
EN_2V5_XCVR	out	23	NONE	3.3V	Enable signal for U19 DC-DC converter 3.3V/2.5V_XCVR
PG_ALL	in	13	NONE	3.3V	Power good input signal that is connected to all DC-DC converters U13,U18,U19,U20 and U21
SC_nRST	in	14	UP	3.3V	Reset input signal connected to reset push button on the carrier board directly or indirectly (depends on the used carrier board) via B2B connector.
SC_BOOTMODE	in	25	NONE	3.3V	Boot mode signal connected to B2B connector. This signal is connected with a dummy signal and does not have any function.
SC_EN1	in	11	UP	3.3V	Enable signal connected to B2B connector. This signal is connected with a dummy signal and does not have any function.
SC_PGOOD	inout	12	NONE	3.3V	PGOOD signal connected to B2B connector
NOSEQ	inout	17	UP	3.3V	NOSEQ signal connected to B2B connector. This signal is high as long as reset is not activated.

MR_n	out	16	NONE	3.3V	Reset output signal connected to DEVRST_N Polarfire device reset pin signal via voltage monitor chip U15 (TPS3106K33DBV R)
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## Functional Description

### JTAG

JTAG signals routed directly through the CPLD to FPGA. Access between CPLD and FPGA can be multiplexed via JTAGSEL pin of CPLD (pin 26) (logical one for CPLD, logical zero for FPGA). This pin is connected to B2B (JM1-pin 89) directly. On the carrier board can be this pin enabled or disabled with a dip switch.

CPLD JTAGSEL (B2B JM1-89)	Description
1	CPLD access
0	FPGA access

### Power

Power sequencing is necessary for this module. To implement a power sequencing a state machine is used. Note that the DC-DC converters do not have separate power good output. Therefore timers will be used to create desired delay for sequencing. The state machine stages are shown in the following table:

Stage	Enable Signal	Voltage Domain	Timer	Description
IDLE	---	---	---	The state machine will change its stage to PWR1 immediately after power on.
PWR1	Set EN_1V8	1.8V	Timer1 is active.	In this stage timer1 will be switched on. The stage will be changed to next stage (PWR2) after about 700 ms and timer1 will be turned off.
PWR2	Set EN_LPDDR4, EN_2V5, EN_3V3	1.1V , 2.5V, 3.3V	Timer2 is active.	In this stage timer2 will be switched on. The stage will be changed to next stage (PWR3) after about 700 ms and timer2 will be turned off.
PWR3	Set EN_1V0, EN_2V5_XCVR	1V , 2.5V	Timer3 is active.	In this stage timer3 will be switched on. The stage will be changed to next stage (READY) after about 700 ms and timer3 will be turned off.

READY	---	---	---	In this stage PG_ALL signal is monitored. If PG_ALL is high, state machine stays in this stage otherwise state machine will be changed to ERROR_SYS stage and CPLD will turn all DC-DC converters off.
ERROR_SYS	Reset all enable signals	1.8V,1V,1.1V,2.5V,3.3V	---	The state machine will stay in this stage and user should turn the board off and look for the cause of the error.

## Boot mode

Boot Mode is independent from 4x5 Boot mode pins SC\_BOOTMODE,SC\_PGOOD (see: [4 x 5 SoM Integration Guide#4x5SoMIntegrationGuide-4x5ModuleControllerIOs](#))

The TEM0007 module supports SD card boot mode and JTAG boot mode. The selection between SD card or other boot mode will be done in HSS.

## Reset

Reset pins are explained in detail in the following table:

Reset Pin	Direction in CPLD	Description
SC_nRST	in	Reset input signal connected to reset push button on the carrier board directly or indirectly (dependent on the used carrier board) via B2B connector.
MR_n	out	Reset output signal connected to DEVRST_N pin of Polarfire SoC through a voltage monitor chip U15 (TPS3106K33DBVR)

## Appx. A: Change History and Legal Notices

### Revision Changes

### Document Change History

To get content of older revision go to "Change History" of this page and select older document revision number.

Date	Document Revision	CPLD Firmware Revision	Supported PCB Revision	Authors	Description	Firmware release
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		REV01	REV01		<ul style="list-style-type: none"> <li>REV01 release</li> </ul>	SC-PGM-TEM0007-01_SCM0007-01_20230815.zip
<div>Error rendering macro 'page-info'</div> <div>Ambiguous method overloading for method jdk.proxy279.\$Proxy4022#</div>	<div>Error rendering macro 'page-info'</div> <div>Ambiguous method overloading for method jdk.proxy279.\$Proxy4022#</div>	<div>Error rendering macro 'page-info'</div> <div>Ambiguous method overloading for method jdk.proxy279.\$Proxy4022#</div>	<div>Error rendering macro 'page-info'</div> <div>Ambiguous method overloading for method jdk.proxy279.\$Proxy4022#</div>	<div>Error rendering macro 'page-info'</div> <div>Ambiguous method overloading for method jdk.proxy279.\$Proxy4022#</div>	<div>Error rendering macro 'page-info'</div> <div>Ambiguous method overloading for method jdk.proxy279.\$Proxy4022#</div>	<div>Error rendering macro 'page-info'</div> <div>Ambiguous method overloading for method jdk.proxy279.\$Proxy4022#</div>
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Ambiguous method overloading for method `jdk.proxy279.$Proxy4022#hasContentLevelPermission`.  
Cannot resolve which method to invoke for `[null, class java.lang.String, class com.atlassian.confluence.pages.Page]` due to overlapping prototypes between: `[interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]`  
`[interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]`