

# TE0813 StarterKit

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|            |          |                                                                                                                                       |                  |                                                                                                                        |
|------------|----------|---------------------------------------------------------------------------------------------------------------------------------------|------------------|------------------------------------------------------------------------------------------------------------------------|
| 2022-10-20 | 2021.2.1 | TE0813-StarterKit_noprebuilt-vivado_2021.2-build_19_20221020112739.zip<br>TE0813-StarterKit-vivado_2021.2-build_19_20221020112739.zip | Manuela Strücker | <ul style="list-style-type: none"> <li>Vivado 2021.2.1 release</li> <li>new variants</li> <li>script update</li> </ul> |
| 2021-11-16 | 2020.2   | TE0813-StarterKit_noprebuilt-vivado_2020.2-build_9_20211116073800.zip<br>TE0813-StarterKit-vivado_2020.2-build_9_20211116073742.zip   | John Hartfiel    | <ul style="list-style-type: none"> <li>new variants</li> </ul>                                                         |
| 2021-10-28 | 2020.2   | TE0813-StarterKit-vivado_2020.2-build_8_20211028142542.zip<br>TE0813-StarterKit_noprebuilt-vivado_2020.2-build_8_20211028142614.zip   | Manuela Strücker | <ul style="list-style-type: none"> <li>initial release</li> </ul>                                                      |

**Design Revision History**

## Release Notes and Know Issues

| Issues          | Description                                                                                                                               | Workaround/Solution                                   | To be fixed version |
|-----------------|-------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------|---------------------|
| Xilinx Software | Incompatibility of board files for ZynqMP with eMMC activated between 2021.2 and 2021.2.1 patch, see <a href="#">Xilinx Forum Request</a> | use corresponding board files for the Vivado versions | --                  |
| QSPI Flash      | Programming QSPI flash fails sometimes                                                                                                    | use Vivado 2019.2 for programming                     | --                  |

**Known Issues**

## Requirements

### Software

| Software            | Version | Note                                               |
|---------------------|---------|----------------------------------------------------|
| Vitis               | 2023.2  | needed, Vivado is included into Vitis installation |
| PetaLinux           | 2023.2  | needed                                             |
| SI ClockBuilder Pro | ---     | optional                                           |

**Software**

## Hardware

Basic description of TE Board Part Files is available on [TE Board Part Files](#).

Complete List is available on "<project folder>\board\_files\\*\_board\_files.csv"

Design supports following modules:

| Module Model       | Board Part Short Name | PCB Revision Support | DDR | QSPI Flash | EMMC | Others | Notes       |
|--------------------|-----------------------|----------------------|-----|------------|------|--------|-------------|
| TE0813-01-2AE11-A  | 2cg_1e_2gb            | REV01                | 2GB | 128MB      | NA   | NA     | NA          |
| TE0813-01-2AE11-AZ | 2cg_1e_2gb            | REV01                | 2GB | 128MB      | NA   | NA     | NA          |
| TE0813-01-2AE11-KZ | 2cg_1e_2gb            | REV01                | 2GB | 128MB      | NA   | NA     | NA          |
| TE0813-01-2BE11-A  | 2eg_1e_2gb            | REV01                | 2GB | 128MB      | NA   | NA     | NA          |
| TE0813-01-3AE11-A  | 3cg_1e_2gb            | REV01                | 2GB | 128MB      | NA   | NA     | NA          |
| TE0813-01-3BE11-A  | 3eg_1e_2gb            | REV01                | 2GB | 128MB      | NA   | NA     | NA          |
| TE0813-01-4AE11-A  | 4cg_1e_2gb            | REV01                | 2GB | 128MB      | NA   | NA     | NA          |
| TE0813-01-4BE11-A  | 4eg_1e_2gb            | REV01                | 2GB | 128MB      | NA   | NA     | NA          |
| TE0813-01-4BE11-AZ | 4eg_1e_2gb            | REV01                | 2GB | 128MB      | NA   | NA     | NA          |
| TE0813-01-4BE71-A  | 4eg_1e_4gb            | REV01                | 4GB | 128MB      | NA   | NA     | NA          |
| TE0813-01-4BE71-AZ | 4eg_1e_4gb            | REV01                | 4GB | 128MB      | NA   | NA     | NA          |
| TE0813-01-4BE81-A  | 4eg_1e_4gb            | REV01                | 4GB | 128MB      | NA   | NA     | NA          |
| TE0813-01-4BE81-AZ | 4eg_1e_4gb            | REV01                | 4GB | 128MB      | NA   | NA     | NA          |
| TE0813-01-4DE11-A  | 4ev_1e_2gb            | REV01                | 2GB | 128MB      | NA   | NA     | NA          |
| TE0813-01-4DE11-AZ | 4ev_1e_2gb            | REV01                | 2GB | 128MB      | NA   | NA     | NA          |
| TE0813-01-5DE11-A  | 5ev_1e_2gb            | REV01                | 2GB | 128MB      | NA   | NA     | NA          |
| TE0813-01-S003     | 2cg_1e_2gb            | REV01                | 2GB | 128MB      | NA   | NA     | without PLL |
| TE0813-02-2AE81-A  | 2cg_1e_4gb            | REV02                | 4GB | 128MB      | NA   | NA     | NA          |
| TE0813-02-2AE81-AK | 2cg_1e_4gb            | REV02                | 4GB | 128MB      | NA   | NA     | NA          |
| TE0813-02-2BE81-A  | 2eg_1e_4gb            | REV02                | 4GB | 128MB      | NA   | NA     | NA          |
| TE0813-02-3AE81-A  | 3cg_1e_4gb            | REV02                | 4GB | 128MB      | NA   | NA     | NA          |
| TE0813-02-3BE81-A  | 3eg_1e_4gb            | REV02                | 4GB | 128MB      | NA   | NA     | NA          |
| TE0813-02-4AE81-A  | 4cg_1e_4gb            | REV02                | 4GB | 128MB      | NA   | NA     | NA          |
| TE0813-02-4BE71-A  | 4eg_1e_4gb            | REV02                | 4GB | 128MB      | NA   | NA     | NA          |

|                   |            |       |     |       |    |    |    |
|-------------------|------------|-------|-----|-------|----|----|----|
| TE0813-02-4BE81-A | 4eg_1e_4gb | REV02 | 4GB | 128MB | NA | NA | NA |
| TE0813-02-4DE81-A | 4ev_1e_4gb | REV02 | 4GB | 128MB | NA | NA | NA |
| TE0813-02-5DE81-A | 5ev_1e_4gb | REV02 | 4GB | 128MB | NA | NA | NA |
| TE0813-02-5DI81-A | 5ev_1i_4gb | REV02 | 4GB | 128MB | NA | NA | NA |
| TE0813-02-S001    | 4eg_1i_8gb | REV02 | 8GB | 128MB | NA | NA | NA |

\*used as reference

#### Hardware Modules

Note: Design contains also Board Part Files for TE0818 only configuration, this board part files are not used for this reference design.

Design supports following carriers:

| Carrier Model | Notes                      |
|---------------|----------------------------|
| TEBF0818*     | Used as reference carrier. |

\*used as reference

#### Hardware Carrier

Additional HW Requirements:

| Additional Hardware | Notes                                                                                                                                       |
|---------------------|---------------------------------------------------------------------------------------------------------------------------------------------|
| DP Monitor          | Optional HW<br>Not all monitors are supported, also Adapter to other Standard can make trouble.<br>Design was tested with <b>DELL P2421</b> |
| USB Keyboard        | Optional HW<br>Can be used to get access to console which is show on DP                                                                     |
| USB Stick           | Optional HW<br>USB was tested with USB memory stick                                                                                         |
| SATA Disk           | Optional HW                                                                                                                                 |
| PCIe Card           | Optional HW                                                                                                                                 |
| ETH cable           | Optional HW<br>Ethernet works with DHCP, but can be setup also manually                                                                     |
| SD card             | with fat32 partition                                                                                                                        |

#### Additional Hardware

## Content

For general structure and usage of the reference design, see [Project Delivery - AMD devices](#)

## Design Sources

| Type      | Location                                                                                                                 | Notes                                                                                                         |
|-----------|--------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------|
| Vivado    | <project folder>\block_design<br><project folder>\constraints<br><project folder>\ip_lib<br><project folder>\board_files | Vivado Project will be generated by TE Scripts                                                                |
| Vitis     | <project folder>\sw_lib                                                                                                  | Additional Software Template for Vitis and apps_list.csv with settings automatically for Vitis app generation |
| PetaLinux | <project folder>\os\petalinux                                                                                            | PetaLinux template with current configuration                                                                 |

#### Design sources

## Additional Sources

| Type    | Location                           | Notes                                         |
|---------|------------------------------------|-----------------------------------------------|
| SI5338  | <project folder>\misc\PLL\SI5338_B | SI5338 Project with current PLL Configuration |
| init.sh | <project folder>\misc\sd           | Additional Initialization Script for Linux    |

#### Additional design sources

## Prebuilt

| File                               | File-Extension | Description                                                                       |
|------------------------------------|----------------|-----------------------------------------------------------------------------------|
| BIF-File                           | *.bif          | File with description to generate Bin-File                                        |
| BIN-File                           | *.bin          | Flash Configuration File with Boot-Image (Zynq-FPGAs)                             |
| BIT-File                           | *.bit          | FPGA (PL Part) Configuration File                                                 |
| Boot Script-File                   | *.scr          | Distro Boot Script file                                                           |
| DebugProbes-File                   | *.ltx          | Definition File for Vivado/Vivado Labtools Debugging Interface                    |
| Diverse Reports                    | ---            | Report files in different formats                                                 |
| Device Tree                        | *.dts          | Device tree (2 possible, one for u-boot and one for linux)                        |
| Hardware-Platform-Description-File | *.xsa          | Exported Vivado <a href="#">hardware description file</a> for Vitis and PetaLinux |
| LabTools Project-File              | *.lpr          | Vivado Labtools Project File                                                      |

|                           |       |                                                                              |
|---------------------------|-------|------------------------------------------------------------------------------|
| OS-Image                  | *.ub  | Image with Linux Kernel (On Petalinux optional with Devicetree and RAM-Disk) |
| Software-Application-File | *.elf | Software Application for Zynq or MicroBlaze Processor Systems                |

Prebuilt files (only on ZIP with prebuilt content)

## Download

Reference Design is only usable with the specified Vivado/Vitis/PetaLinux version. Do never use different Versions of Xilinx Software for the same Project.

Reference Design is available on:

- [TE0813 "StarterKit" Reference Design](#)

## Design Flow



Reference Design is available with and without prebuilt files. It's recommended to use TE prebuilt files for first launch.

Trenz Electronic provides a tcl based built environment based on Xilinx Design Flow.

See also:

- [AMD Development Tools#XilinxSoftware-BasicUserGuides](#)
- [Vivado Projects - TE Reference Design](#)
- [Project Delivery](#).

The Trenz Electronic FPGA Reference Designs are TCL-script based project. Command files for execution will be generated with "\_create\_win\_setup.cmd" on Windows OS and "\_create\_linux\_setup.sh" on Linux OS.

TE Scripts are only needed to generate the vivado project, all other additional steps are optional and can also executed by Xilinx Vivado/Vitis GUI. For currently Scripts limitations on Win and Linux OS see: [Project Delivery Currently limitations of functionality](#)



**Caution!** Win OS has a 260 character limit for path lengths which can affect the Vivado tools. To avoid this issue, use Virtual Drive or the shortest possible names and directory locations for the reference design (for example "x:\<project folder>")

1. Run \_create\_win\_setup.cmd/\_create\_linux\_setup.sh and follow instructions on shell:

#### `_create_win_setup.cmd/_create_linux_setup.sh`

```
-----Set design paths-----
-- Run Design with: _create_win_setup
-- Use Design Path: <absolute project path>
-----
-----TE Reference
Design-----
-----
-- (0) Module selection guide, project creation...prebuilt export...
-- (1) Create minimum setup of CMD-Files and exit Batch
-- (2) Create maximum setup of CMD-Files and exit Batch
-- (3) (internal only) Dev
-- (4) (internal only) Prod
-- (c) Go to CMD-File Generation (Manual setup)
-- (d) Go to Documentation (Web Documentation)
-- (g) Install Board Files from Xilinx Board Store (beta)
-- (a) Start design with unsupported Vivado Version (beta)
-- (x) Exit Batch (nothing is done!)
-----
Select (ex.: '0' for module selection guide)
```

2. Press 0 and enter to start "Module Selection Guide"
3. Create project and follow instructions of the product selection guide, settings file will be configured automatically during this process.
  - optional for manual changes: Select correct device and Xilinx install path on "design\_basic\_settings.cmd" and create Vivado project with "vivado\_create\_project\_gui mode.cmd"



Note: Select correct one, see also [Vivado Board Part Flow](#)

- **Important:** Use Board Part Files, which ends with \*\_tebf0818

4. Create hardware description file (.xsa file) for PetaLinux project and export to prebuilt folder

**run on Vivado TCL (Script generates design and export files into "<project folder>\prebuilt\hardware\<short name>")**

```
TE::hw_build_design -export_prebuilt
```



Using Vivado GUI is the same, except file export to prebuilt folder.

5. Create and configure your PetaLinux project with exported .xsa-file, see [PetaLinux KICKstart](#)
  - use TE Template from "<project folder>\os\petalinux"
  - use exported .xsa file from "<project folder>\prebuilt\hardware\<short name>". **Note:** HW Export from Vivado GUI creates another path as default workspace.
  - The build images are located in the "<plnx-proj-root>/images/linux" directory
6. Configure the **boot.scr** file as needed, see [Distro Boot with Boot.scr](#)
7. Copy PetaLinux build image files to prebuilt folder
  - copy **u-boot.elf**, **bl31.elf**, **image.ub** and **boot.scr** from "<plnx-proj-root>/images/linux" to prebuilt folder





"<project folder>\prebuilt\os\petalinux\<ddr size>" or "<project folder>\prebuilt\os\petalinux\<short name>"

#### 8. Generate Programming Files with Vitis

**run on Vivado TCL (Script generates applications and bootable files, which are defined in "test\_board\sw\_lib\apps\_list.csv")**

```
TE::sw_run_vitis -all
TE::sw_run_vitis (optional; Start Vitis from Vivado GUI or start
with TE Scripts on Vivado TCL)
```



TCL scripts generate also platform project, this must be done manually in case GUI is used. See [Vitis](#)

## Launch

## Programming



Check Module and Carrier TRMs for proper HW configuration before you try any design.

Reference Design is also available with prebuilt files. It's recommended to use TE prebuilt files for first launch.

Xilinx documentation for programming and debugging: [Vivado/Vitis/SDSoC-Xilinx Software Programming and Debugging](#)

## Get prebuilt boot binaries

1. Run `_create_win_setup.cmd/_create_linux_setup.sh` and follow instructions on shell
2. Press 0 and enter to start "Module Selection Guide"
  - a. Select assembly version
  - b. Validate selection
  - c. Select create and open delivery binary folder



Note: Folder "<project folder>\\_binaries\_<Article Name>" with subfolder "boot\_<app name>" for different applications will be generated

## QSPI-Boot mode

Option for **Boot.bin** on QSPI Flash.

1. Connect **JTAG** and power on carrier with module
2. Open Vivado Project with "vivado\_open\_existing\_project\_gui mode.cmd" or if not created, create with "vivado\_create\_project\_gui mode.cmd"



run on Vivado TCL (Script programs BOOT.bin on QSPI flash)

```
TE::pr_program_flash -swapp hello_te0813
```

3. Set Boot Mode to **QSPI-Boot**
  - Depends on Carrier, see carrier TRM.
  - TEBF0818 automatically changes the boot mode to SD when the SD card is inserted. Optional CPLD firmware without boot mode change for microSD slot is available in the download area

## SD-Boot mode

1. Copy **image.ub**, **boot.src** and **Boot.bin** on SD
  - use files from "<project folder>\\_binaries\_<Article Name>\boot\_linux" from generated binary folder, see: [Get prebuilt boot binaries](#)
  - or use prebuilt file location, see "<project folder>\prebuilt\file\_location.txt"
2. Set Boot Mode to SD-Boot.
  - Depends on Carrier, see carrier TRM.
3. Insert SD-Card in SD-Slot.

## JTAG

Not used on this Example.

## Usage

1. Prepare HW like described on section [Programming](#)
2. Connect UART USB (JTAG XMOD)
3. Select SD Card as Boot Mode (or QSPI - depending on step 1)



Note: See TRM of the Carrier, which is used.



Starting with Petalinux version 2020.1, the industry standard "Distro-Boot" boot flow for U-Boot was introduced, which significantly expands the possibilities of the boot process and has the primary goal of making booting much more standardised and predictable.

The boot options described above describe the common boot processes for this hardware; other boot options are possible.

For more information see [Distro Boot with Boot.scr](#)

4. (Optional) Insert PCIe Card (detection depends on Linux driver. Only some basic drivers are installed)
5. (Optional) Connect SATA Disc
6. (Optional) Connect DisplayPort Monitor (List of usable Monitors: <https://www.xilinx.com/support/answers/68671.html>)
7. (Optional) Connect Network Cable
8. Power On PCB

1. ZynqMP Boot ROM loads FSBL from SD/QSPI into OCM,
2. FSBL init the PS, programs the PL using the bitstream and loads PMU, ATF and U-boot from SD/QSPI into DDR,
3. U-boot loads Linux (**image.ub**) from SD/QSPI/... into DDR



## Linux

1. Open Serial Console (e.g. putty)
  - Speed: 115200
  - select COM Port



Win OS, see device manager, Linux OS see dmesg |grep tty (UART is \*USB1)

2. Linux Console:

```
# password disabled
petalinux login: root
Password: root
```



Note: Wait until Linux boot finished

3. You can use Linux shell now.

```
i2cdetect -y -r 0      (check I2C Bus)
dmesg | grep rtc       (RTC check)
udhcpc                (ETH0 check)
lsusb                  (USB check)
lspci                  (PCIe check)
```

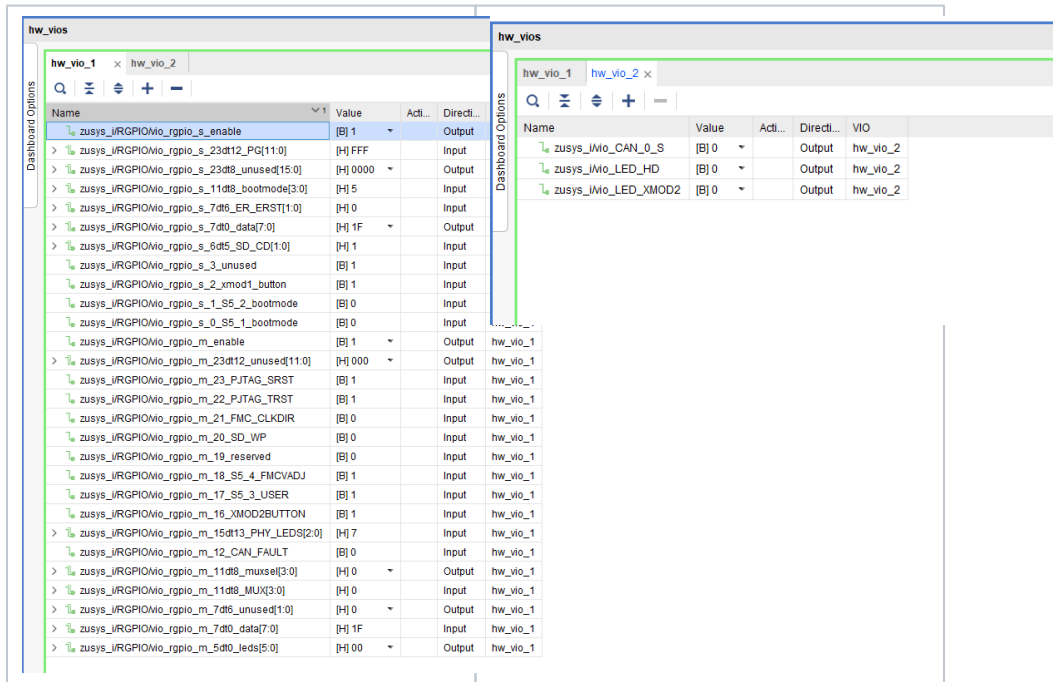
4. Option Features

- Webserver to get access to Zynq
  - insert IP on web browser to start web interface
- init.sh scripts
  - add init.sh script on SD, content will be load automatically on startup (template included in "<project folder>\misc\SD")

## Vivado Hardware Manager

Open Vivado HW-Manager and add VIO signal to dashboard (\*.ltx located on prebuilt folder).

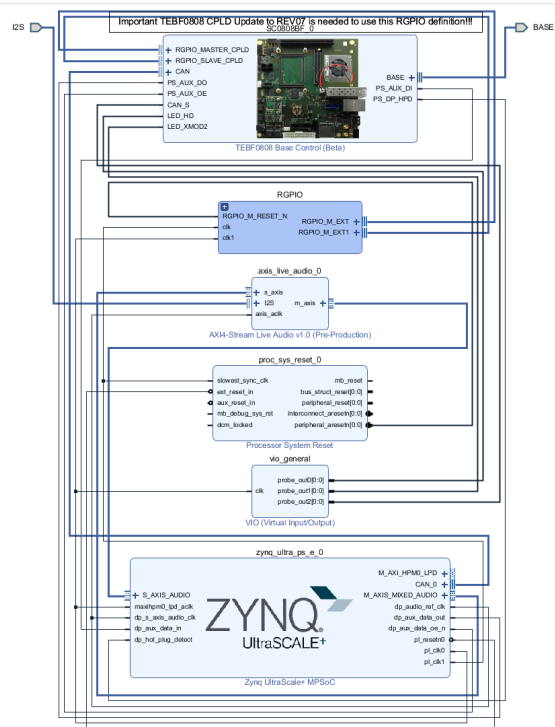
- RGPIO Interface (**Important:** CPLD Firmware REV07 or newer is needed) for Control and Monitoring:
  - Set Enable to send Write data over RGPIO interface.
    - **Important use CPLD Firmware REV07 or newer:** <https://wiki.trenz-electronic.de/display/PD/TEBF0818+CPLD>
      - Buttons, LEDs, Status...
- Control:
  - LEDs: XMOD 2 (without green dot) and HD LED are accessible.
  - CAN\_S



Vivado Hardware Manager

## System Design - Vivado

### Block Design



Block Design

## PS Interfaces

Activated interfaces:

| Type        | Note     |
|-------------|----------|
| DDR         |          |
| QSPI        | MIO      |
| SD0         | MIO      |
| SD1         | MIO      |
| CAN0        | EMIO     |
| I2C0        | MIO      |
| PJTAG0      | MIO      |
| UART0       | MIO      |
| GPIO0       | MIO      |
| SWDT0..1    |          |
| TTC0..3     |          |
| GEM3        | MIO      |
| USB0        | MIO/GTP  |
| PCIe        | MIO/GTP  |
| SATA        | GTP      |
| DisplayPort | EMIO/GTP |

#### PS Interfaces

## Constrains

### Basic module constrains

|                                                                                                                                            |
|--------------------------------------------------------------------------------------------------------------------------------------------|
| <b>_i_bitgen.xdc</b>                                                                                                                       |
| <pre>set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design] set_property BITSTREAM.CONFIG.UNUSEDPIN PULLNONE [current_design]</pre> |

### Design specific constrain

## \_i\_io.xdc

```
#TEBF0818
# system controller ip
#LED_HD SC0      J3:C13
#LED_XMOD SC17   J3:B19
#CAN RX SC19     J3:B23 B26_L2_P
#CAN TX SC18     J3:B22 B26_L2_N
#CAN S SC16      J3:B18 B26_L3_N

set_property PACKAGE_PIN J14 [get_ports BASE_sc0]
set_property PACKAGE_PIN F15 [get_ports BASE_sc5]
set_property PACKAGE_PIN H13 [get_ports BASE_sc6]
set_property PACKAGE_PIN H14 [get_ports BASE_sc7]
set_property PACKAGE_PIN A15 [get_ports BASE_sc10_io]
set_property PACKAGE_PIN B15 [get_ports BASE_sc11]
set_property PACKAGE_PIN C13 [get_ports BASE_sc12]
set_property PACKAGE_PIN C14 [get_ports BASE_sc13]
set_property PACKAGE_PIN E13 [get_ports BASE_sc14]
set_property PACKAGE_PIN E14 [get_ports BASE_sc15]
set_property PACKAGE_PIN A13 [get_ports BASE_sc16]
set_property PACKAGE_PIN B13 [get_ports BASE_sc17]
set_property PACKAGE_PIN A14 [get_ports BASE_sc18]
set_property PACKAGE_PIN B14 [get_ports BASE_sc19]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc0]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc5]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc6]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc7]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc10_io]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc11]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc12]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc13]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc14]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc15]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc16]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc17]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc18]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc19]

# Audio Codec
#LRCLK          J3:D22
#BCLK           J3:D23
#DAC_SDATA      J3:C21
#ADC_SDATA      J3:C22
set_property PACKAGE_PIN G14 [get_ports I2S_lrclk ]
set_property PACKAGE_PIN G15 [get_ports I2S_bclk ]
set_property PACKAGE_PIN F13 [get_ports I2S_sdin ]
set_property PACKAGE_PIN G13 [get_ports I2S_sdout ]
set_property IOSTANDARD LVCMOS18 [get_ports I2S_lrclk ]
set_property IOSTANDARD LVCMOS18 [get_ports I2S_bclk ]
set_property IOSTANDARD LVCMOS18 [get_ports I2S_sdin ]
set_property IOSTANDARD LVCMOS18 [get_ports I2S_sdout ]
```

For Vitis project creation, follow instructions from:

[Vitis](#)

## Application

Template location: "<project folder>\sw\_lib\sw\_apps\"

### zynqmp\_fsbl

TE modified 2023.2 FSBL

General:

- Modified Files: xfsbl\_main.c, xfsbl\_hooks.h/.c, xfsbl\_board.h/.c (search for 'TE Mod' on source code)
- Add Files: te\_xfsbl\_hooks.h/.c (for hooks and board)
- General Changes:
  - Display FSBL Banner and Device Name

Module Specific:

- Add Files: all TE Files start with te\_\*
  - Si5338 Configuration
  - OTG+PCIe Reset over MIO
  - I2C MUX for EEPROM MAC

### zynqmp\_pmufw

Xilinx default PMU firmware.

### hello\_te0813

Hello TE0813 is a Xilinx Hello World example as endless loop instead of one console output.

### u-boot

U-Boot.elf is generated with PetaLinux. Vitis is used to generate Boot.bin.

## Software Design - PetaLinux

---

For PetaLinux installation and project creation, follow instructions from:

- [PetaLinux KICKstart](#)

## Config

Start with **petalinux-config** or **petalinux-config --get-hw-description**

Activate:

- select SD default instead of eMMC:

- CONFIG\_SUBSYSTEM\_PRIMARY\_SD\_PSU\_SD\_1\_SELECT=y
- add new flash partition for bootscr and sizing
  - CONFIG\_SUBSYSTEM\_FLASH\_PSU\_QSPI\_0\_BANKLESS\_PART0\_SIZE=0xA00000
  - CONFIG\_SUBSYSTEM\_FLASH\_PSU\_QSPI\_0\_BANKLESS\_PART1\_SIZE=0x2000000
  - CONFIG\_SUBSYSTEM\_FLASH\_PSU\_QSPI\_0\_BANKLESS\_PART2\_SIZE=0x40000
  - CONFIG\_SUBSYSTEM\_FLASH\_PSU\_QSPI\_0\_BANKLESS\_PART3\_NAME="bootscr"
  - CONFIG\_SUBSYSTEM\_FLASH\_PSU\_QSPI\_0\_BANKLESS\_PART3\_SIZE=0x80000
- Identification
  - CONFIG\_SUBSYSTEM\_HOSTNAME="Trenz"
  - CONFIG\_SUBSYSTEM\_PRODUCT="TE0813\_TEBF0818"

## U-Boot

Start with **petalinux-config -c u-boot**

Changes:

- MAC from eeprom together with uboot and device tree settings:
  - CONFIG\_ENV\_OVERWRITE=y
  - CONFIG\_NVMEM=y
  - CONFIG\_DM\_RTC=y (needed for nvmem driver because of bug in uboot)
- Boot Modes:
  - CONFIG\_QSPI\_BOOT=y
  - CONFIG\_SD\_BOOT=y
  - CONFIG\_ENV\_IS\_IN\_FAT is not set
  - CONFIG\_ENV\_IS\_IN\_NAND is not set
  - CONFIG\_ENV\_IS\_IN\_SPI\_FLASH is not set
  - CONFIG\_BOOT\_SCRIPT\_OFFSET=0x2A40000
- Identification
  - CONFIG\_IDENT\_STRING=" TE0813\_TEBF0818"

Change platform-top.h:

## Device Tree

project-spec\meta-user\recipes-bsp\device-tree\files\system-user.dtsi

```
/include/ "system-conf.dtsi"

/*----- gtr -----*/

//https://xilinx-wiki.atlassian.net/wiki/spaces/A/pages/18841716
//Zynq+Ultrascale+MPSOC+Linux+SI0U+driver
/ {
    refclk3:psgtr_dp_clock {
        compatible = "fixed-clock";
        #clock-cells = <0x00>;
        clock-frequency = <270000000>;
    };

    refclk2:psgtr_pcie_usb_clock {
        compatible = "fixed-clock";
        #clock-cells = <0x00>;
        clock-frequency = <100000000>;
    };
};
```



```

    refclk1:psgtr_sata_clock {
        compatible = "fixed-clock";
        #clock-cells = <0x00>;
        clock-frequency = <150000000>;
    };

    refclk0:psgtr_unused_clock {
        compatible = "fixed-clock";
        #clock-cells = <0x00>;
        clock-frequency = <100000000>;
    };
};

&psgtr {
    clocks = <&refclk0 &refclk1 &refclk2 &refclk3>;
    //clocks = <&refclk0 &refclk2 &refclk3>;
    /* ref clk instances used per lane */
    clock-names = "ref0\0ref1\0ref2\0ref3";
};

/*----- SD -----*/
&sdhci0 {
    // disable-wp;
    no-1-8-v;
};

&sdhci1 {
    // disable-wp;
    no-1-8-v;
};

/*----- USB -----*/
&dwc3_0 {
    status = "okay";
    dr_mode = "host";
    snps,usb3_lpm_capable;
    snps,dis_u3_susphy_quirk;
    snps,dis_u2_susphy_quirk;
    phy-names = "usb2-phy", "usb3-phy";
    maximum-speed = "super-speed";
};

/*----- ETH PHY -----*/
&gem3 {
    /delete-property/ local-mac-address;
    phy-handle = <&phy0>;

    nvmem-cells = <&eth0_addr>;
    nvmem-cell-names = "mac-address";

    phy0: phy0@1 {
        device_type = "ethernet-phy";
        reg = <1>;
    };
};

```

```

/*----- SATA PHY -----*/
&sata {

    ceva,p0-burst-params = <0x13084a06>;
    ceva,p0-cominit-params = <0x18401828>;
    ceva,p0-comwake-params = <0x614080e>;
    ceva,p0-retry-params = <0x96a43ffc>;
    ceva,p1-burst-params = <0x13084a06>;
    ceva,p1-cominit-params = <0x18401828>;
    ceva,p1-comwake-params = <0x614080e>;
    ceva,p1-retry-params = <0x96a43ffc>;

};

/*----- QSPI -----*/
&qspi {
    #address-cells = <1>;
    #size-cells = <0>;
    status = "okay";
    flash0: flash@0 {
        compatible = "jedec,spi-nor";
        reg = <0x0>;
        #address-cells = <1>;
        #size-cells = <1>;

        spi-rx-bus-width = <4>;
        spi-tx-bus-width = <4>;
        spi-max-frequency = <90000000>;
    };
};

/*----- I2C -----*/
&i2c0 {
    i2cswitch@73 { // u
        compatible = "nxp,pca9548";
        #address-cells = <1>;
        #size-cells = <0>;
        reg = <0x73>;
        i2c-mux-idle-disconnect;
        i2c@0 { // MCLK TEBF0818 SI5338A, 570FBB000290DG_unassembled
            reg = <0>;
        };
        i2c@1 { // SFP TEBF0818 PCF8574DWR
            reg = <1>;
        };
        i2c@2 { // PCIE
            reg = <2>;
        };
        i2c@3 { // SFP1 TEBF0818
            reg = <3>;
        };
        i2c@4 { // SFP2 TEBF0818
            reg = <4>;
        };
        i2c@5 { // TEBF0818 EEPROM
            reg = <5>;
            eeprom: eeprom@50 {
                compatible = "microchip,24aa025", "atmel,24c02";
                reg = <0x50>;
            };
        };
    };
};

```

```

        #address-cells = <1>;
        #size-cells = <1>;
        eth0_addr: eth-mac-addr@FA {
            reg = <0xFA 0x06>;
        };
    };
};
i2c@6 { // TEBF0818 FMC
    reg = <6>;
};
i2c@7 { // TEBF0818 USB HUB
    reg = <7>;
};
};
i2cswitch@77 { // u
    compatible = "nxp,pca9548";
    reg = <0x77>;
    i2c-mux-idle-disconnect;
    i2c@0 { // TEBF0818 PMOD P1
        reg = <0>;
    };
    i2c@1 { // i2c Audio Codec
        reg = <1>;
        /*
        adau1761: adau1761@38 {
            compatible = "adi,adau1761";
            reg = <0x38>;
        };
        */
    };
    i2c@2 { // TEBF0818 Firefly A
        reg = <2>;
    };
    i2c@3 { // TEBF0818 Firefly B
        reg = <3>;
    };
    i2c@4 { //Module PLL Si5338 or SI5345
        reg = <4>;
    };
    i2c@5 { //TEBF0818 CPLD
        reg = <5>;
    };
    i2c@6 { //TEBF0818 Firefly PCF8574DWR
        reg = <6>;
    };
    i2c@7 { // TEBF0818 PMOD P3
        reg = <7>;
    };
};
};
};

```

## Kernel

Start with **petalinux-config -c kernel**

Changes:

- Only needed to fix JTAG Debug issue:
  - # CONFIG\_CPU\_FREQ is not set
- Support PCIe memory card
  - CONFIG\_NVME\_CORE=y
  - CONFIG\_BLK\_DEV\_NVME=y
  - # CONFIG\_NVME\_MULTIPATH is not set
  - # CONFIG\_NVME\_VERBOSE\_ERRORS is not set
  - # CONFIG\_NVME\_HWMON is not set
  - # CONFIG\_NVME\_AUTH is not set
  - CONFIG\_NVME\_TARGET=y
  - # CONFIG\_NVME\_TARGET\_PASSTHRU is not set
  - # CONFIG\_NVME\_TARGET\_LOOP is not set
  - # CONFIG\_NVME\_TARGET\_FC is not set
  - # CONFIG\_NVME\_TARGET\_TCP is not set
  - # CONFIG\_NVME\_TARGET\_AUTH is not set
  - CONFIG\_SATA\_AHCI=y
  - CONFIG\_SATA\_MOBILE\_LPM\_POLICY=0

## Rootfs

Start with **petalinux-config -c rootfs**

Changes:

- For web server app:
  - CONFIG\_busybox-httpd=y
- For additional test tools only:
  - CONFIG\_i2c-tools=y
  - CONFIG\_packagegroup-petalinux-utils=y (util-linux, cpufrequtils, bridge-utils, mtd-utils, usbutils, pciutils, canutils, i2c-tools, smartmontools, e2fsprogs)
- For auto login:
  - CONFIG\_imagefeature-serial-autologin-root=y

## FSBL patch (alternative for vitis fsbl trenz patch)

See "<project folder>\os\petalinux\project-spec\meta-user\recipes-bsp\embeddedsw"



te\_\* files are identical to files in "<project folder>\sw\_lib\sw\_apps\zynqmp\_fsbl\src".  
[Petalinux Troubleshoot#Petalinux2023.2](#)

## Applications

See "<project folder>\os\petalinux\project-spec\meta-user\recipes-apps\"

### startup

Script App to load init.sh from SD Card if available.

### webfwu

Webserver application suitable for ZynqMP access. Need busybox-httpd

## Additional Software

---

## SI5338

File location "<project folder>\misc\PLL\SI5338\_B\SI5338-\*.slabtimeproj"

General documentation how you work with this project will be available on [SI5338](#)

## Appx. A: Change History and Legal Notices

### Document Change History

To get content of older revision go to "Change History" of this page and select older document revision number.

| Date                                                                                                                                                                          | Document Revision                                                                                                                                                             | Authors                                                                                                                                                                       | Description                                                                                          |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------|
| <div>Error rendering macro 'page-info'</div> <div>Ambiguous method overload ing for method jdk. proxy27 9.\$Proxy 4022#hasContentLevelPermission . Cannot resolve which</div> | <div>Error rendering macro 'page-info'</div> <div>Ambiguous method overload ing for method jdk. proxy27 9.\$Proxy 4022#hasContentLevelPermission . Cannot resolve which</div> | <div>Error rendering macro 'page-info'</div> <div>Ambiguous method overload ing for method jdk. proxy27 9.\$Proxy 4022#hasContentLevelPermission . Cannot resolve which</div> | <div><ul style="list-style-type: none"><li>Release Vivado 2023.2</li><li>new variant</li></ul></div> |

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| 2023-09-27                                                                                                                                                                                                                                   | v.11                                                                                                                                                                                                                                         | Manuela Strücker                                                                                                                                                                                                                             | <ul style="list-style-type: none"> <li>new variants</li> </ul>                                                         |
| 2023-09-13                                                                                                                                                                                                                                   | v.10                                                                                                                                                                                                                                         | John Hartfiel                                                                                                                                                                                                                                | <ul style="list-style-type: none"> <li>Release Vivado 2022.2</li> <li>new variants</li> <li>script update</li> </ul>   |
| 2022-10-20                                                                                                                                                                                                                                   | v.6                                                                                                                                                                                                                                          | Manuela Strücker                                                                                                                                                                                                                             | <ul style="list-style-type: none"> <li>Release Vivado 2021.2.1</li> <li>new variants</li> <li>script update</li> </ul> |
| 2022-09-06                                                                                                                                                                                                                                   | v.4                                                                                                                                                                                                                                          | Manuela Strücker                                                                                                                                                                                                                             | <ul style="list-style-type: none"> <li>new variants</li> </ul>                                                         |
| 2021-10-28                                                                                                                                                                                                                                   | v.2                                                                                                                                                                                                                                          | Manuela Strücker                                                                                                                                                                                                                             | <ul style="list-style-type: none"> <li>Release 2020.2</li> </ul>                                                       |
|                                                                                                                                                                                                                                              | All                                                                                                                                                                                                                                          |                                                                                                                                                                                                                                              |                                                                                                                        |

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Trenz Electronic is registered under WEEE-Reg.-Nr. DE97922676.

#### Error rendering macro 'page-info'

Ambiguous method overloading for method jdk.  
proxy279.\$Proxy4022#hasContentLevelPermission. Cannot resolve which method to  
invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due  
to overlapping prototypes between: [interface com.atlassian.confluence.user.  
ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.  
ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class  
com.atlassian.confluence.core.ContentEntityObject]

