SD Card Interface

Zynq PS SDIO

SDIO MIO Settings in PS7 IP Configuration if external level shifter is used:

- speed (slew rate): slow
- pullup: disabled

> ⚠ It is important to disable the pull-ups, otherwise some SD card may exhibit systematic or random problem at initialization.

Peripheral	IO	Signal	IO Type	Speed	Pullup	Direction	Polarity
⊞ Memory Interfaces							
⊟ I/O Peripherals							
⊞ ☑ ENET 0	MIO 16 .. 27						
⊞ ☐ ENET 1							
⊞ ☑ USB 0	MIO 28 .. 39						
☐ USB 1							
⊟ ☑ SD 0	MIO 40 .. 45						
☑ CD	EMIO						
☑ WP	EMIO						
☐ Power							
SD 0	MIO 40	clk	LVCMOS 1.8V	slow	disabled	inout	
SD 0	MIO 41	cmd	LVCMOS 1.8V	slow	disabled	inout	
SD 0	MIO 42	data[0]	LVCMOS 1.8V	slow	disabled	inout	
SD 0	MIO 43	data[1]	LVCMOS 1.8V	slow	disabled	inout	
SD 0	MIO 44	data[2]	LVCMOS 1.8V	slow	disabled	inout	
SD 0	MIO 45	data[3]	LVCMOS 1.8V	slow	disabled	inout	

Bank 0 I/O Voltage: LVCMOS 3.3V; Bank 1 I/O Voltage: LVCMOS 1.8V

Example settings for SDIO MIO pins (TE0720), MIO pullups are disabled.
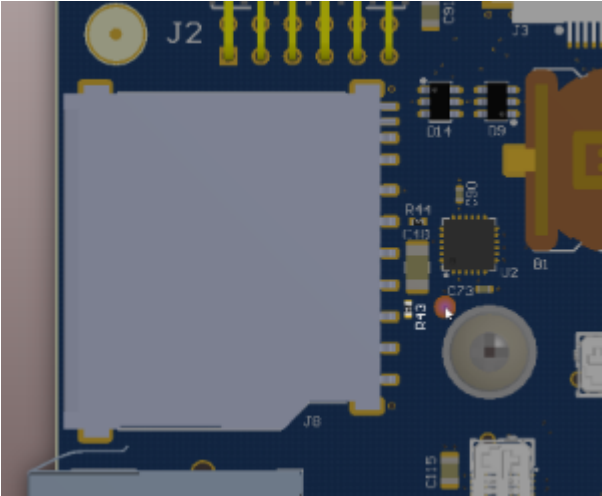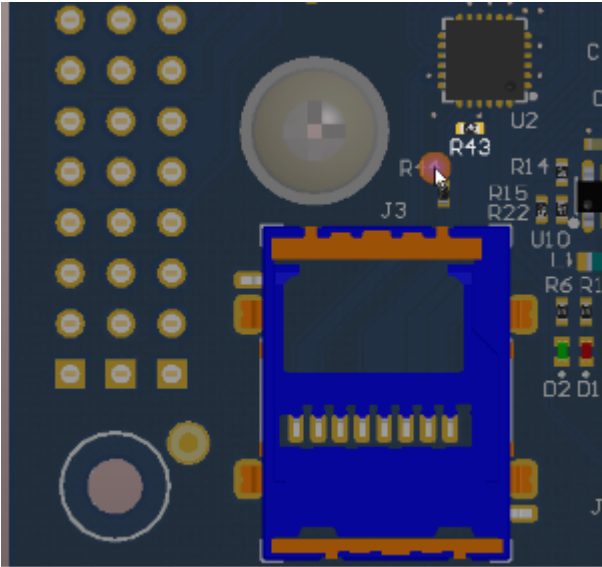
SDIO Peripheral Clock

This clock may as of Xilinx default sometimes be set to 125MHz, this would cause Xilinx FSBL to fail on clock lookup when setting SD clock to 400KHz. SDIO peripheral clock should be set to 100MHz or 50MHz.

Level shifter

Modules that expose SDIO Interface on the B2B Connector from 1.8V VCCIO bank need SD Level shifter IC on the baseboard.

> ⚠ When using TXS02612 as SDIO level shifter external pullups should not be used on CMD and DAT lines.

⚠️

TE0701 and TE0703 have pullup resistor on CMD line, which has been removed since:

Base	CMD pullup Resistor R43	Removed since
TE0701		TE0701-05 Serial number: TBD
TE0703		TE0703-04 Serial number: TBD

This extra pullup may cause problems in some special cases with some SD Cards. As example hama micro-SD Card when used with PS7 SDIO MIO pullups enabled and R43 loaded had sporadic initialization problems on TE0703, removing R43 solved the issue.

⚠️ Some other designs and boards that use TXS02612 may have pullup on CMD, this is incorrect as per TXS02612 datasheet. Xilinx ZC702 board that uses SDIO level shifter with similar technology has the CMD pullup in schematic with marking "DNP" do not populate.

When using SDIO level shifter from other vendors, or other level shifting technology then requirements listed in the vendor datasheet and application notes should be followed.

⚠️

References

- TXS02612 Documentation from TI
- ZC702 Documentation from Xilinx