

IBERT Test

The customizable IBERT core for 7 series FPGA can be used for evaluating and monitoring the GTs.

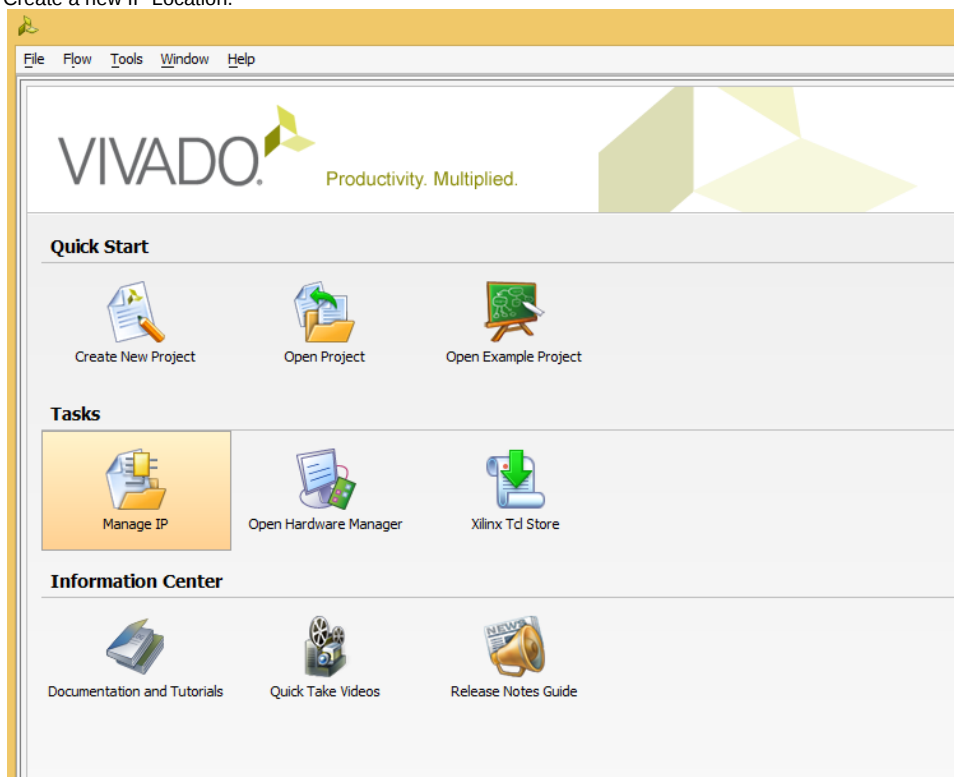
The IBERT core can be defined and generated using the Vivado built-in IP Cores. And with the generated example designs the IBERT Test can be implemented.

	Ref Clock Selection	GT Clock(MHz)	Notes
TE0712	MGTREFCLK0 216	125	
TE0715	MGTREFCLK1 112	125	
TE0741	MGTREFCLK1 116	125	Both Quads can use same refclock

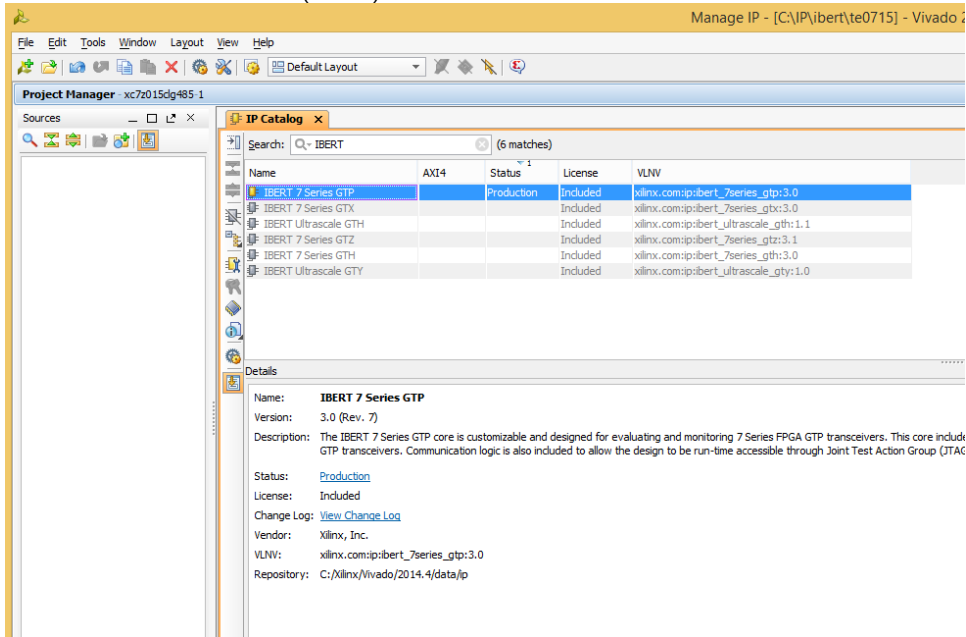
Ref clock selection to use on board fixed clock from Si5338.

Step to Step to generate the IBERT core:

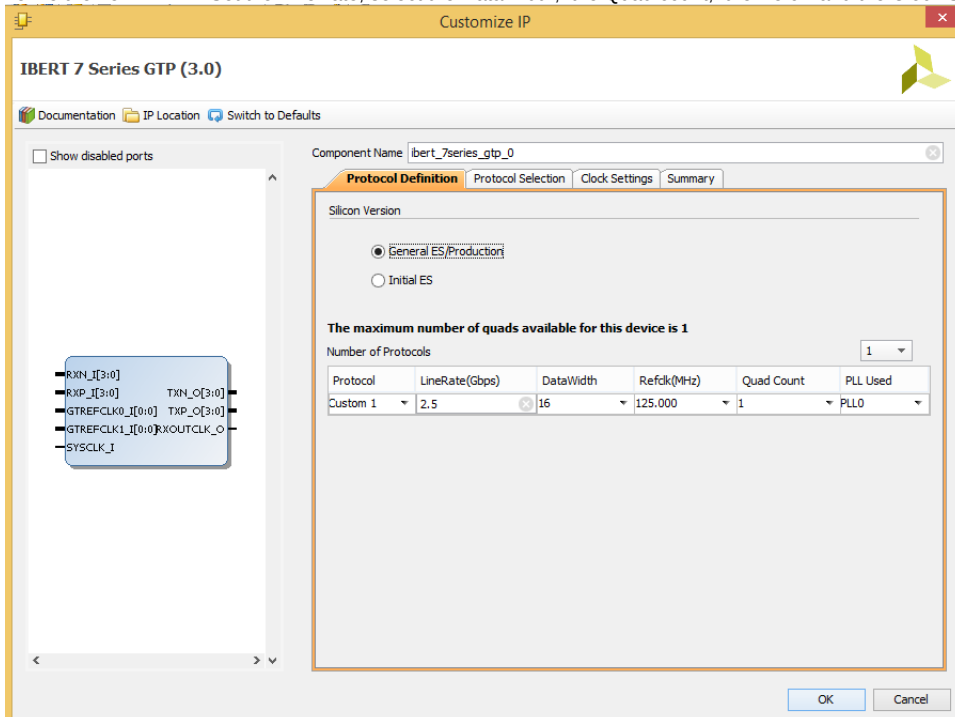
1. Create a new IP Location.

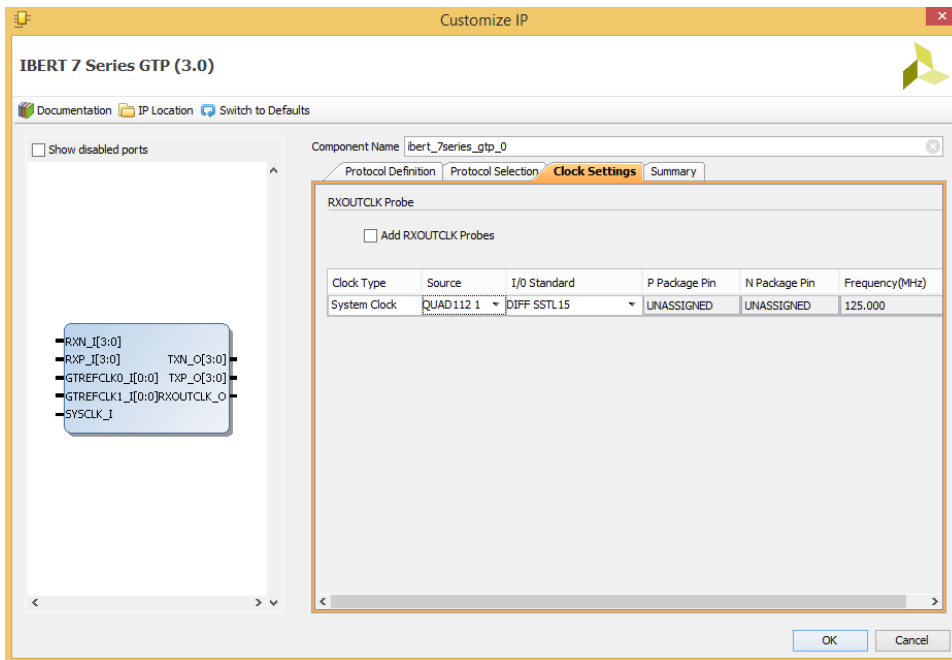
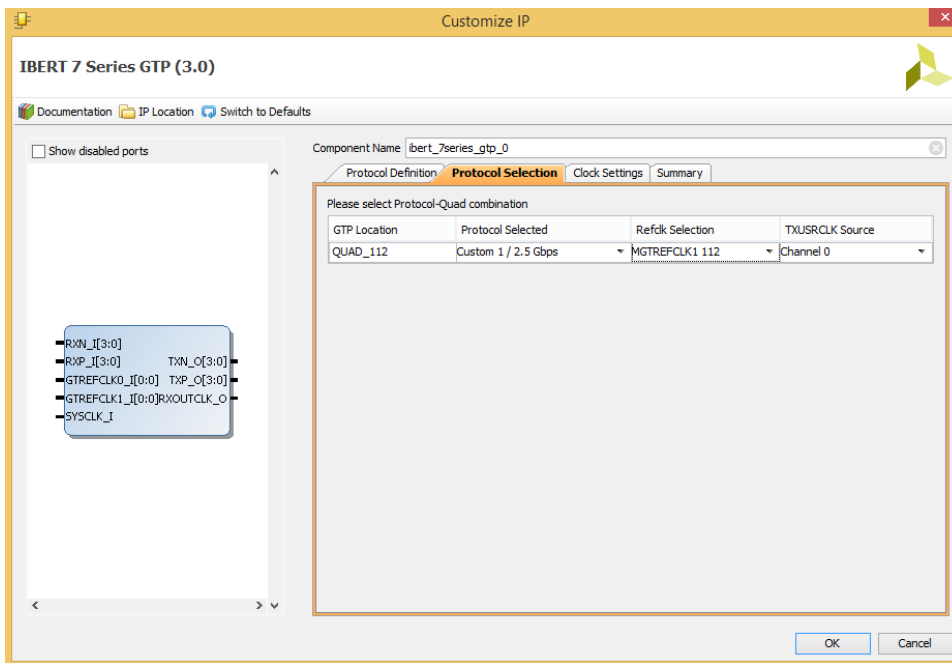


2. Double-click IBERT 7 series GTP (or GTX).

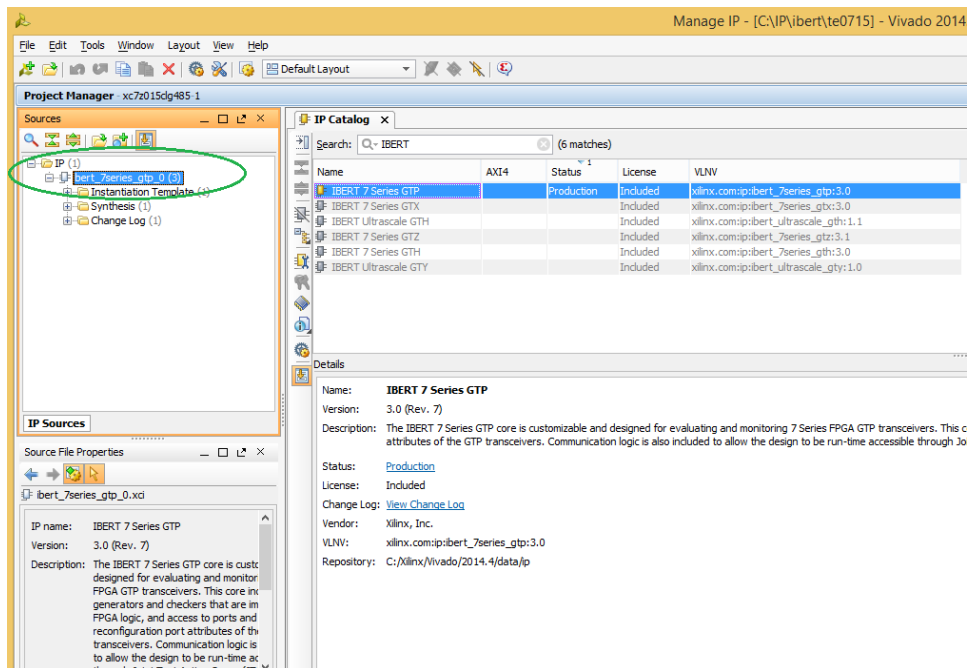
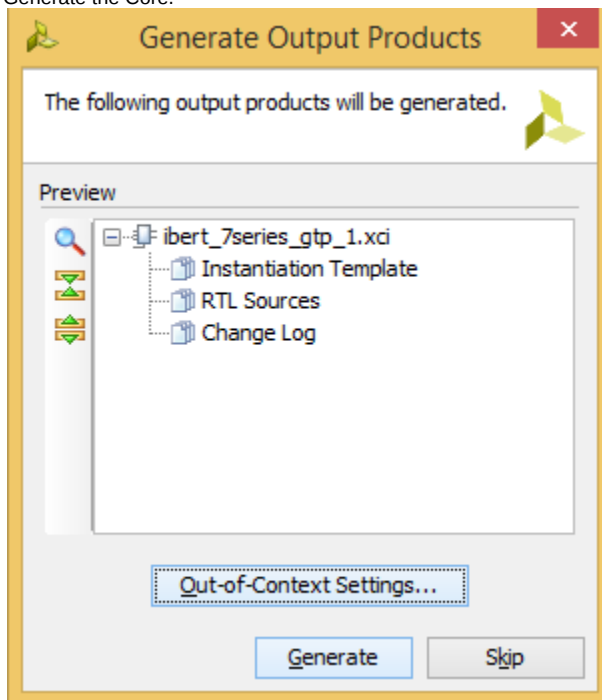


3. Define the new IBERT. Set the LineRate, select the DataWidth, the Quad count, the Refclk and the Clock Source.

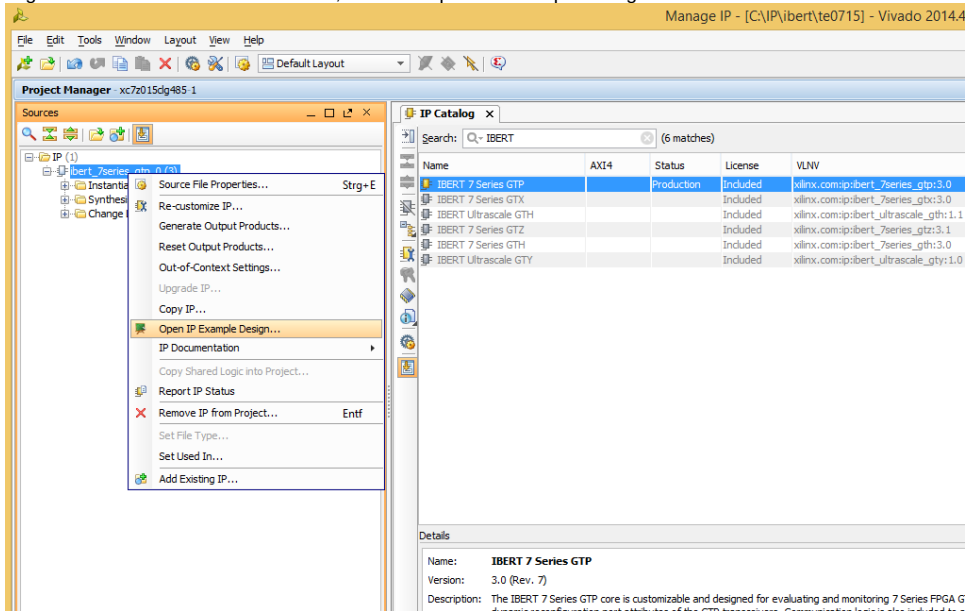




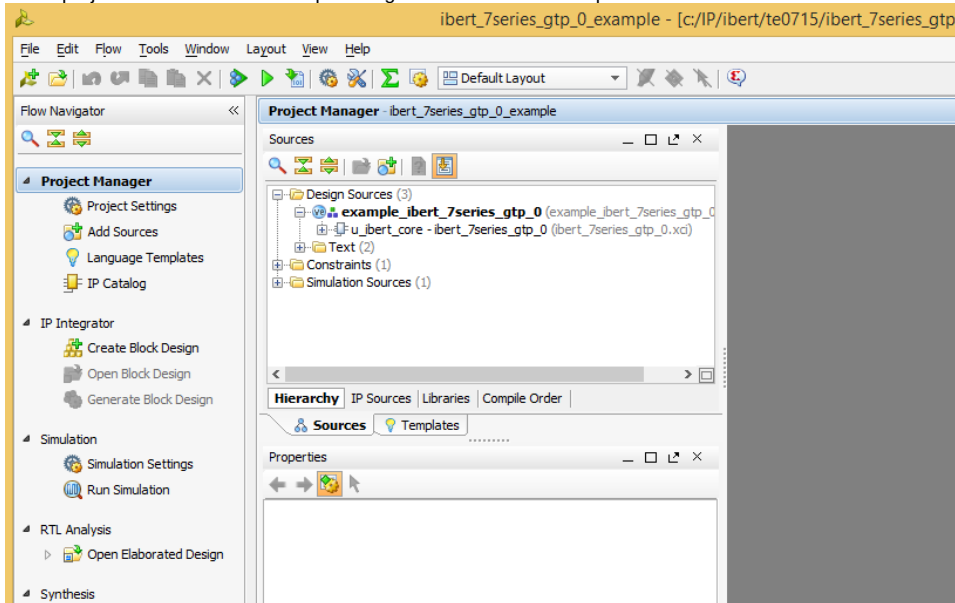
4. Generate the Core.



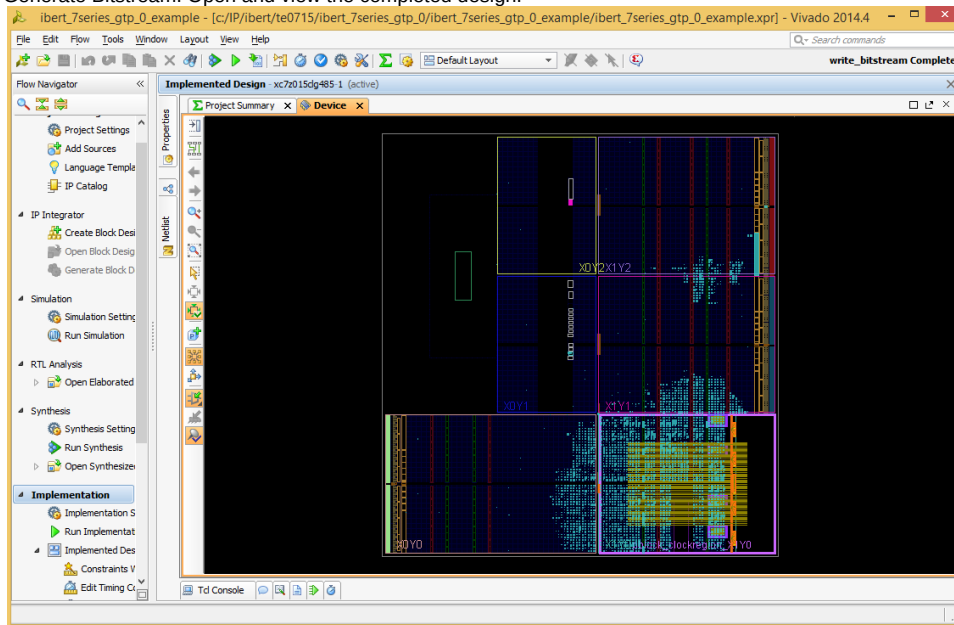
5. Right-click the IP in the Sources view, choose "Open IP Example Design".



6. A new project with the IBERT example design will be created and opened.



7. Generate Bitstream. Open and view the completed design.



8. Testing with Hardware

References

1. LogiCORE IP Integrated Bit Error Ratio Tester (IBERT) for 7 Series GTP Transceivers v3.0 ([pg133](#))
2. LogiCORE IP Integrated Bit Error Ratio Tester (IBERT) for 7 Series GTX Transceivers v3.0 ([pg132](#))