IBERT Test

The customizable IBERT core for 7 series FPGA can be used for evaluating and monitoring the GTs.

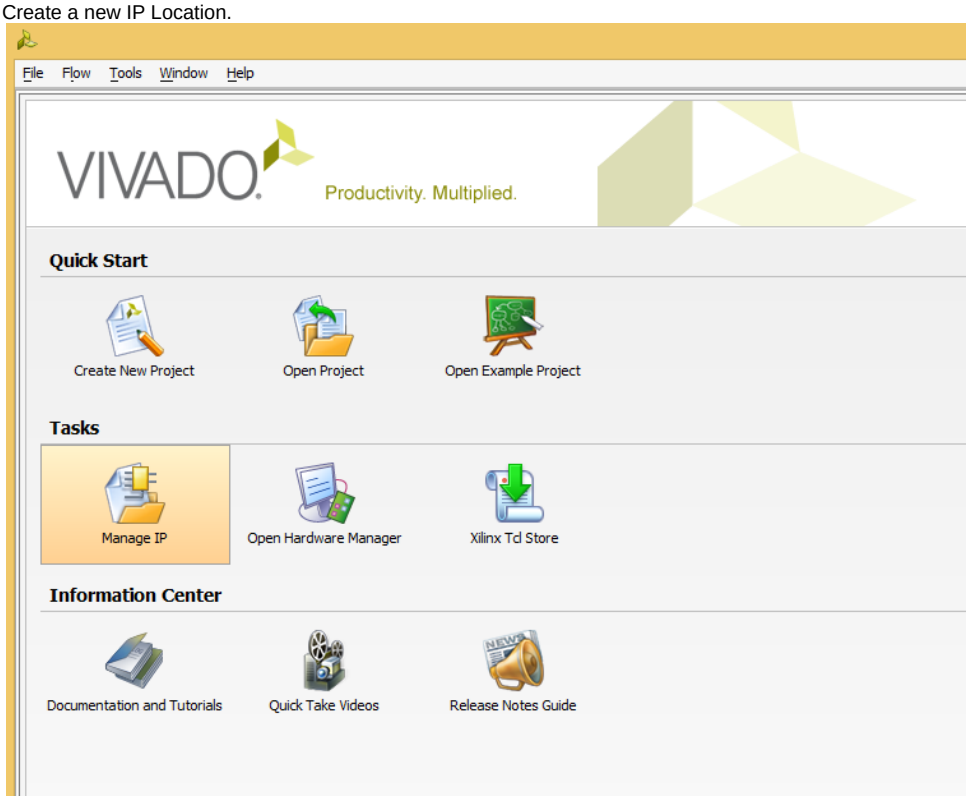
The IBERT core can be defined and generated using the Vivado built-in IP Cores. And with the generated example designs the IBERT Test can be implemented.

	Ref Clock Selection	GT Clock(MHz)	Notes
TE0712	MGTREFCLK0 216	125	
TE0715	MGTREFCLK1 112	125	
TE0741	MGTREFCLK1 116	125	Both Quads can use same refclock

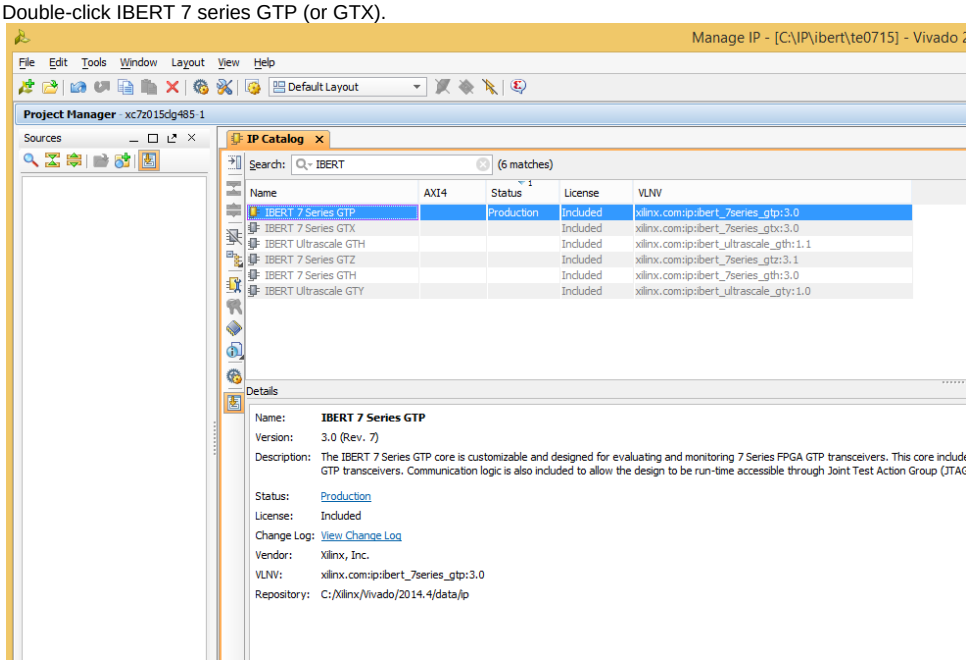
Ref clock selection to use on board fixed clock from Si5338.

Step to Step to generate the IBERT core:

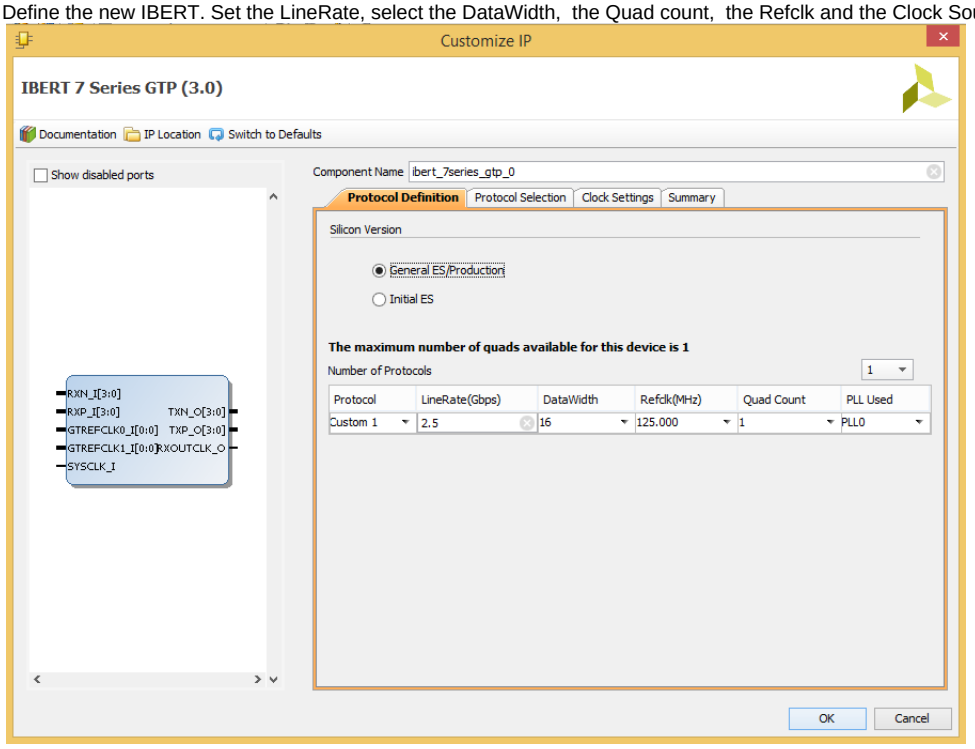
1. Create a new IP Location.

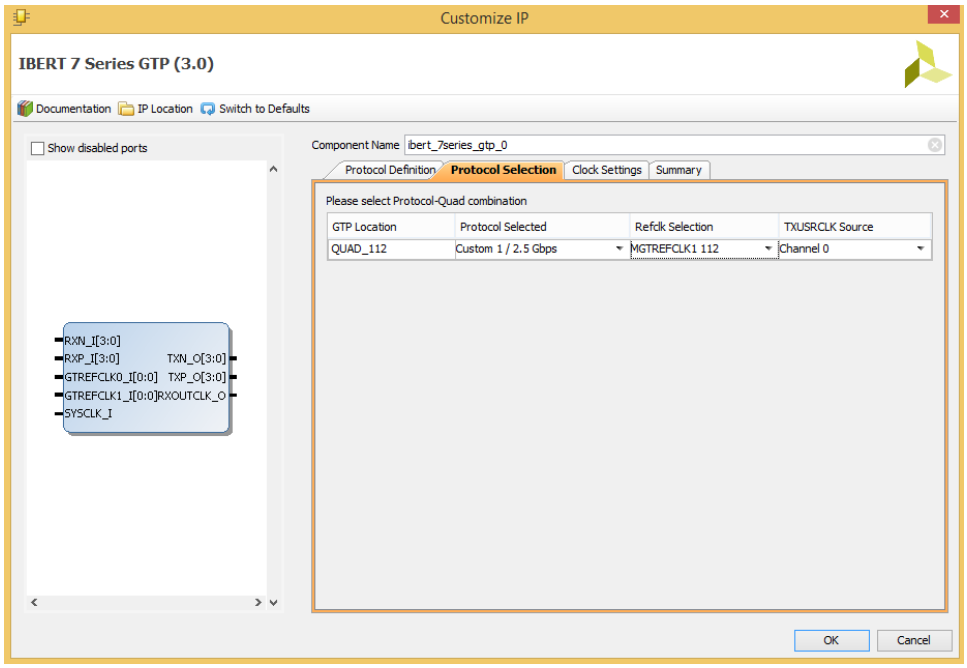


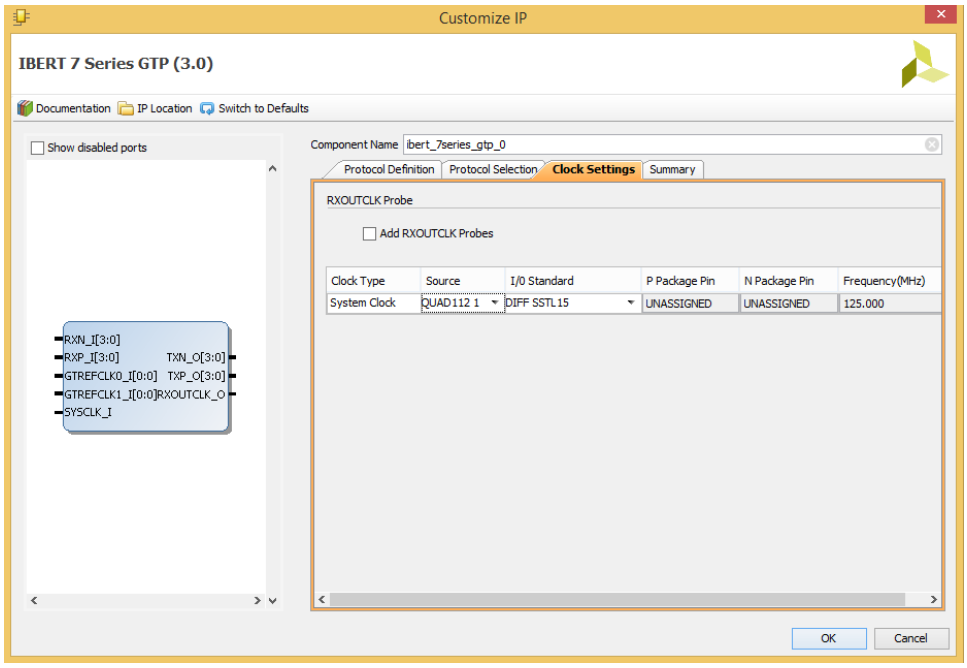
2. Double-click IBERT 7 series GTP (or GTX).



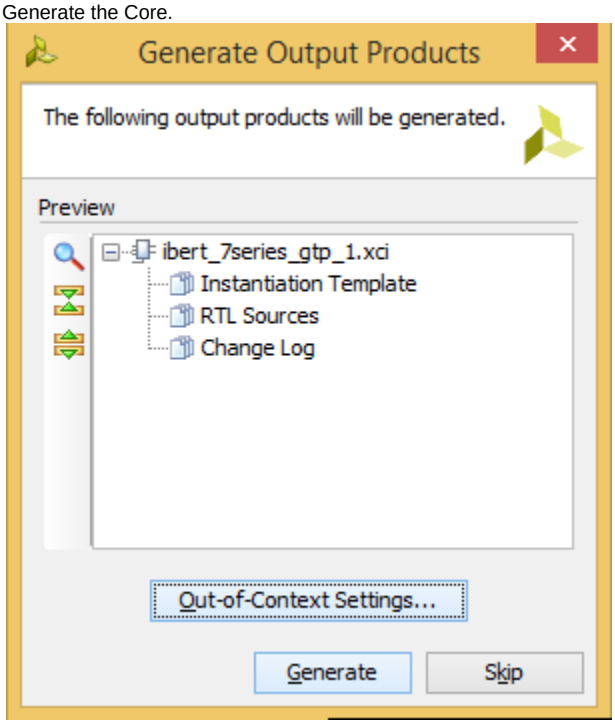
3. Define the new IBERT. Set the LineRate, select the DataWidth, the Quad count, the Refclk and the Clock Source.

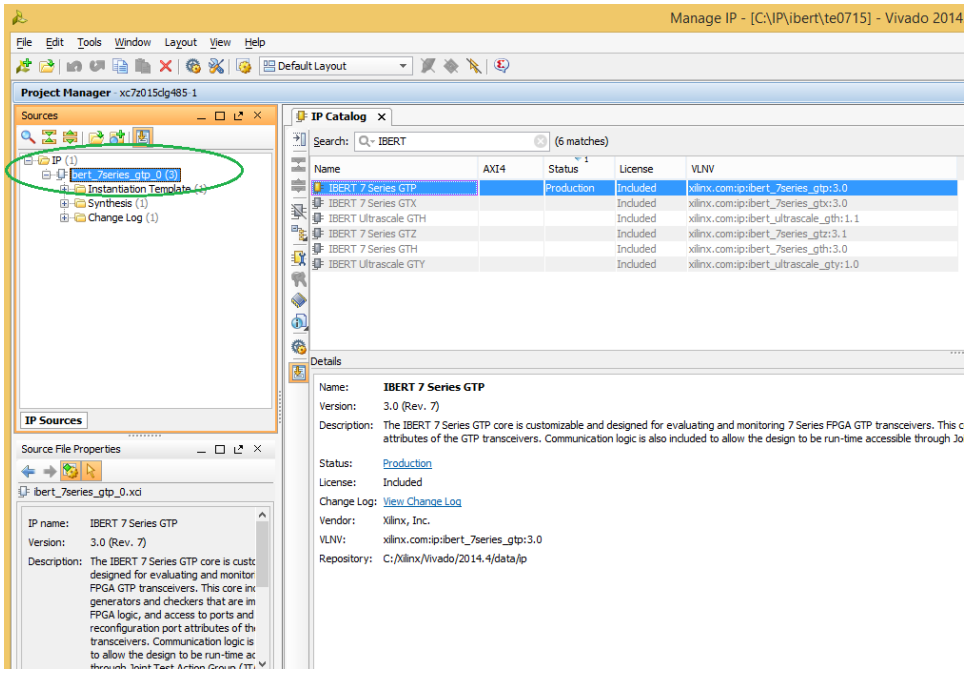



Customize IP
IBERT 7 Series GTP (3.0)
Documentation
IP Location
Switch to Defaults
Show disabled ports
RXN_I[3:0]
RXP_I[3:0]
GTREFCLK0_I[0:0]
GTREFCLK1_I[0:0]
SYSCLK_I
TXN_O[3:0]
TXP_O[3:0]
RXOUTCLK_O
Component Name
ibert_7series_gtp_0
Protocol Definition
Protocol Selection
Clock Settings
Summary
Please select Protocol-Quad combination
GTP Location
Protocol Selected
Refclk Selection
TXUSRCLK Source
QUAD_112
Custom 1 / 2.5 Gbps
MGTREFCLK1 112
Channel 0
OK
Cancel

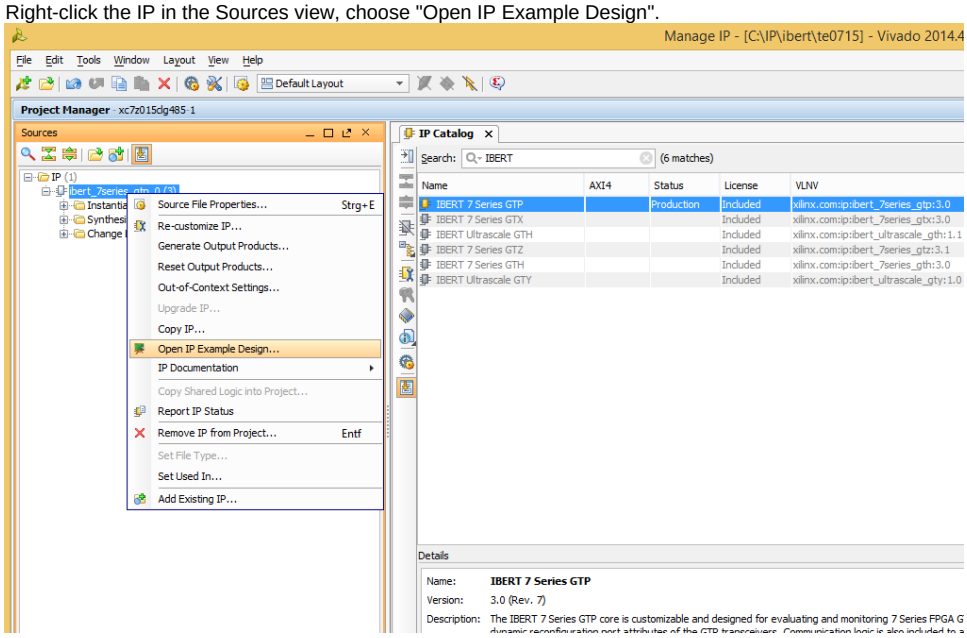

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GTREFCLK0_I[0:0]
GTREFCLK1_I[0:0]
SYSCLK_I
TXN_O[3:0]
TXP_O[3:0]
RXOUTCLK_O
Component Name
ibert_7series_gtp_0
Protocol Definition
Protocol Selection
Clock Settings
Summary
RXOUTCLK Probe
Add RXOUTCLK Probes
Clock Type
Source
I/O Standard
P Package Pin
N Package Pin
Frequency(MHz)
System Clock
QUAD112 1
DIFF SSTL15
UNASSIGNED
UNASSIGNED
125.000
OK
Cancel

4. Generate the Core.

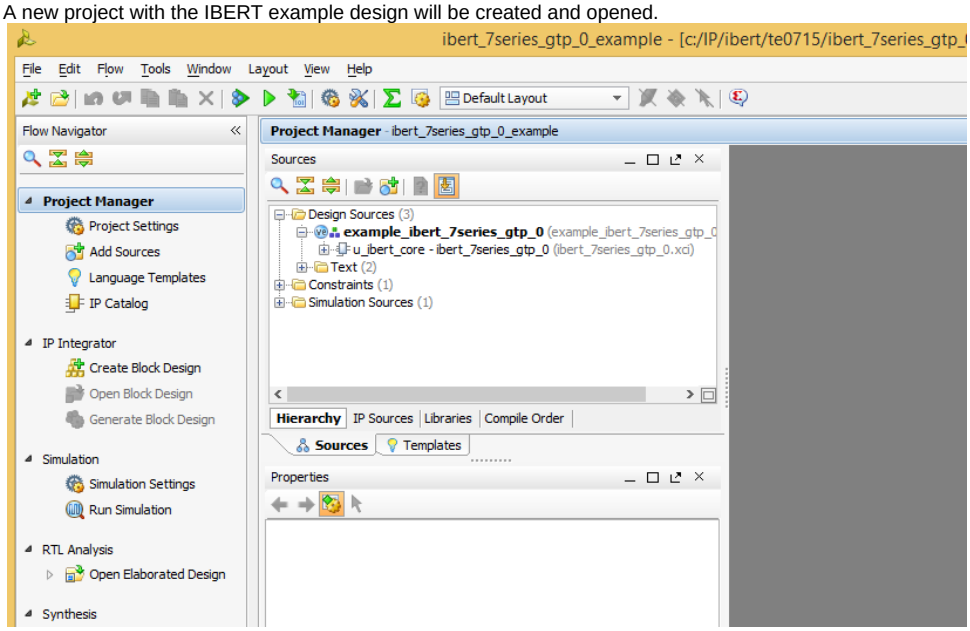




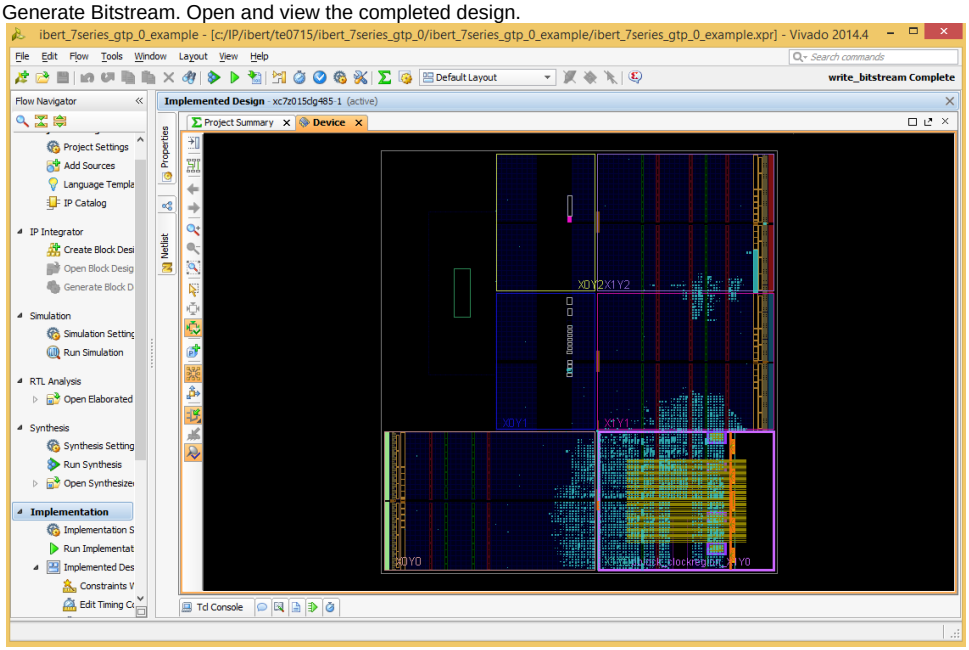
5. Right-click the IP in the Sources view, choose "Open IP Example Design".



6. A new project with the IBERT example design will be created and opened.



7. Generate Bitstream. Open and view the completed design.



8. Testing with Hardware

References

1. LogiCORE IP Integrated Bit Error Ratio Tester (IBERT) for 7 Series GTP Transceivers v3.0 (pg133)
2. LogiCORE IP Integrated Bit Error Ratio Tester (IBERT) for 7 Series GTX Transceivers v3.0 (pg132)