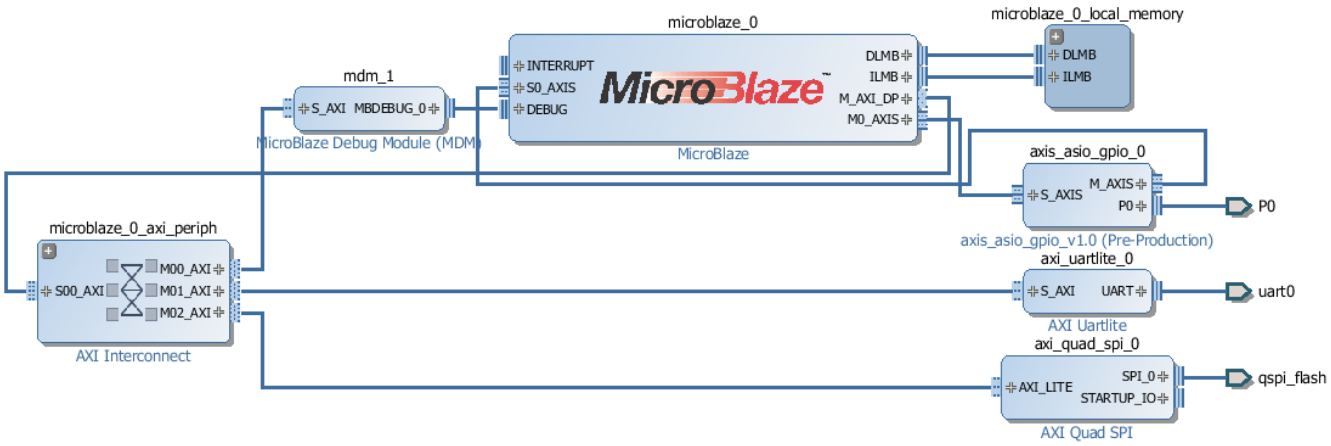
ASIO GPIO Demo

ASIO (A Simple IO) is re-implementation of ASIO IP Cores developed around 2004. ASIO GPIO Demos allocate all FPGA I/O pins that are not used for on-board components except single UART as ASIO I/O - bit addressable GPIO.



Example ASIO Demo for TE0711 SoM: a total of 196 I/O pins are connected to single ASIO GPIO IP Core. All ports are mapped to FPGA pins using Vivado board part flow, no manual constraints entered.