

# CR00140 TRM

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## Overview

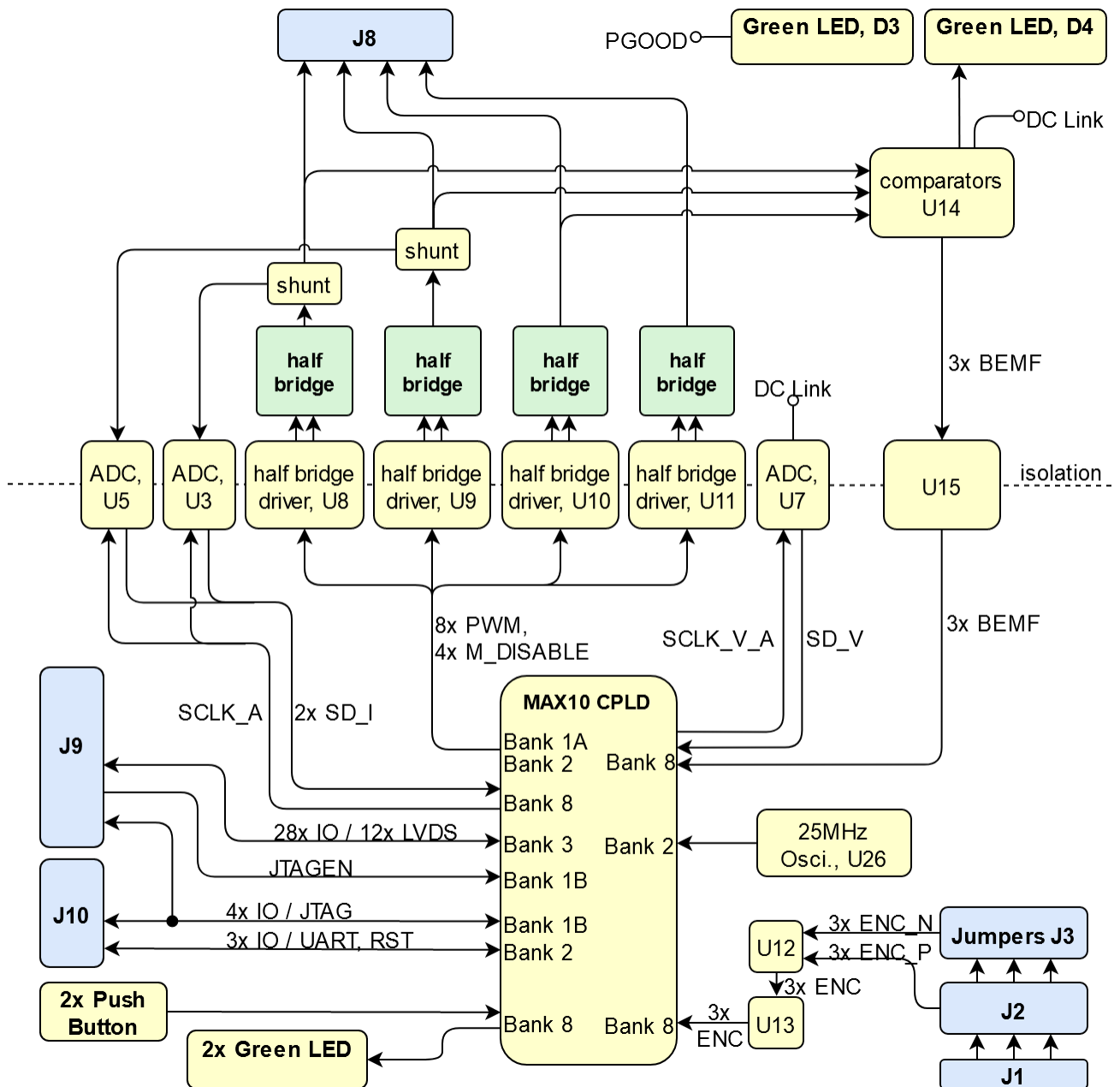
The Trenz Electronic CR00140-01 is a CRUVI motor driver module. It supports motors with up to 4 phases up to 40V.

Refer to <http://trenz.org/> for the current online version of this manual and other available documentation.

## Key Features

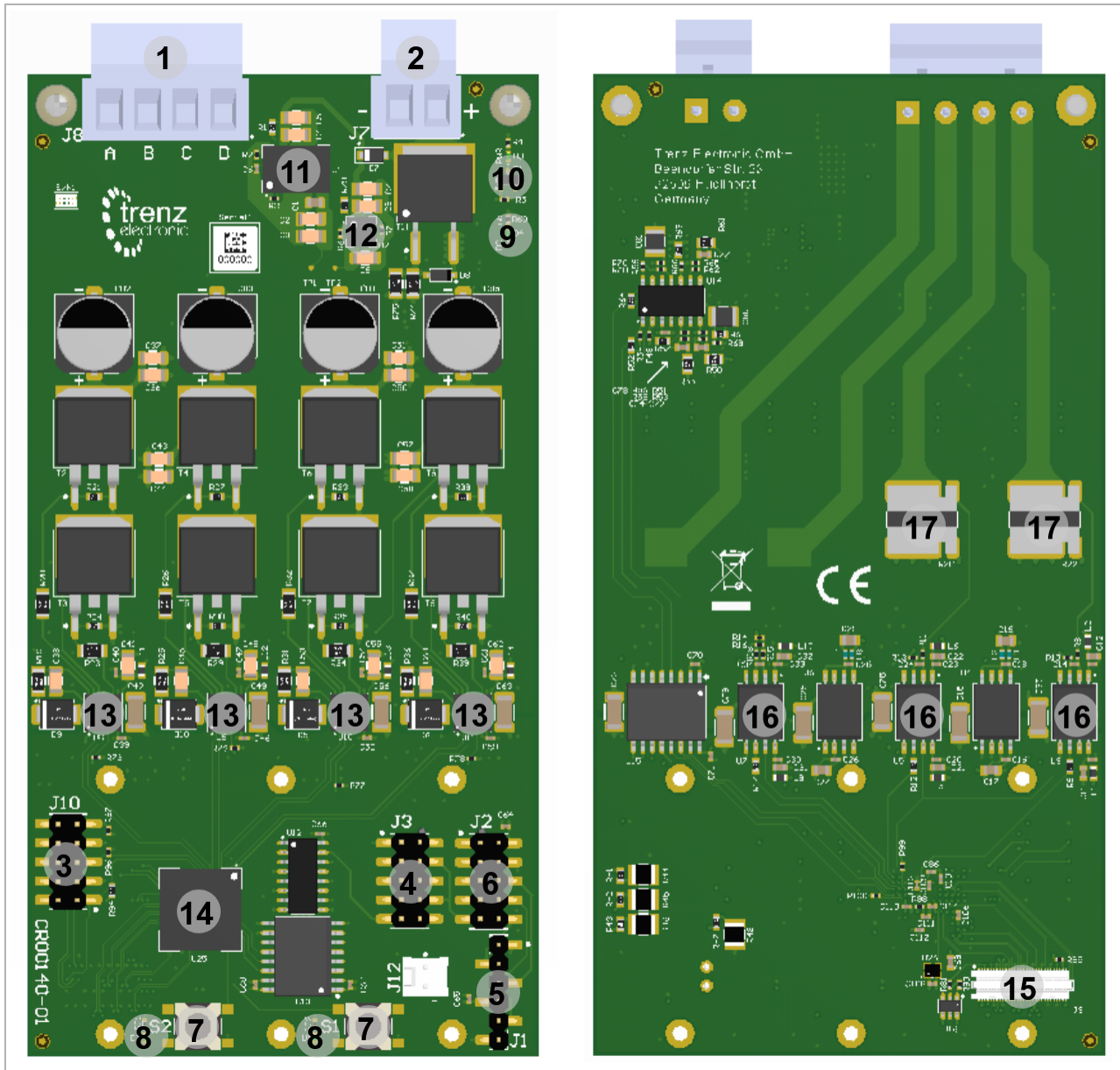
- **On Board**
  - MAX10 CPLD
  - 2 phase current measurement
  - DC\_LINK voltage measurement
  - 4x LEDs (2 power indicator, 2 user)
  - 2x Pushbutton
  - EEPROM
- **Interface**
  - 4 phase screw terminal motor connector
  - CRUVI for control
    - 1x high speed connector
  - 6x1 pin header for single ended sensors
  - 5x2 pin header for differential sensors
- **Power**
  - screw terminal for up to 40 V DC motor supply
- **Dimension**
  - 131 mm x 68.35 mm

## Block Diagram



CR00140 block diagram

## Main Components



#### CR00140 main components

1. Motor connector screw terminal, J8
2. Power supply screw terminal, J7
3. 5x2 pinheader, base for TEI0004 JTAG programmer, J10
4. 5x2 pinheader for sensor selection, J3
5. 6x1 pinheader for single ended sensors, J1
6. 5x2 pinheader for differential sensors, J2
7. User push buttons, S1, S2
8. User LEDs, D1, D2
9. LED DC\_Link, D4
10. LED Power Good, D3
11. DCDC for 15V, U1

12. DCDC for 5V, U2
13. half bridge drivers, U8, U9, U10, U11
14. MAX10 CPLD, U25
15. CRUVI high speed connector
16. ADCs, U3, U5, U7
17. Shunt resistors, R22, R28

## Initial Delivery State

Storage device name	Content	Notes
MAX10 CPLD	default firmware REV01	See firmware documentation

Initial delivery state of programmable devices on the module

## Signals, Interfaces and Pins

### Board to Board (B2B) I/Os

FPGA bank number and number of I/O signals connected to the B2B connector:

CPLD Bank	B2B Connector	I/O Signal Count	Voltage Level	Notes
3	J9	12 x LVDS / 24 I/Os	VADJ	6 x RX + 6 x TX
3	J9	4 I/Os	VADJ	
8	J9	4 I/Os	3.3V	Constant 3.3V
1B	J9	5 I/Os	3.3V	JTAG, JTAGEN, Constant 3.3V

General PL I/O to B2B connectors information

### JTAG Interface

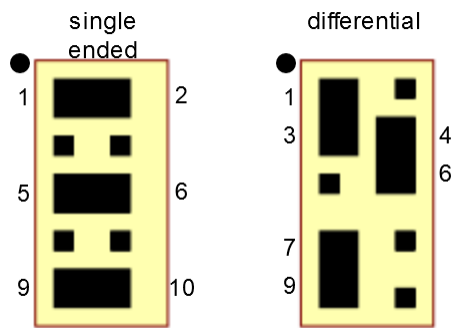
JTAG access to the CPLD of CR00140 is possible via the CRUVI high speed connector J9 and the pinheader J10, which is a base for TEI004 JTAG programmer. The JTAGEN signal is pulled up and available on J9 only. If JTAGEN is pulled low, the four signals can be used as user I/Os.

JTAG Signal	B2B Connector	Pin header	Notes
TMS	J9-55	J10-5	pull up
TDI	J9-51	J10-9	pull up
TDO	J9-53	J10-3	-
TCK	J9-59	J10-1	pull down
JTAGEN	J9-57	-	high for enable JTAG port of CPLD, low for user I/Os, pull up
UART_RX	-	J10-7	CPLD Firmware dependent, see <a href="#">Firmware</a>
UART_TX	-	J10-8	CPLD Firmware dependent, see <a href="#">Firmware</a>
RST	-	J10-6	CPLD Firmware dependent, see <a href="#">Firmware</a>
+3.3V_D	J9-4, J9-9	J10-4	-
DGND	several, see <a href="#">CRUVI</a>	J10-2, J10-10	-

JTAG pins connection

## Sensor Interface

The pin headers J1, J2 and J3 constitute the sensor interface. It can be e.g. used with Encoders or Hall sensors. J3 is the selector between differential sensor interface (J2) or single ended sensors (J1). Connecting sensors is only allowed to one of the two pinheaders (J1/J2), the other one has to stay unconnected. In the figure below the jumper configuration of J3 to enable one or the other type of sensor interface is depicted.



CR00140 Jumpers


The pinheaders for connection of the sensors are further described in the following table. For differential configuration 100 Ohm parallel termination is used.

Signal	J1 pin (singel ended)	J2 pin (differential)
ISO_ENC_A_P	3	6
ISO_ENC_A_N	-	5
ISO_ENC_B_P	5	8
ISO_ENC_B_N	-	7
ISO_ENC_I_P	2	10
ISO_ENC_I_N	-	9
DGND	4	3
+5.0V_D	1, 6	2

Sensor pins connection

## Motor Interface

CR00140 has a motor interface, where up to 4 phases can be driven.

 Check carefully correct connection of the phases of the motor, according to the motor and the implemented driving algorithm.

Signal	J8 pin lable	Note
Motor_A	A	Current measurement via R22 and ADC U3
Motor_B	B	Current measurement via R28 and ADC U5
Motor_C	C	-
Motor_D	D	-

Motor pins connection

CRUVI

For the connection to a control unit, the CRUVI interface is implemented. One high speed connector J9 is assembled. The connectors are further described in section [B2B Connectors](#). The connection of the signals and the voltage levels is described in the [CPLD](#) section.

Signal	Connector - Pin
DGND	J9-12, J9-18, J9-24, J9-30, J9-42, J9-48, J9-54, J9-13, J9-19, J9-25, J9-31, J9-37, J9-43, J9-49
+3.3V_D	J9-4, J9-9
+5.0V_D	J9-60
VADJ	J9-36
A0_P	J9-14
A0_N	J9-16
A1_P	J9-20
A1_N	J9-22
A2_P	J9-26
A2_N	J9-28
A3_P	J9-32
A3_N	J9-34
A4_P	J9-38
A4_N	J9-40
A5_P	J9-44
A5_N	J9-46
B0_P	J9-15
B0_N	J9-17
B1_P	J9-21
B1_N	J9-23
B2_P	J9-27
B2_N	J9-29
B3_P	J9-33
B3_N	J9-35
B4_P	J9-39
B4_N	J9-41
B5_P	J9-45
B5_N	J9-47
HSIO	J9-2

HSO	J9-6
RESET	J9-8
HSI	J9-10
TDI	J9-51
TDO	J9-53
TMS	J9-55
JTAGEN	J9-57
TCK	J9-59
SMB_ALERT	J9-3
SMB_SDA	J9-5
SMB_SCL	J9-7
REFCLK	J9-11

**CRUVI signals**

## On-board Peripherals

### CPLD

A Intel/Altera MAX10 FPGA 10M08SAU169C8G (U25) is used as system controller. Table below lists the SC CPLD I/O signals and pins.

Signal name	SC CPLD Pin	CPLD Bank	Connected to	Function	Notes
A0_P	J8	3	J9-14	CPLD firmware dependent	<a href="#">See CPLD Firmware</a>
A0_N	K8	3	J9-16	CPLD firmware dependent	<a href="#">See CPLD Firmware</a>
A1_P	M13	3	J9-20	CPLD firmware dependent	<a href="#">See CPLD Firmware</a>
A1_N	M12	3	J9-22	CPLD firmware dependent	<a href="#">See CPLD Firmware</a>
A2_P	M9	3	J9-26	CPLD firmware dependent	<a href="#">See CPLD Firmware</a>
A2_N	M8	3	J9-28	CPLD firmware dependent	<a href="#">See CPLD Firmware</a>
A3_P	N8	3	J9-32	CPLD firmware dependent	<a href="#">See CPLD Firmware</a>
A3_N	N7	3	J9-34	CPLD firmware dependent	<a href="#">See CPLD Firmware</a>
A4_P	M7	3	J9-38	CPLD firmware dependent	<a href="#">See CPLD Firmware</a>
A4_N	N6	3	J9-40	CPLD firmware dependent	<a href="#">See CPLD Firmware</a>
A5_P	K5	3	J9-44	CPLD firmware dependent	<a href="#">See CPLD Firmware</a>
A5_N	J5	3	J9-46	CPLD firmware dependent	<a href="#">See CPLD Firmware</a>
B0_P	N5	3	J9-15	CPLD firmware dependent	<a href="#">See CPLD Firmware</a>
B0_N	N4	3	J9-17	CPLD firmware dependent	<a href="#">See CPLD Firmware</a>
B1_P	J7	3	J9-21	CPLD firmware dependent	<a href="#">See CPLD Firmware</a>
B1_N	K7	3	J9-23	CPLD firmware dependent	<a href="#">See CPLD Firmware</a>
B2_P	L11	3	J9-27	CPLD firmware dependent	<a href="#">See CPLD Firmware</a>

B2_N	M11	3	J9-29	CPLD firmware dependent	<a href="#">See CPLD Firmware</a>
B3_P	L10	3	J9-33	CPLD firmware dependent	<a href="#">See CPLD Firmware</a>
B3_N	M10	3	J9-35	CPLD firmware dependent	<a href="#">See CPLD Firmware</a>
B4_P	J6	3	J9-398	CPLD firmware dependent	<a href="#">See CPLD Firmware</a>
B4_N	K6	3	J9-41	CPLD firmware dependent	<a href="#">See CPLD Firmware</a>
B5_P	L5	3	J9-45	CPLD firmware dependent	<a href="#">See CPLD Firmware</a>
B5_N	L4	3	J9-47	CPLD firmware dependent	<a href="#">See CPLD Firmware</a>
HSIO	N9	3	J9-2	CPLD firmware dependent	<a href="#">See CPLD Firmware</a>
HSO	N10	3	J9-6	CPLD firmware dependent	<a href="#">See CPLD Firmware</a>
RESET	M5	3	J9-8	CPLD firmware dependent	<a href="#">See CPLD Firmware</a>
HSI	N12	3	J9-10	CPLD firmware dependent	<a href="#">See CPLD Firmware</a>
TDI	F5	1B	J9-51, J10-9	JTAG / user IO CPLD firmware dependent	<a href="#">See CPLD Firmware</a>
TDO	F6	1B	J9-53, J10-3	JTAG / user IO CPLD firmware dependent	<a href="#">See CPLD Firmware</a>
TMS	G1	1B	J9-55, J10-5	JTAG / user IO CPLD firmware dependent	<a href="#">See CPLD Firmware</a>
JTAGEN	E5	1B	J9-57	JTAG enable CPLD firmware dependent	<a href="#">See CPLD Firmware</a>
TCK	G2	1B	J9-59, J10-1	JTAG / user IO CPLD firmware dependent	<a href="#">See CPLD Firmware</a>
SMB_ALERT	K2	2	J9-3	CPLD firmware dependent	<a href="#">See CPLD Firmware</a>
SMB_SDA	H5	2	J9-5	CPLD firmware dependent	<a href="#">See CPLD Firmware</a>
SMB_SCL	H4	2	J9-7	CPLD firmware dependent	<a href="#">See CPLD Firmware</a>
REFCLK	M2	2	J9-11	CPLD firmware dependent	<a href="#">See CPLD Firmware</a>
BUTTON1	C10	8	S2	CPLD firmware dependent	activ low, <a href="#">See CPLD Firmware</a>
BUTTON2	B10	8	S1	CPLD firmware dependent	activ low, <a href="#">See CPLD Firmware</a>
ENC_A	A10	8	U13-13	Sensor input channel A	-
ENC_B	A9	8	U13-12	Sensor input channel B	-
ENC_I	A11	8	U13-14	Sensor input channel I	-
LED0	D6	8	D2	CPLD firmware dependent	<a href="#">See CPLD Firmware</a>
LED1	B2	8	D1	CPLD firmware dependent	<a href="#">See CPLD Firmware</a>
M_BEMF_B_D	B5	8	U15-13	Back EMF signal phase B	-
M_BEMF_C_D	A5	8	U15-12	Back EMF signal phase C	-
M_BEMF_A_D	A4	8	U15-14	Back EMF signal phase A	-
M_PWM_AH	F1	1A	U8-2	Phase A half bridge high (DC_LINK) side driver signal	-
M_PWM_AL	E3	1A	U8-3	Phase A half bridge low (PGND) side driver signal	-
M_PWM_BH	E1	1A	U9-2	Phase B half bridge high (DC_LINK)side driver signal	-
M_PWM_BL	D1	1A	U9-3	Phase B half bridge low (PGND) side driver signal	-
M_PWM_CH	E4	1A	U10-2	Phase C half bridge high (DC_LINK)side driver signal	-
M_PWM_CL	C1	1A	U10-3	Phase C half bridge low (PGND) side driver signal	-
M_PWM_DH	C2	1A	U11-2	Phase D half bridge high (DC_LINK) side driver signal	-
M_PWM_DL	B1	1A	U11-3	Phase D half bridge low (PGND) side driver signal	-
SD_IA	E6	8	U3-6	Current measurement phase A	33 Ohm series Resistor
SCLK_A	B3	8	U3-7, U5-7	Clock for ADC for current measurement phase A and B	(5-20 MHz)

SD_V	B4	8	U7-6	Voltage measurement DC_LINK	33 Ohm series Resistor
SD_IB	A2	8	U5-6	Current measurement phase B	33 Ohm series Resistor
SCLK_V_A	A3	8	U7-7	Clock for ADC for voltage measurement DC_LINK	(5-20 MHz)
M_DISABLE_D_D	J1	2	U11-5	Halfe bridge disable phase D	disabled when high, pull up connected
M_DISABLE_A_D	M1	2	U8-5	Halfe bridge disable phase A	disabled when high, pull up connected
M_DISABLE_B_D	L2	2	U9-5	Halfe bridge disable phase B	disabled when high, pull up connected
M_DISABLE_C_D	K1	2	U10-5	Halfe bridge disable phase C	disabled when high, pull up connected
REFCLK	M2	2	J9-11	CPLD firmware dependent	-
RST	M3	2	J10-6	CPLD firmware dependent	-
UART_RX	N2	2	J10-7	CPLD firmware dependent	-
UART_TX	N3	2	J10-8	CPLD firmware dependent	-
CLK_25MHZ	H6	2	U26-3	Clock input for accurate 25 Mhz clk.	-

#### On-board LEDs

## CPLD Bank Voltages

Bank	Schematic Name	Voltage	Notes
1A	+3.3V_D	3.3V	Provided via CRUVI
1B	+3.3V_D	3.3V	Provided via CRUVI
2	+3.3V_D	3.3V	Provided via CRUVI
3	VADJ	1.8V, 2.5V, 3.3 V	Provided via CRUVI, supported voltage levels are determined by the CPLD Firmware, and the connected base /controller.
8	+3.3V_D	3.3V	Provided via CRUVI

#### CPLD bank voltages.

## LEDs

Designator	Color	Connected to	Signal name	Active Level	Note
D1	green	U25-B2	LED1	high	User LED, CPLD Firmware dependent, see <a href="#">Firmware</a> description.
D2	green	U25-D6	LED0	high	User LED, CPLD Firmware dependent, see <a href="#">Firmware</a> description.
D3	green	U1-A3, U2-B1	PGOOD	high	ON when +15.0V_M and +5.0V_M regulator indicated power good. Connected via transistor T1.
D4	green	DC_LINK	-	low	ON when DC_LINK above 11.7V. Connected via comparator U14D to DC_LINK

#### On-board LEDs

## Buttons

Designator	Connected to	Signal name	Active Level	Note
S1	U25-B10	BUTTON2	low	User button, CPLD Firmware dependent, see <a href="#">Firmware</a> description.

S2	U25-C10	BUTTON1	low	User button, CPLD Firmware dependent, see <a href="#">Firmware</a> description.
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#### On-board LEDs

## ADCs

There are three isolating AD7403-8 ADCs for continuous measurement of phase A current (U3), phase B current (U5) and the DC\_LINK voltage (U7) on board. The currents are measured through the shunt resistors R22, R28 for phase A and B respectively. The ADC clock is routed to the CPLD. For Currents the clock has the signal label SCLK\_A and for the voltage SCLK\_V\_A. The data signals are also routed to the CPLD. See CPLD [Firmware](#) for further description.

## BEMF

Back EMF zero crossing signals for sensor-less motor control are implemented for Phase A, B and C. They are routed via a triple channel Digital isolator (U15) to the CPLD. See CPLD [Firmware](#) for further description.

## Half bridge drivers

Four ADuM7223 isolated half bridge drivers (U8, U9, U10, U11) are used for driving the four phases.

## DCDCs

On the Motor side are two DCDCs on board. LTM8053 (U1) is utilized for the generation of the 15V transistor control voltage from VIN and can be measured on Testpoint TP1. A LTM8074 DCDC (U2) generates 5V from VIN for miscellaneous signals on the motor side of the PCB and can be measured on TP2.

Two isolated DCDCs ADUM5028 (U4, U6) are used for the generation two separate clean 5V for the supply of the current measurement ADCs U3 and U5.

## Power and Power-On Sequence

### EEPROM

The 2K Microchip 24AA02E48 EEPROM with pre-programmed unique 48bit address is connected to the CRUVI HS (Signals: SMB\_SDA, SMB\_SCL) connector and can e.g. be used for identification purposes.

## Power Supply

The motor driving stage is supplied via connector J7 with maximum of 40V DC. Polarity of the powersupply is noted on the PCB.



Check powersupply for correct polarity. Inversion of polarity will damage the module. At least Transistor T11 may be harmed. Furthermore make sure that under any circumstances the absolute maximum voltage does not exceed 42V.

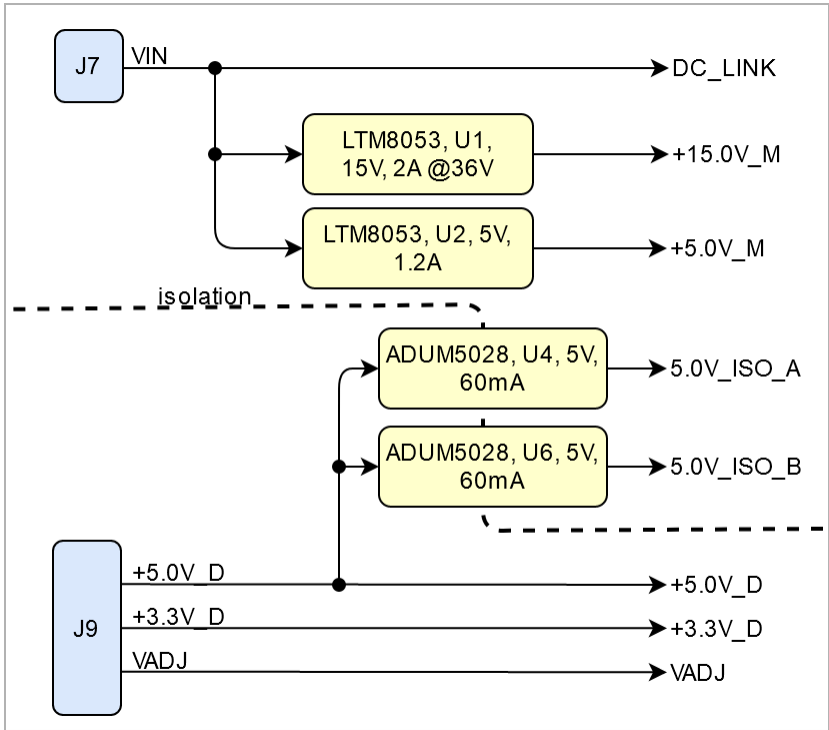
## Power Consumption

The power consumption on the motor stage side (J7) is dominated by the connected motor and the corresponding driving algorithm. The idle consumption is given below.

Power Input Pin	Typical Current	Note
VIN	~ 47mA	@24V (J7), no motor connected, no PWM signal driven.

#### Power Consumption

## Power Distribution Dependencies



Power Distribution

## Power-On Sequence

There is no power on sequence which has to be maintained.

## Power Rails

Power Rail Name	B2B Connectors	Direction	Notes
+3.3V_D	J9-4, J9-9	In	-
+5.0V_D	J9-60	In	-
VADJ	J9-36	In	-
VIN	J7	In	isolated

Module power rails.

## Board to Board Connectors

CRUVI modules use on bottom side:

- TMMH-106-04-F-DV-A-M as Low Speed connectors, (12 pins, 6 per row)
- ST4-30-1.50-L-D as High Speed connectors, (60 pins, 30 per row)

CRUVI carrier use on top side:

- CLT-106-02-F-D-A-K as Low Speed connectors , (12 pins, 6 per row)
- SS4-30-3.50-L-D as High Speed connectors, (60 pins, 30 per row)

Connector Mating height

Mating height of the high speed connectors is 5mm. The low speed connectors mate correctly within a range from 4.78 mm to 5.29 mm.

Current Rating

Current rating of High Speed B2B connectors is 1.6A per pin (2 pins powered).

Current rating of Low Speed B2B connectors is 4.1A per pin (2 pins powered).

Speed Rating

There is no data available for the connectors actual used here. Data available for other stacking heights of same connectors is summarized in the following table:

Connector	Speed ratings
ST4/SS4 single ended (4mm stacking height!)	13.5GHz / 27 Gbps
ST4/SS4 differential (4mm stacking height!)	15.5 GHz / 31 Gbps
TMMH/CLT single ended (4.77mm stacking height!)	5.5GHz / 11 Gbps

Connector speed ratings

Operating Temp Range

All connectors are specified for a temp. range of -55 °C to 125 °C.

Technical Specifications

Absolute Maximum Ratings

Symbols	Description	Min	Max	Unit
VIN	Motor supply voltage	0	42	V
+3.3V_D	digital part 3.3V supply voltage	-0.3	3.9	V
+5.0V_D	digital part 5V supply voltage	-0.3	6.0	V
VADJ	IO Bank Voltage	-0.3	3.9	V

PS absolute maximum ratings

Recommended Operating Conditions

Operating temperature range depends also on customer design and cooling solution. Please contact us for options.

Parameter	Min	Max	Units	Reference Document
VIN	22	40	V	LTM8053 datasheet
+3.3V_D	3.135	3.465	V	MAX10 datasheet

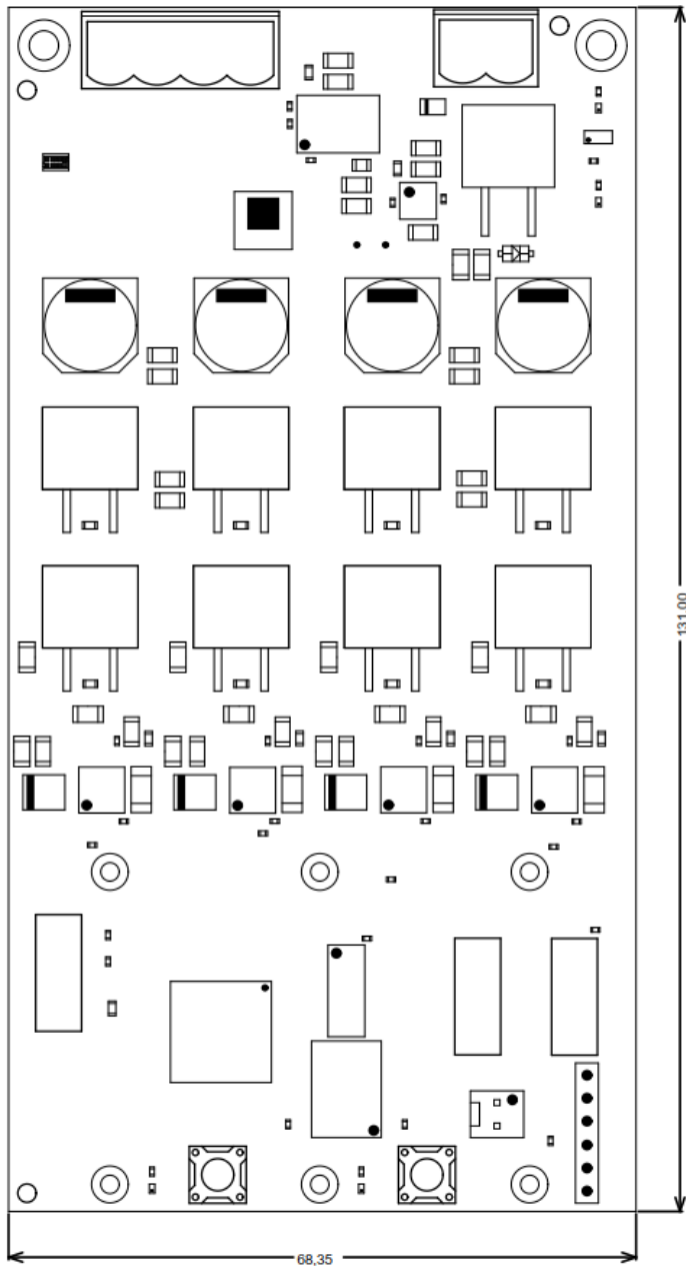
+5.0V_D	4.75	5.25	V	SN65LBC173AD datasheet
VADJ (3.3V operation)	3.135	3.465	V	MAX10 datasheet
VADJ (2.5V operation)	2.375	2.625		
VADJ (1.8V operation)	1.71	1.89		
T	-40	105	°C	AD7403-8 (junction)
T (ambient)	-40	85	°C	SN65LBC173AD datasheet

**Recommended operating conditions.**

## Physical Dimensions

- Module size: 68.35 mm × 131 mm. Please download the assembly diagram for exact numbers.
- Mating height with standard connectors: 5 mm.

PCB thickness: 1.6 mm.



Physical Dimension

# Currently Offered Variants

Trenz shop CR00140 overview page	
<a href="#">English page</a>	<a href="#">German page</a>

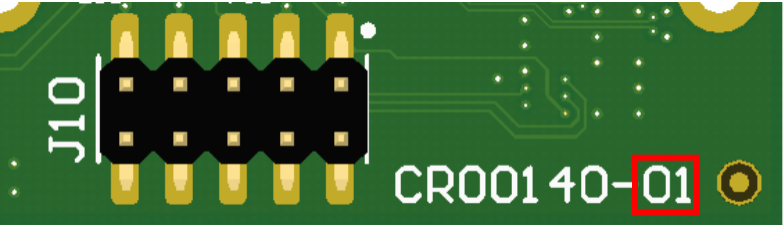
# Revision History

## Hardware Revision History

Date	Revision	Changes	Documentation Link
2019-12-20	01	Prototypes	-
2020-03-10	02	removed LS connector J11, added EEPROM U16	-

### Hardware Revision History

Hardware revision number can be found on the PCB board together with the module model number separated by the dash.



Board hardware revision number.

## Document Change History

Date	Revision	Contributor	Description
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Document change history.

Disclaimer

Data Privacy

Please also note our data protection declaration at <https://www.trenz-electronic.de/en/Data-protection-Privacy>

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## Environmental Protection

To confront directly with the responsibility toward the environment, the global community and eventually also oneself. Such a resolution should be integral part not only of everybody's life. Also enterprises shall be conscious of their social responsibility and contribute to the preservation of our common living space. That is why Trenz Electronic invests in the protection of our Environment.

## REACH, RoHS and WEEE

### REACH

Trenz Electronic is a manufacturer and a distributor of electronic products. It is therefore a so called downstream user in the sense of [REACH](#). The products we supply to you are solely non-chemical products (goods). Moreover and under normal and reasonably foreseeable circumstances of application, the goods supplied to you shall not release any substance. For that, Trenz Electronic is obliged to neither register nor to provide safety data sheet. According to present knowledge and to best of our knowledge, no [SVHC \(Substances of Very High Concern\) on the Candidate List](#) are contained in our products. Furthermore, we will immediately and unsolicited inform our customers in compliance with REACH - Article 33 if any substance present in our goods (above a concentration of 0,1 % weight by weight) will be classified as SVHC by the [European Chemicals Agency \(ECHA\)](#).

### RoHS

Trenz Electronic GmbH herewith declares that all its products are developed, manufactured and distributed RoHS compliant.

### WEEE

Information for users within the European Union in accordance with Directive 2002/96/EC of the European Parliament and of the Council of 27 January 2003 on waste electrical and electronic equipment (WEEE).

Users of electrical and electronic equipment in private households are required not to dispose of waste electrical and electronic equipment as unsorted municipal waste and to collect such waste electrical and electronic equipment separately. By the 13 August 2005, Member States shall have ensured that systems are set up allowing final holders and distributors to return waste electrical and electronic equipment at least free of charge. Member States shall ensure the availability and accessibility of the necessary collection facilities. Separate collection is the precondition to ensure specific treatment and recycling of waste electrical and electronic equipment and is necessary to achieve the chosen level of protection of human health and the environment in the European Union. Consumers have to actively contribute to the success of such collection and the return of waste electrical and electronic equipment. Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.

Trenz Electronic is registered under WEEE-Reg.-Nr. DE97922676.

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