

TE0823 CPLD

Table of contents

- 1 [Table of contents](#)
- 2 [Overview](#)
 - 2.1 [Feature Summary](#)
 - 2.2 [Firmware Revision and supported PCB Revision](#)
- 3 [Product Specification](#)
 - 3.1 [Port Description](#)
 - 3.2 [Functional Description](#)
 - 3.2.1 [JTAG](#)
 - 3.2.2 [Boot Mode](#)
 - 3.2.3 [Power](#)
- 4 [Appx. A: Change History](#)
 - 4.1 [Revision Changes](#)
 - 4.2 [Document Change History](#)
- 5 [Appx. B: Legal Notices](#)
 - 5.1 [Data Privacy](#)
 - 5.2 [Document Warranty](#)
 - 5.3 [Limitation of Liability](#)
 - 5.4 [Copyright Notice](#)
 - 5.5 [Technology Licenses](#)
 - 5.6 [Environmental Protection](#)
 - 5.7 [REACH, RoHS and WEEE](#)

Overview

CPLD Device with designator U21: LCMX02-256HC

Feature Summary

- JTAG routing
- Boot Mode settings
- Power Managment

Firmware Revision and supported PCB Revision

See Document Change History

Product Specification

Port Description

Name / opt. VHD Name	Direction	Pin	Bank Power	Description
C_TCK	in	30	3.3VIN	JTAG B2B
C_TDI	in	32	3.3VIN	JTAG B2B
C_TDO	out	1	3.3VIN	JTAG B2B

C_TMS	in	29	3.3VIN	JTAG B2B
PG_FPD	in	27	3.3VIN	Power GOOD from SOC FPD regulators
RESIN	inout	4	3.3VIN	Reset control and minitoring
EN_MGT	out	5	3.3VIN	enable GTR Power Domain
JTAGEN	in	26	3.3VIN	Enable JTAG access to CPLD for Firmware update (zero: JTAG routed to module, one: CPLD access)
MODE	in	25	3.3VIN	Boot Mode for Zynq/ZynqMP Devices (Flash or SD)
MODE0	out	12	1.8V	ZynqMP Boot Mode Pin 0
MODE1	out	13	1.8V	ZynqMP Boot Mode Pin 1
MODE2	out	14	1.8V	ZynqMP Boot Mode Pin 2
MODE3	out	16	1.8V	ZynqMP Boot Mode Pin 3
NOSEQ	inout	23	3.3VIN	usage CPLD Variant depends
PGOOD	inout	28	3.3VIN	Module Power Good (FPD + MGT(if not disabled by user))
PG_MGT	in	17	1.8V	Power Good of GTR power domain
TCK	out	9	1.8V	JTAG ZynqMP
TDI	out	8	1.8V	JTAG ZynqMP
TDO	in	10	1.8V	JTAG ZynqMP
TMS	out	11	1.8V	JTAG ZynqMP
X0	in	20	VCCO_65	X0 X1 can be used to disable MGT Power
X1	in	21	VCCO_65	X0 X1 can be used to disable MGT Power

Functional Description

JTAG

JTAG signals routed directly through the CPLD to FPGA. Access between CPLD and FPGA can be multiplexed via JTAGEN (logical one for CPLD, logical zero for FPGA) on JM1-89.

Boot Mode

Boot Modes can be selected via B2B Pin Mode. Trenz Electronic provides currently 4 Firmware variants, one for SD/JTAG, one for JTAG/QSPI, one for SD /QSPI and SD/QSPI/JTAG usage.

Mode	JTAG/QSPI-Variant	SD/JTAG-Variant	SD/QSPI (default Firmware)	SD/QSPI/JTAG
low	JTAG	Boot from SD	Boot from SD	JTAG Mode, if NOSEQ* is high otherwise boot from SD
high	Boot from Flash	JTAG	Boot from Flash	JTAG Mode, if NOSEQ* is high otherwise boot from Flash

For other UltraScale+ Boot Modes options custom firmware is needed, see also Table 11.1 Boot Modes from Xilinx UG1085.



A special FSBL is provided on 2017.4 or newer reference designs to write boot image to QSPI with Xilinx tools (Vivado or SDK) on Boot Mode unequal JTAG .



NOSEQ*: Please check the carrier board documentation, before using the SD/QSPI/JTAG firmware variant on TE0823. In the most cases special carrier CPLD firmware is needed.

Power

PGOOD is zero if PG_FPD is low or if PG_MGT is low (as long as it is enabled by user) otherwise it's high impedance

Appx. A: Change History

Revision Changes

- REV01
 - initial release

Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

Date	Document Revision	CPLD Firmware Revision	Supported PCB Revision	Authors	Description
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Appx. B: Legal Notices

Data Privacy

Please also note our data protection declaration at <https://www.trenz-electronic.de/en/Data-protection-Privacy>

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Ambiguous method overloading for method `jdk.proxy279.$Proxy4022#hasContentLevelPermission`. Cannot resolve which method to invoke for `[null, class java.lang.String, class com.atlassian.confluence.pages.Page]` due to overlapping prototypes between: `[interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]` `[interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]`