Vivado Labtools

Vivado Labtools include programming and debug for all FPGA and SoC devices. Labtools do not need license and support all Xilinx devices.

> ⚠ Pre-built images for labtools use may have I/O pullups defined on all FPGA I/O Pins, make sure that this is OK for your base board and attached peripherals! Please check the README.TXT in the distribution archive.

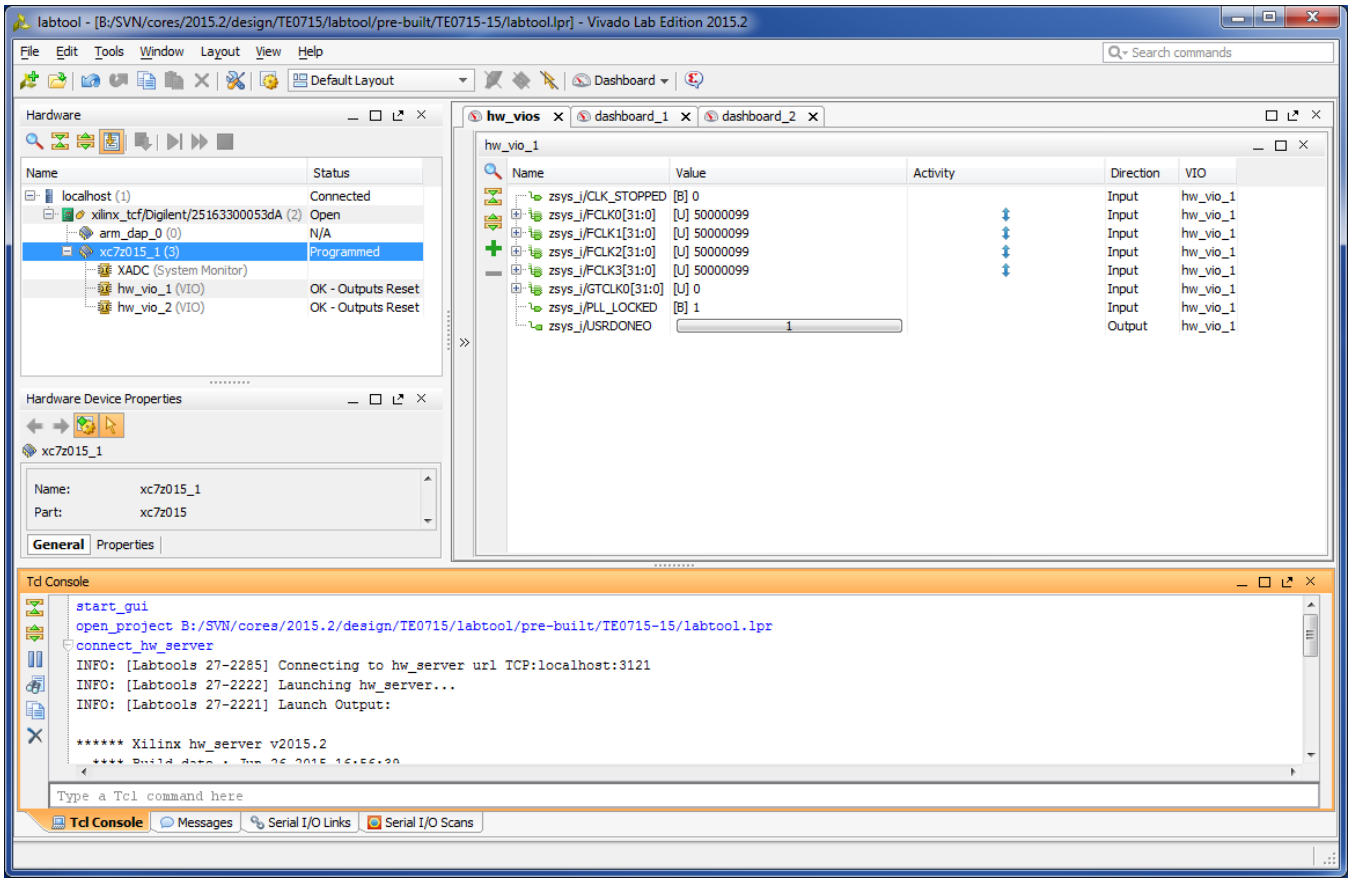
Using Labtools

Labtools can be used if pre-built images for FPGA are available, for debugging also the debug netlist file is needed.

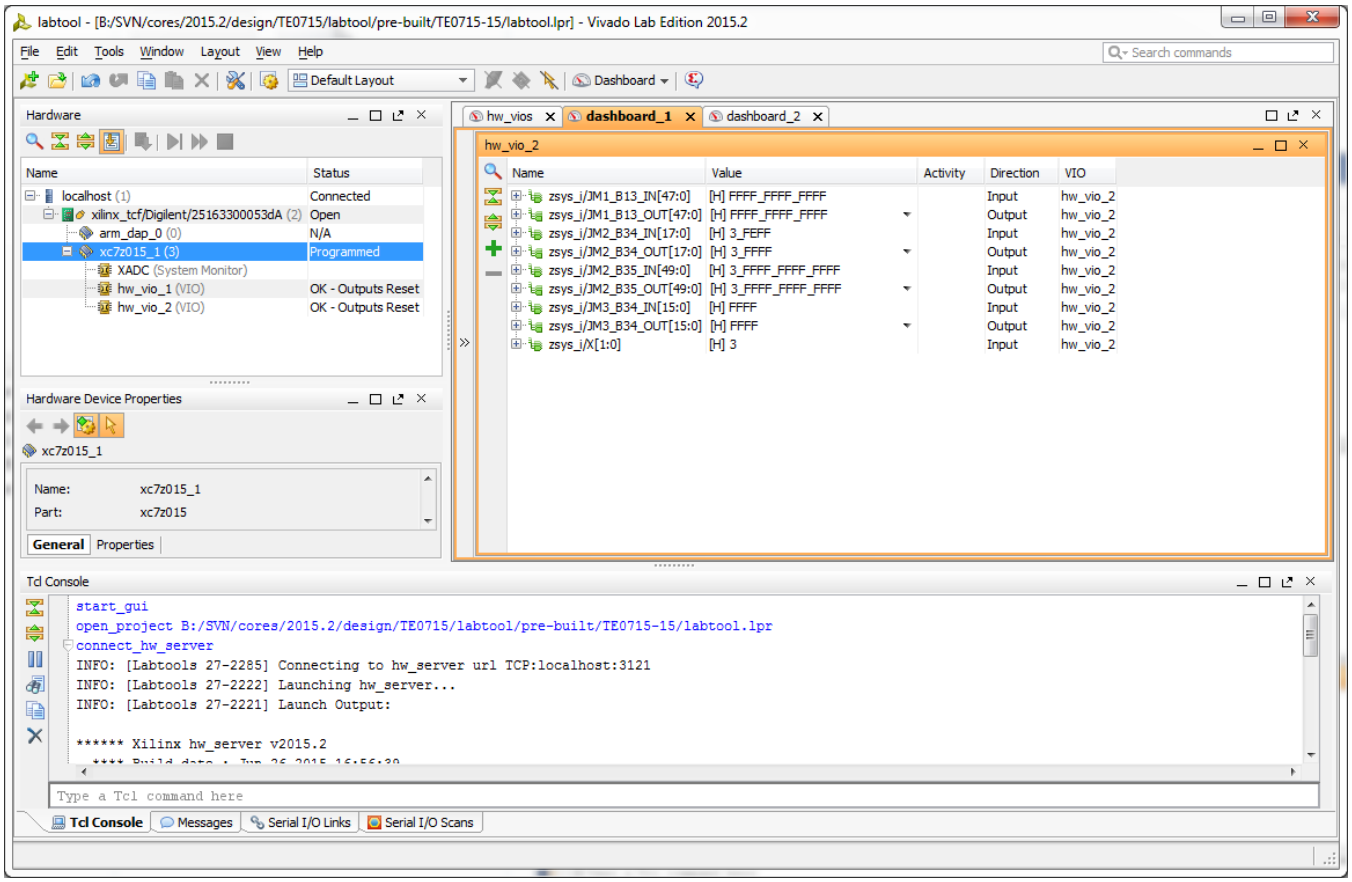
Example Debug Session

TE0715

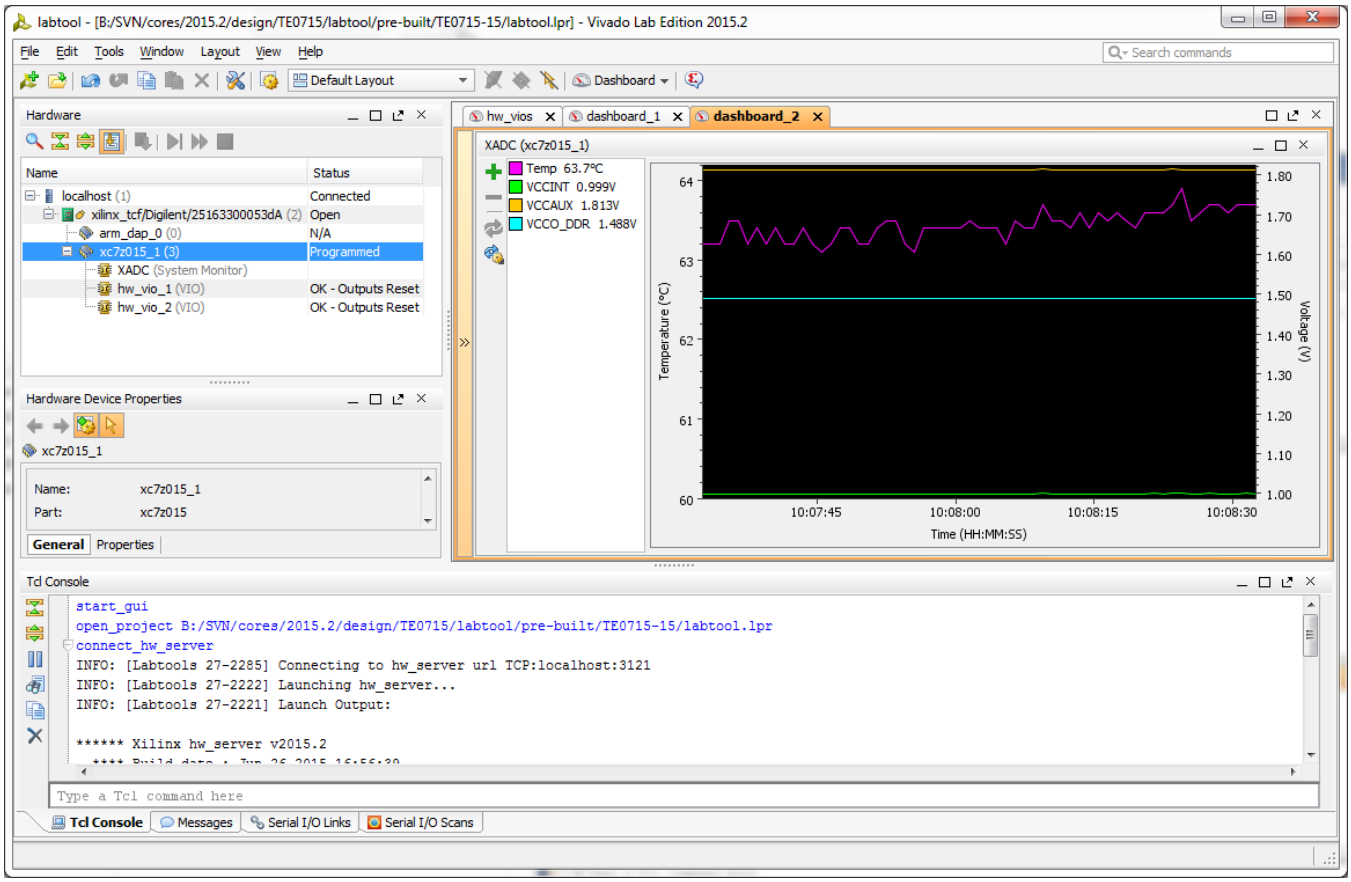
TE0715-xx-15 Micromodule with "VIO only" labtools pre-built design. This design does not depend on the PS subsystem being initialized by the Zynq Bootrom.



ZYNQ PS Fabric clocks can be monitored (the frequency depends on the FSBL settings). Frequency measurement reference is taken from Si5338 PLL supplied 125MHz clock. If this is not running then the PL fabric PLL flags would show clock stopped. In this dashboard it is also possible to toggle the output of DONE pin, setting it low would lit the DONE LED on TE0715.

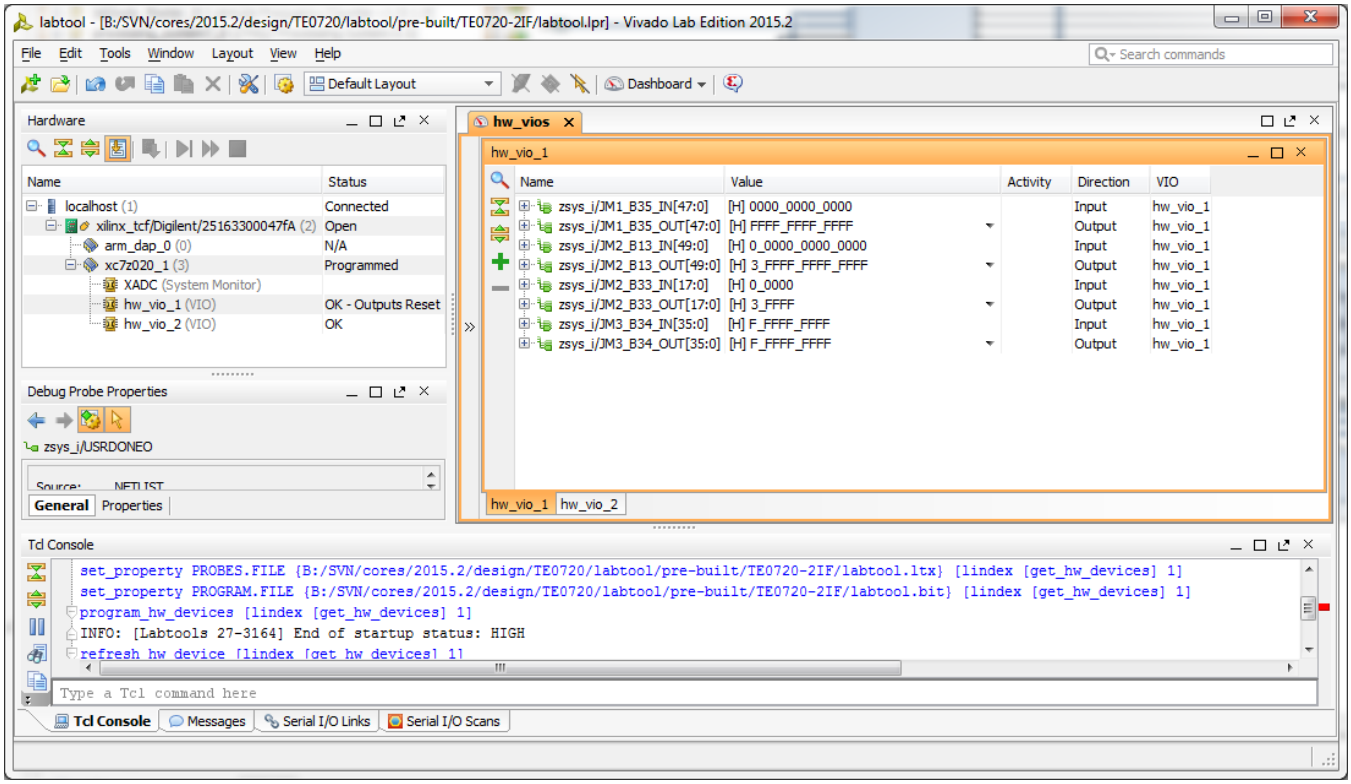


B2B I/O Pins can be monitored in this dashboard, if no external peripherals drive the I/O then all pins would show 1 as input value. It is also possible to force I/O pins to low by writing 0 into VIO OUT port.

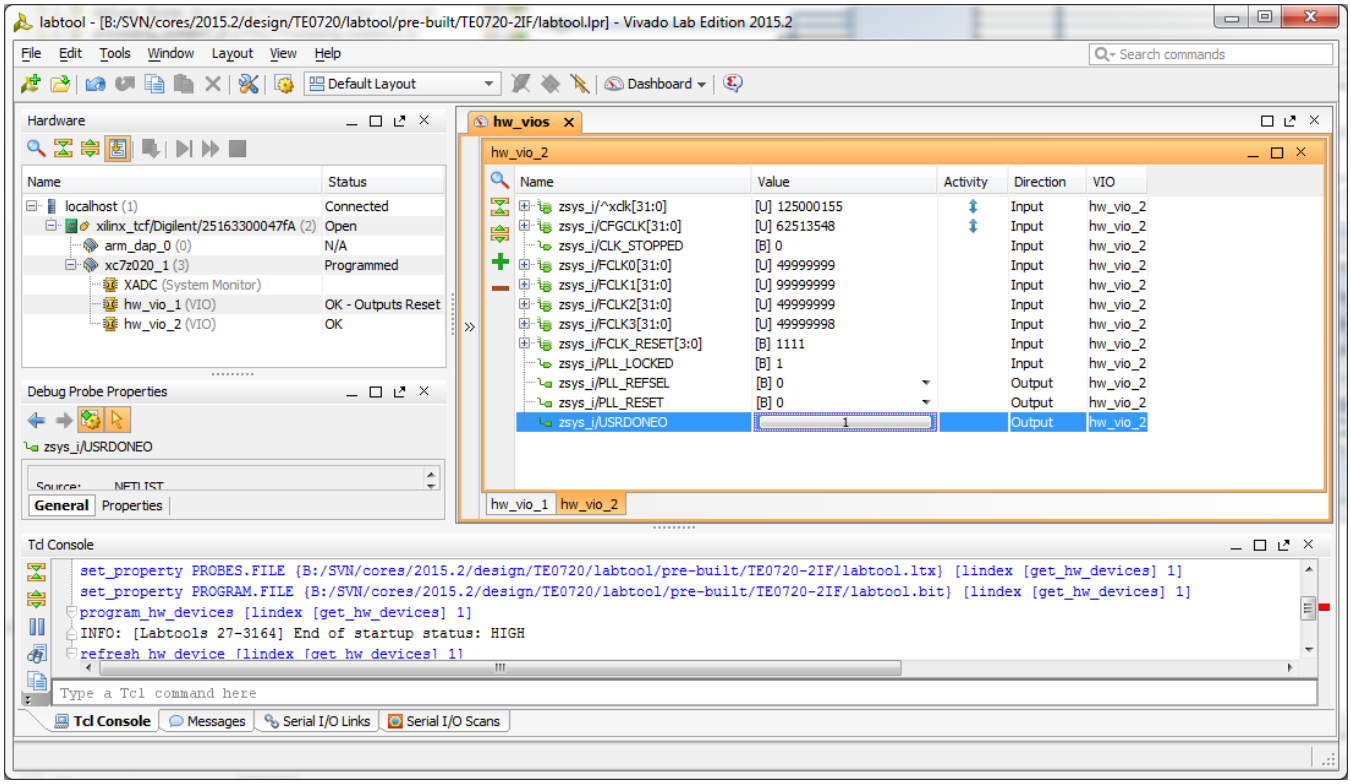


XADC can also be monitored to check the temperature and voltage sensor values.

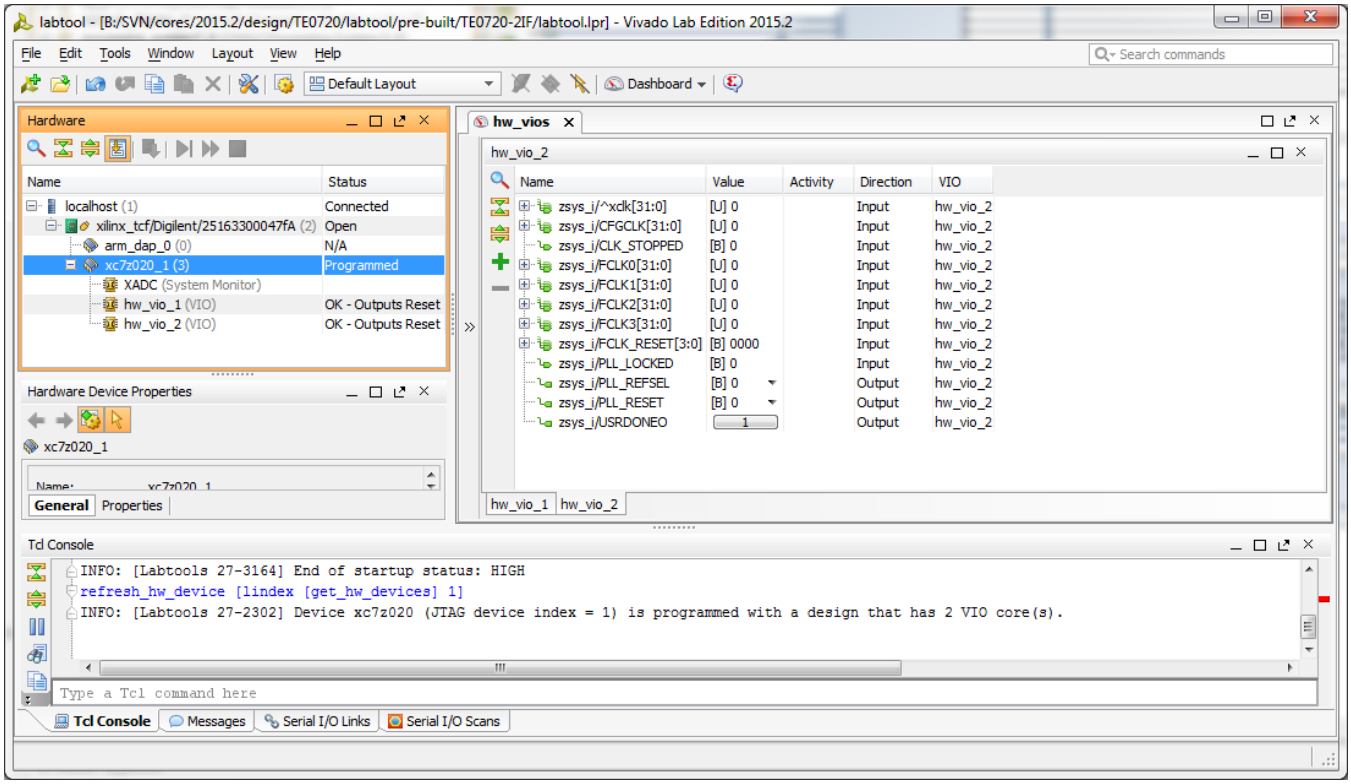
TE0720



B2B I/O Pins: TE0720 is on TE0703 baseboard with no user specified VCCIO supplied for banks B13, B33, B35 - unpowered banks Read Inputs as 0 (despite the IO pullups), only B34 reads inputs as high as this bank is powered (J5 is set on TE0703)

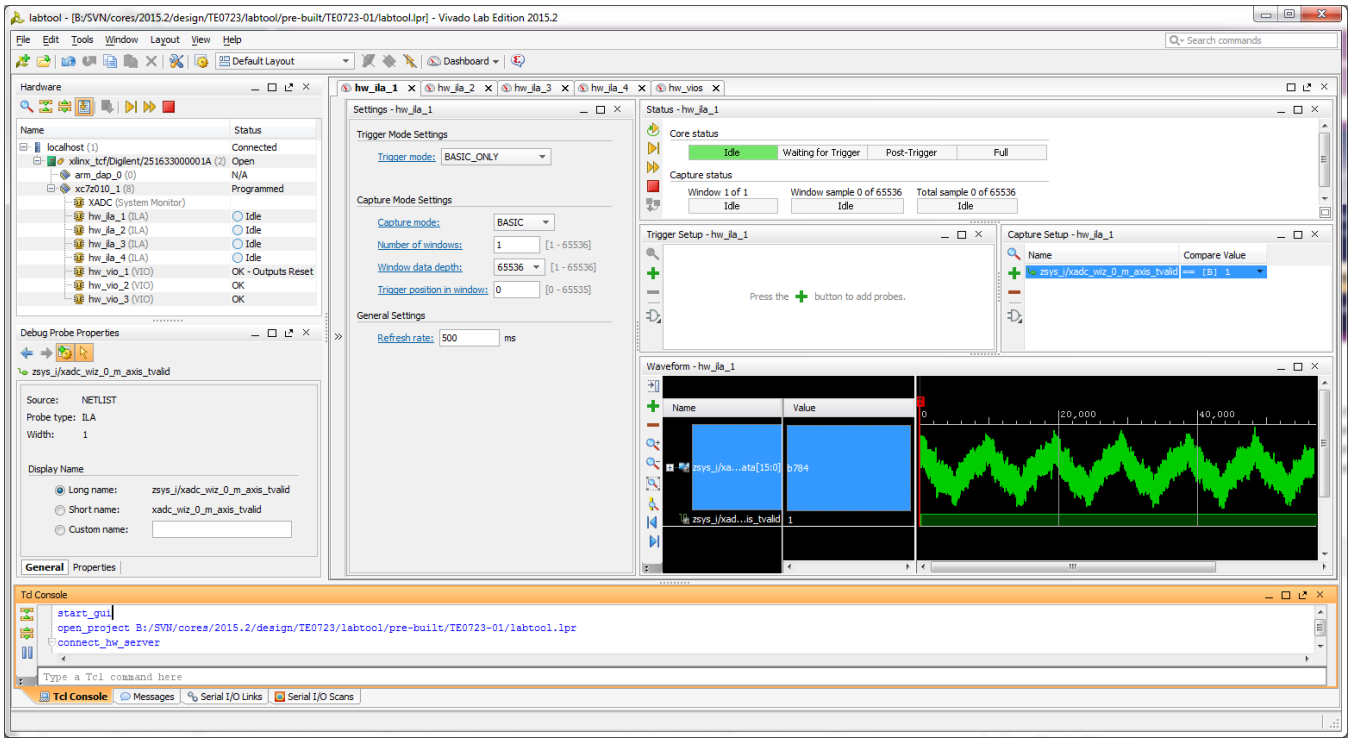


Clock measurements: 125MHz is Clock from Ethernet PHY, CFGCLK is FPGA internal configuration clock (nominal frequency 66MHz). TE0720 has no fixed PL clock sources, so the labtools design uses free running clock for all VIO's and PS supplied clock FCLK0 or FCLK3 as reference clock (it can be selected by changing PLL_REFSEL to 1 for FCLK0).



If the PS subsystem has executed FSBL (or it failed) then there are no clocks from PS, also the FCLK_RESET read as 0, this is indication that PS is not running at all.

TE0723



Reading analog values from XADC (50Hz noise visible)