

# PCN-20231110 TE0729-02 to TE0729-03 Hardware Revision Change

[Download PDF version of this document.](#)

<b>Company</b>	Trenz Electronic GmbH
<b>PCN Number</b>	PCN-20231110
<b>Title</b>	TE0729-02 to TE0729-03 Hardware Revision Change
<b>Subject</b>	Hardware Revision Change
<b>Issue Date</b>	2023-12-13

## Products Affected

This change affects all Trenz Electronic TE0729 SoMs: TE0729-02\*.

Affected Product	Replacement
TE0729-02-62I63MA	TE0729-03-62I63MA
TE0729-02-62I63MAK	TE0729-03-62I63MAK
TE0729-02-62I63MAS	TE0729-03-62I63MAS
TE0729-02-62I65MM	EOL
TE0729-02-62I63MAY	EOL

## Changes

### #1 Changed DCDC EN5311QI (U24, U25, U26) to MPM3834C and adapted power circuit.

**Type:** Schematic Change

**Reason:** EOL of Component.

**Impact:** None. Increased current output capability. Minor changes in electrical characteristics.

### #2 Changed DCDC EN6347QI (U23) to MPM3860GQW-Z and adapted power circuit.

**Type:** Schematic Change

**Reason:** EOL of Component.

**Impact:** None. Increased current output capability. Minor changes in electrical characteristics.

### #3 Changed load switch TPS27082LDDCR (Q1) to MP5077GG-Z and adapted circuit.

**Type:** Schematic Change

**Reason:** BOM Optimization.

**Impact:** None. Increased current output capability. Minor changes in electrical characteristics.

### #4 Added power supervisor (U4) for voltage rail VIN handling.

**Type:** Schematic Change

**Reason:** Power handling improvement.

**Impact:** Power supply starts only if voltage rail VIN is in adequate voltage range.

### #5 Changed power net name from 1.5V to DDR\_VDD.

**Type:** Schematic Change

**Reason:** Improve naming.

**Impact:** None.

### #6 Changed power sequencing.

**Type:** Schematic Change

**Reason:** Follow AMD and Texas Instruments recommendation.

**Impact:** Check that the new power-up sequence fits your requirements. Voltage supervisor (U4) enables 1V voltage rail (DCDC U23) via signal EN\_Module. 1V DCDC (U23) enables 1.8V voltage rail (DCDC U25) via signal PG\_1V0. 1.8V DCDC (U25) enables 2.5V (DCDC U24) and DDR\_VDD (DCDC U26) voltage rails via signal PG\_1V8. Voltage rail 3.3V (load switch Q1) is logical AND-enabled via power good signal PG\_2V5\_3V3 from voltage rail 2.5V DCDC (U24) and DDR\_VDD DCDC (U26) via diode (D4) and CPLD (U6) signal EN\_3V3 via diode (D5).

### #7 Added bidirectional level shifter (U7) and capacitors (C185, C186) to separate power domains for signal FPGA\_IO. Added fallback resistor (R91).

**Type:** Schematic Change

**Reason:** Improve power domain handling for signal FPGA\_IO.

**Impact:** None.

### #8 Added diode (D3) between U21 pin 3 net nRST\_in and voltage rail 3.3V.

**Type:** Schematic Change

**Reason:** Protect manual reset pin.

**Impact:** None.

## **#9 Added option to improve noise immunity for signal nRST\_in via capacitor C187 (default: not assembled).**

**Type:** Schematic Change

**Reason:** Improve noise immunity in needed cases.

**Impact:** None.

## **#10 Connected exposed pad for SDIO port expander (U15) to GND.**

**Type:** Schematic Change

**Reason:** Improve thermal situation.

**Impact:** None.

## **#11 Added additional decoupling capacitors C166...C179.**

**Type:** Schematic Change

**Reason:** Improve decoupling.

**Impact:** None.

## **#12 Changed 10 $\mu$ F capacitors (C36, C86) to 22 $\mu$ F.**

**Type:** Schematic Change

**Reason:** BOM Optimization.

**Impact:** None. Minor changes in electrical characteristics.

## **#13 Changed 22 $\mu$ F capacitors (C117, C121, C125, and C127) from size 0806 to 0603.**

**Type:** Schematic Change

**Reason:** BOM Optimization.

**Impact:** None. Minor changes in electrical characteristics.

## **#14 Changed capacitor (C144) from 470 nF, 6.3 V, X5R, 20 % to 100 nF, 16 V, X7R, 10 %.**

**Type:** Schematic Change

**Reason:** Increase battery input voltage range.

**Impact:** None. Changes in electrical characteristics.

## #15 Pulled-up board revision signal (FPGA U2 pin H17) and updated board revision documentation.

**Type:** Schematic Change

**Reason:** Update revision information.

**Impact:** None. Firmware reflects it but custom firmware needs to be updated by customer.

## #16 Changed fiducials to standard fiducial type.

**Type:** Schematic Change

**Reason:** Use standard fiducials.

**Impact:** None.

## #17 Removed track-it traceability pad S/N.

**Type:** Schematic Change

**Reason:** EOL of Component.

**Impact:** None.

## #18 Added testpoints TP1...TP41.

**Type:** PCB Change

**Reason:** Improve testing.

**Impact:** None.

## #19 Added serial number box print on bottom overlay.

**Type:** PCB Change

**Reason:** Required for manufacturing.

**Impact:** None.

## #20 Signal trace lengths changed

**Type:** PCB change

**Reason:** Result of changes above.

**Impact:** Changed trace length have to be taken into account in existing designs. The trace length for new revision will be available in [TE0729 series pinout generator](#). Please check if change in trace length still matches your requirements. Adaption of carrier may be necessary.

## #21 Added revision history, block and power diagram. Updated page count and order.

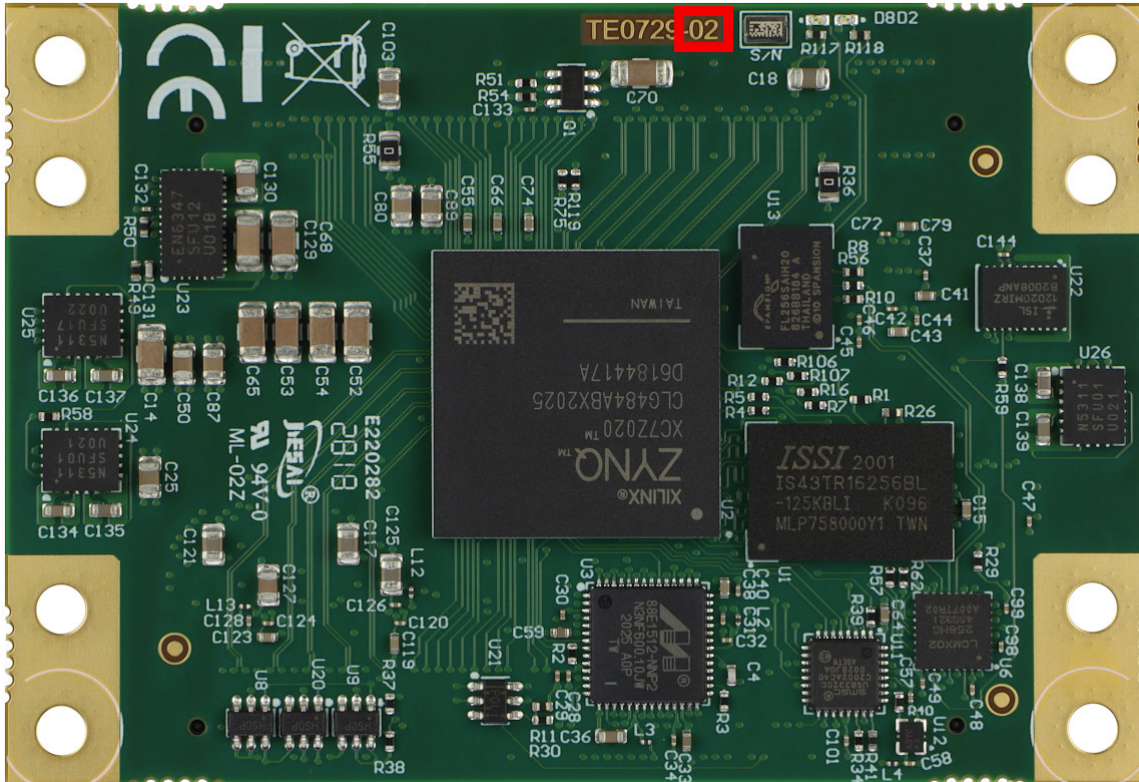
**Type:** Documentation Update

**Reason:** Documentation improvement.

**Impact:** None.

## Method of Identification

The revision number is visible on the top side of the PCB.



- international calls: 0049 5741 3200-0

## Disclaimer

Any projected dates in this PCN are based on the most current product information at the time this PCN is being issued, but they may change due to unforeseen circumstances. For the latest schedule and any other information, please contact your local Trenz Electronic sales office, technical support or local distributor.

This PCN follows JEDEC Standard J-STD-046.