ZYNQ Design not using A9 Cores

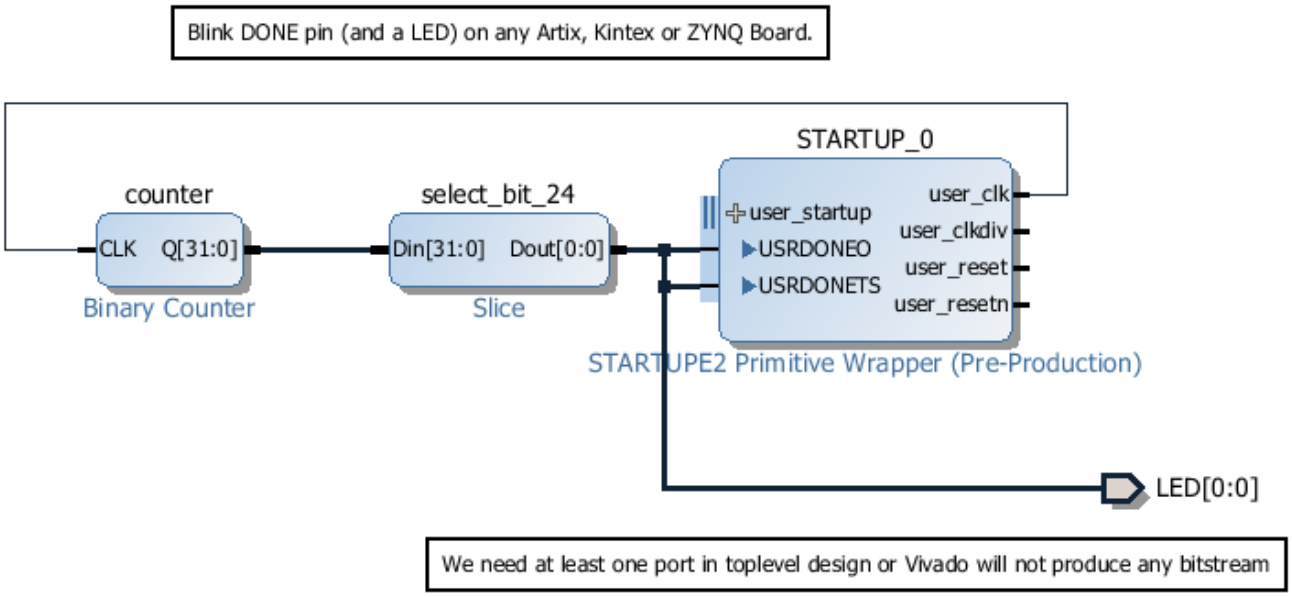
Boot and configuration

The only way to configure the PL portion without using the A9 Cores is JTAG. This is possible only during lab testing and troubleshooting.

> ⚠ If FPGA PL is loaded over JTAG and the Zynq CPU0 has not executed FSBL successfully, then the PS PLL supplied fabric clocks do not provide any clock to the PL Fabric.

PL only case

If PS supplied Fabric clocks are not required then a FPGA only design is possible without instantiating the PS7 Wrapper. Bitfiles generated from such design can be loaded by JTAG or by FSBL. For FSBL there is special option to specify that the bitfile does not instantiate the PS7 wrapper.



Blink a LED, this design will work on ANY Artix, Kintex, Virtex or Zynq Board and Blink DONE pin and one I/O pin.

PL using PS Peripherals

FPGA PL Design can access the PS connected peripherals, they are visible on AXI bus from the FPGA.

⚠ It is not possible to route PL Peripheral I/O to MIO pins.