Hardware Revision 2

#	Change	Type	Description/Reason
1	PS_CLK changed from 33.3333 to 50 MHz	component change	50 MHz is more reasonable if Zynq PS is operated in PLL bypass mode
2	32 MB winbond SPI changed to Spansion	component type change	32 Mbyte winbond is not supported in dual parallel mode
3	SPI flash size changed to 16 MB per device	component type change	Xilinx FSBL does auto-disable linear mode if devices larger 16MB are detected
4	SPI package changed from BGA to SO8W	component package change	easier in manufacturing and and optical inspection
5	antenna select 0R from 0201 to 0402	component package change	better for hand solder if need to change option after assembly
6	C29 to top layer and further away from conn		
7	move j7 to left		was too close to SD card metal housing
8	move c28		bad position no need to be so close to PCB edge there
9	add at least 2 LED on FPGA IO	enhancement	RGB LED would be best