TE0725 TRM

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Overview

The Trenz Electronic TE0725 is a low cost small-sized FPGA module integrating a Xilinx Artix-7 (15-100T) and 32 MByte Flash memory for configuration and operation.

Key Features

- Xilinx Artix-7 XC7A35T (A15 to A100T)
- Commercial Temperature Grade (Industrial on Request)
- 32 MByte Flash Memory
- 2 x 50 Pin Headers with 2,54mm Pitch, Ideal for Breadboard Use
- 87 IOs (42 + 42 + 3)
- 100 MHz System Clock
- I2C EEPROM
- 3.3V Single Power Supply with On-Board Voltage Regulators
- Size 73 x 35 mm
- JTAG/UART Connector
- 2 LED's
- Optional HyperRAM (8 to 32 MByte)
- Optional POF Fiber Optical Adapter (125/250 Mbps)

Block Diagram

TE0725-04

- 100.000000 MHz Oscillator → CLK_SYS → Bank 14
- HyperRAM ↔ Bank 15
- J1
- 42 x IOs, 21 x LVDS pairs ↔ Bank 35
- Green LED D2 ← SYSLED ← Bank 14

Xilinx Artix-7 FPGA

- Bank 14 ↔ Quad SPI Flash
- Bank 0 → SPI_SCK → Quad SPI Flash
- Bank 14 ↔ I²C ↔ Serial EEPROM
- Bank 34 ↔ 42 x IOs, 21 x LVDS pairs ↔ J2
- Bank 16 ↔ POF Transceiver
- Bank 0 → DONE → Red LED D3
- Bank 0 / Bank 14 — JTAG / XMOD / UART → JB1
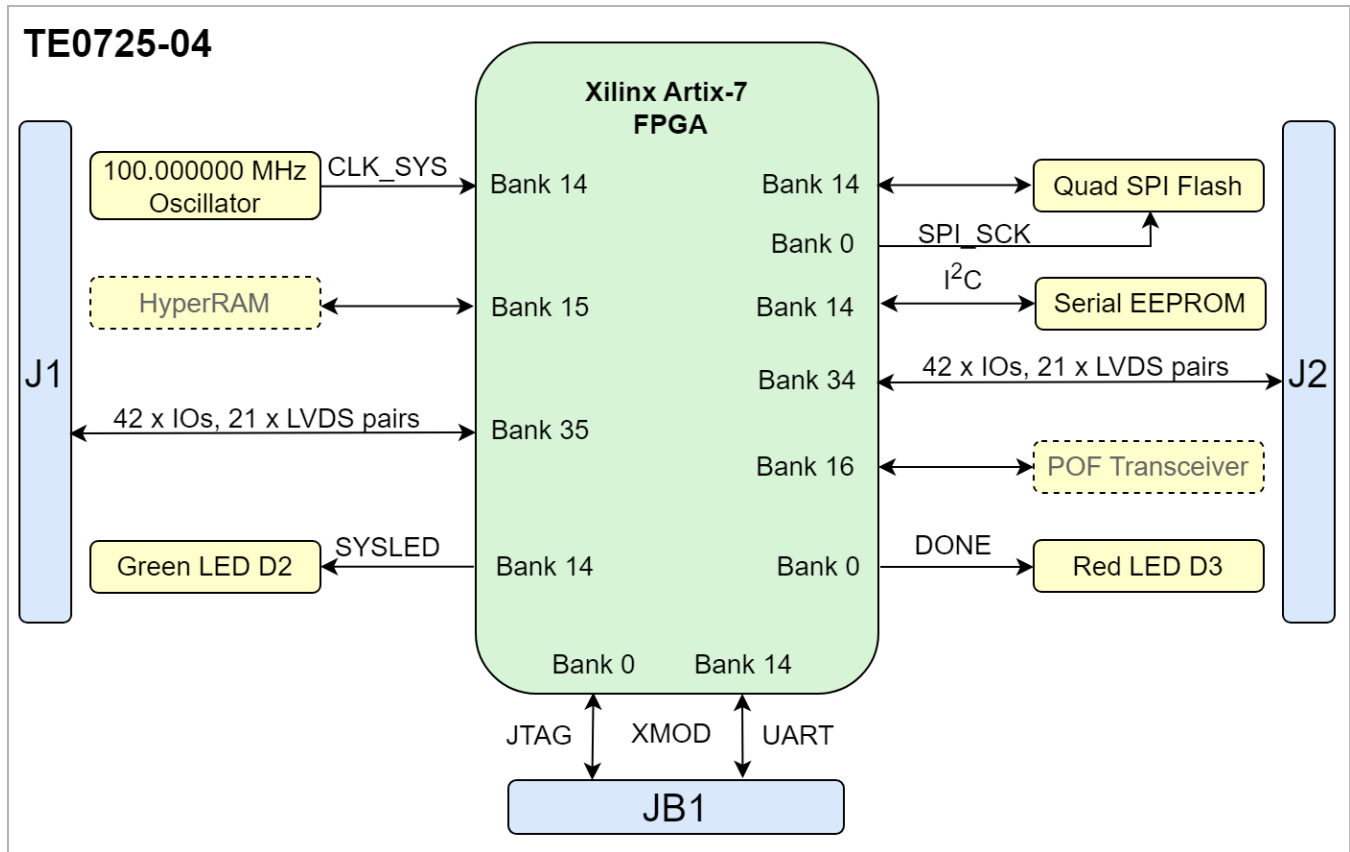
Main Components

Note on the images below, that there is no POF transceiver, no 50-pin headers and no JTAG/UART header installed.
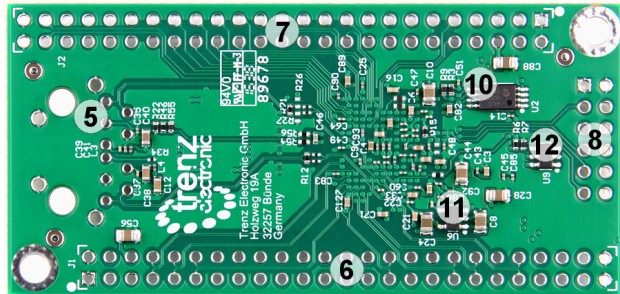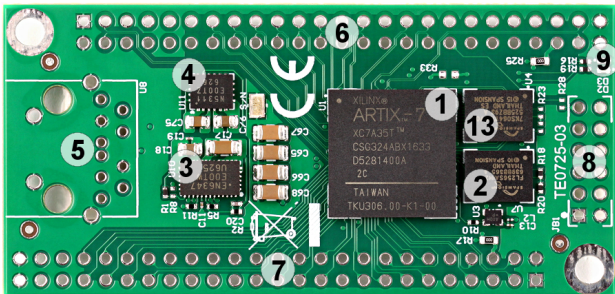
1. Xilinx Artix-7 FPGA, U1
2. 32-MByte Flash memory, U7
3. Enpirion EN6347 4A PowerSoC DC-DC step down converter, U10
4. Enpirion EN5311 1A PowerSoC synchronous buck regulator with integrated inductor, U11
5. POF transceiver placeholder, U8
6. 50-pin placeholder for breadboard connector, J1

7. 50-pin placeholder for breadboard connector, J2
8. JTAG/UART connector, JB1
9. Green LED D2(SYSLED) and red LED D3(DONE)
10. 16K x 8 (128-Kbit) serial EEPROM, U2
11. Low-noise, high PSRR, RF, 200-mA low-dropout linear regulator, U9
12. Ultra-low supply-current voltage monitor with optional watchdog, U6
13. Cypress S27KS0641 64-Mbit (8-MByte) HyperRAM™ self-refresh DRAM, U4

Signals, Interfaces and Pins

I/O Banks

Bank	VCCIO	B2B I/O	Notes
0	3.3V	0	JTAG
14	3.3V	0 (3)	3 I/O in XMOD-JTAG - for use as UART
15	1.8V	0	used for optional hyper RAM
16	2.5V	0	used for optional optical fiber transceiver
34	User select	42	0R resistor option to select 3.3V
35	User select	42	0R resistor option to select 3.3V

JTAG Interface

JTAG access to the Xilinx Artix-7 device is provided through connector JB1.

Signal	Pin Number
TCK	JB1-4
TDO	JB1-8
TDI	JB1-10
TMS	JB1-12
JTAGVREF(VIO)	JB1-6
GND	JB1-1, JB1-2

Connector JB1 (2 x 6 pin header) is compatible with XMOD JTAG adapter TE0790. This adapter can be inserted from top onto the TE0725, if JB1 is fitted with male pin header. Optionally JB1 can be fitted with pin header from bottom, in that case the JTAG cable connector must be on the base board. When using XMOD-JTAG in JB1 then additionally USB UART is usable, and the push-button on XMOD works as configuration reset.

Recommended TE0790 (XMOD) DIP-switch settings :

- S2-1: ON
- S2-2: OFF
- S2-3: OFF
- S2-4: OFF

TE0790 can be in some cases used to power up TE0725 (other TE0790 DIP settings), however this is not recommended. TE0790-01 can not supply enough power for TE0725 (LED may blink but the module is not operating properly, especially in case of larger and more sophisticated designs).

POF Transceiver

blocked URL

Model	Bitrate MB/s	Notes

AFBR-59F2Z	250	

On-board LED's

LED	Color	FPGA	Notes
D2	Green	M16	
D3	Red	DONE	Active low

Connectors

All connectors are are for 100mil headers, all connector locations are in 100 mil grid.

LED	Color	FPGA	Notes
D2	Green	M16	
D3	Red	DONE	Active low

Power and Power-On Sequence

To power-up a module, power supply with minimum current capability of 1A is recommended.

Power Supply

TE0725 needs one single power supply with nominal of 3.3V.

Power Consumption

FPGA	Design	Typical Power, 25C ambient
A35T	Not configured	TBD*
A35T	LED blinking	170mW (typical)
A100T	Not configured	TBD*

*TBD - To Be Determined.

Actual power consumption depends on the FPGA design and ambient temperature.

Power-On Sequence

There is no specific or special power-on sequence, single power source is needed as VIN, rest of the sequence is automatic.

Variants Currently In Production

Trenz shop TE0725 overview page	
English page	German page

Technical Specifications

Absolute Maximum Ratings

Parameter	Min	Max	Units	Reference document
3.3V supply voltage	-0.1	3.6	V	
HR I/O banks supply voltage (VCCO)	-0.5	3.6	V	Xilinx datasheet DS181
HR I/O banks input voltage	-0.4	VCCO + 0.55	V	Xilinx datasheet DS181
Storage Temperature	-40	+85	°C	

Recommended Operating Conditions

Parameter	Min	Max	Units	Reference document
VIN supply voltage	3.135	3.45	V	
HR I/O banks supply voltage (VCCO)	1.14	3.465	V	Xilinx datasheet DS181
HR I/O banks input voltage	-0.20	VCCO + 0.20	V	Xilinx datasheet DS181
Operating Temperature	0	+85	°C	

⚠ Please check Xilinx datasheet DS181 for complete list of absolute maximum and recommended operating ratings for the Artix-7 device.

Physical Dimensions

Please note that two different units are used on the figures below, SI system millimeters (mm) and imperial system thousandths of an inch(mil). This is because of the 100mil pin headers used, see also explanation below. To convert mils to millimeters and vice versa use formula 100mil's = 2,54mm.
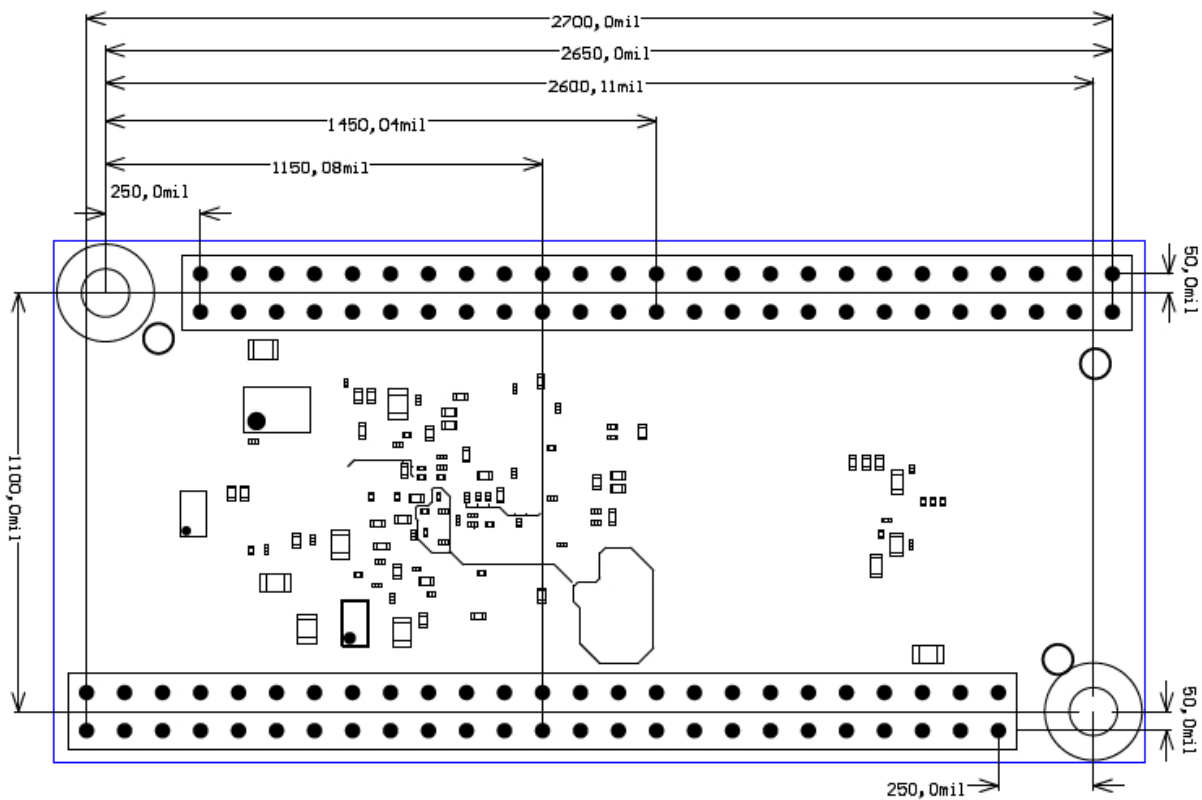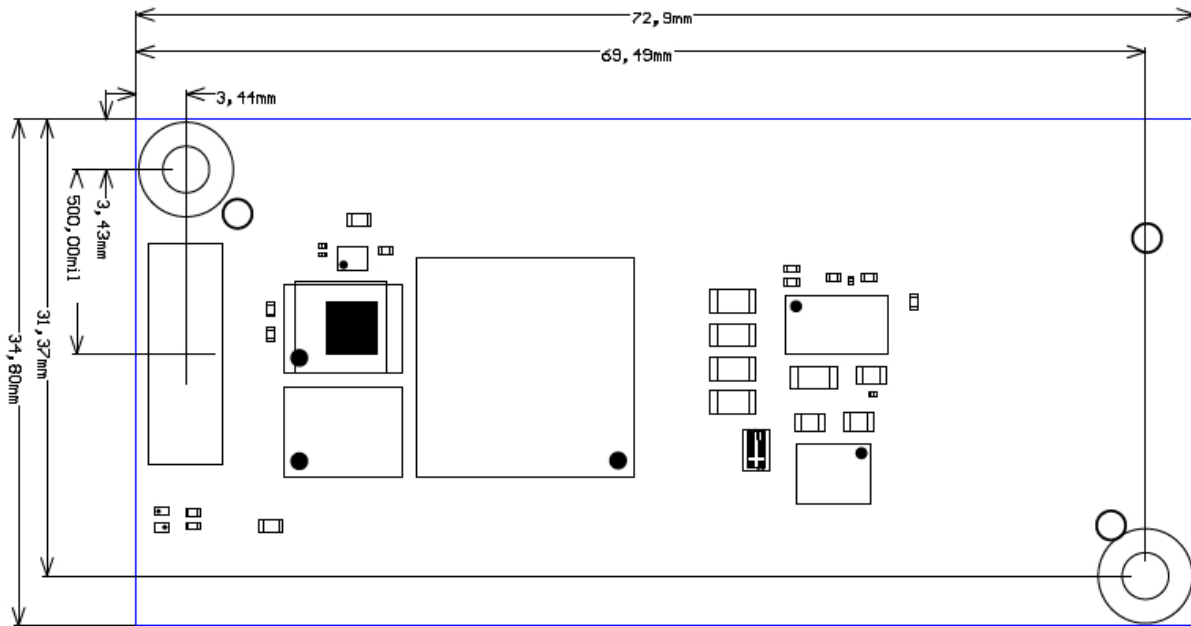
All 100 mil pin headers are in 100 mil grid, the M3 mounting holes are in 50 mil grid aligned to the centers of the 100mil headers. The module is symmetrical, turning it 180 degrees will keep all I/O and Power pins in both 50 pin headers in compatible places.

Operating Temperature Ranges

Commercial grade modules

All parts conform to at least commercial temperature range of 0°C to +70°C.

Industrial grade modules

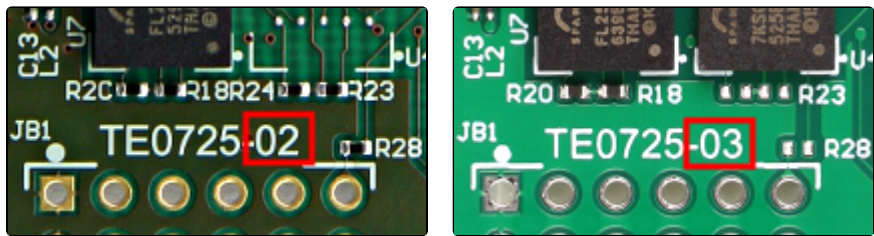All parts are at least industrial temperature range of -40°C to +85°C.

The module operating temperature range depends on customer design and cooling solution. Please contact us for options.

Revision History

Hardware Revision History

Date	Revision	Notes	PCN	Documentation Link
2016-12-09	03	Second production release	Click to see PCN	TE0725-03
-	02	First production release		TE0725-02
-	01	Prototypes		

Hardware revision number is printed on the PCB board together with the module model number separated by the dash.

Document Change History

Date	Revision	Contributors	Description

Error rendering macro 'page-info' Ambiguous method overloading for method jdk. proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com. atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian. confluence.user.ConfluenceUser, class java.lang.String, class com. atlassian.confluence.core. ContentEntityObject] [interface com. atlassian.user.User, class java.lang. String, class com.atlassian. confluence.core. ContentEntityObject]	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk. proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com. atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian. confluence.user.ConfluenceUser, class java.lang.String, class com. atlassian.confluence.core. ContentEntityObject] [interface com. atlassian.user.User, class java.lang. String, class com.atlassian. confluence.core. ContentEntityObject]	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk. proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com. atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian. confluence.user.ConfluenceUser, class java.lang.String, class com. atlassian.confluence.core. ContentEntityObject] [interface com. atlassian.user.User, class java.lang. String, class com.atlassian. confluence.core. ContentEntityObject]	• Block Diagram is updated.
2021-09-02	v.66	John Hartfiel	• add JTAG notes.
2021-02-11	v.65	John Hartfiel	• Replace Links.
2017-06-07	v.60	Jan Kumann	• Minor formatting.
2017-01-27	v.57	Jan Kumann	• New block diagram.
2017-01-12	v.46	Jan Kumann	• Revision 03 product images added.

2016-12-15		Thorsten Trenz	• Hardware revision 03 specific information added.
2016-12-09	v.40	Jan Kumann	• Hardware revision 02 block diagram added.
2016-12-02	v.1	Antti Lukats	• Initial version.

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