DDR less ZYNQ Design

> ⚠ This is preliminary based on Vivado 2016.1 release, the "DDR Less" flow should become even easier with the next Vivado releases. Hope remains.

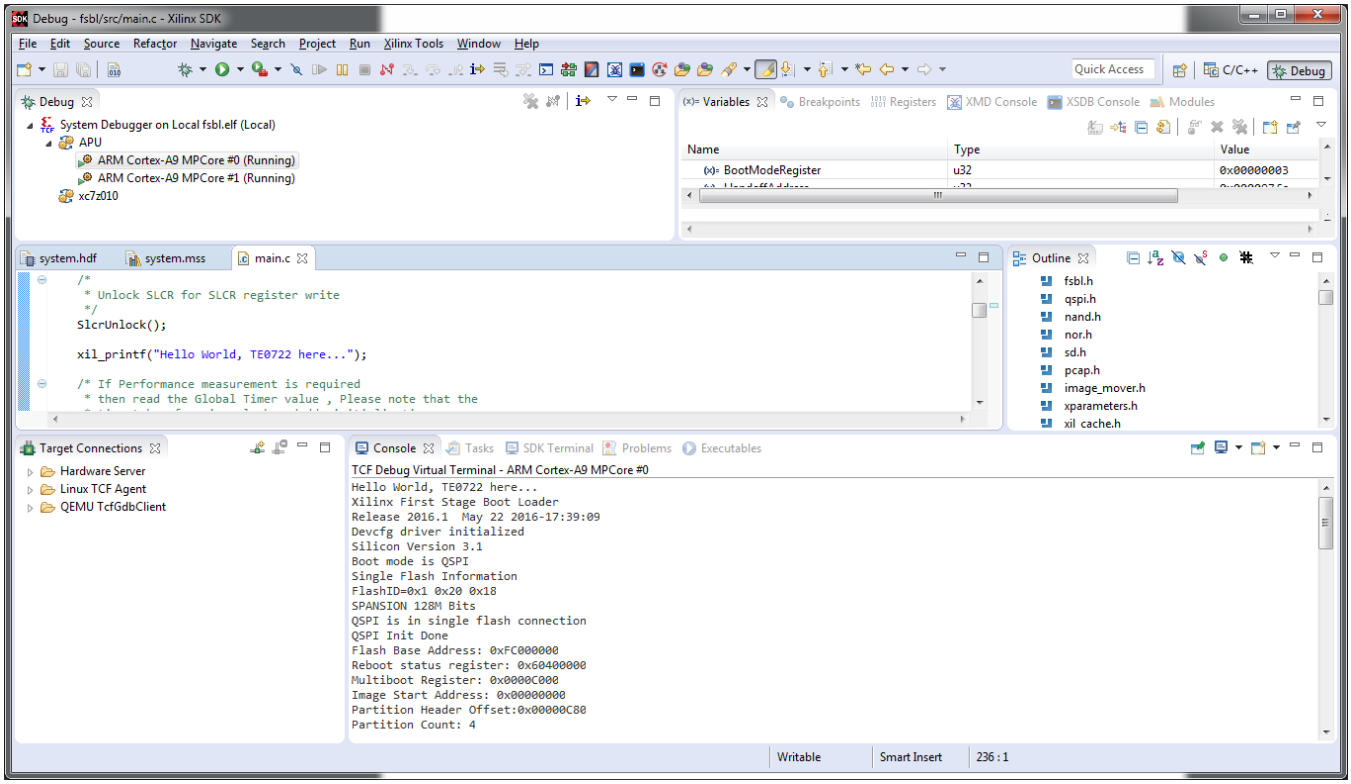
Step by Step

1. In Vivado IPI create a BD and configure PS7 block with no DDR, one UART should be enabled also, even if you do not use UART in your application
2. in SDK create FSBL, in main.c add one line, and comment out one line:
   #define XPAR_PS7_DDR_0_S_AXI_BASEADDR 0
   #ifdef XPAR_PS7_DDR_0_S_AXI_BASEADDR
   //Status = DDRInitCheck();
3. Create BOOT.BIN

Thats all, PS will load the FPGA bitstream and then do nothing. There is no need to patch the init tcl script, it does not include the DDR init so it will not freeze.

> ⚠ Do not add "hello.elf" as application to the BOOT.BIN, it would yield in non bootable boot image

Loading application to be run after bitstream loading is also possible, more FSBL changes are needed then.



Example DDR less Zynq system debug session, FSBL with JTAG DCC console running on TE0722.

Related Links:

- https://www.xilinx.com/support/answers/56044.html
- http://www.wiki.xilinx.com/Zynq-7000+AP+SoC+Boot+-+Booting+and+Running+Without+External+Memory+Tech+Tip