TE0715 TRM

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Table of Contents

- Overview
  - Key Features
  - Block Diagram
  - Main Components
  - Initial Delivery State
- Boot Process
- Signals, Interfaces and Pins
  - Board to Board (B2B) I/Os
  - MGT Lanes
  - JTAG Interface
  - System Controller CPLD I/O Pins
  - Quad SPI Interface
  - SD Card Interface
  - Ethernet Interface
  - USB Interface
  - I2C Interface
- On-board Peripherals
  - System Controller CPLD
  - DDR Memory
  - Quad SPI Flash Memory
  - Gigabit Ethernet PHY
  - High-speed USB ULPI PHY
  - MAC Address EEPROM
  - RTC - Real Time Clock
  - Programmable Clock Generator
  - Oscillators
  - On-board LEDs
- Power and Power-On Sequence
  - Power Consumption
  - Power Distribution Dependencies
  - Power-On Sequence
  - Power Rails
  - Bank Voltages
- Board to Board Connectors
  - Connector Mating height
  - Connector Speed Ratings
  - Current Rating
  - Connector Mechanical Ratings
  - Manufacturer Documentation
- Variants Currently in Production
- Technical Specifications
  - Absolute Maximum Ratings
  - Recommended Operating Conditions
  - Operating Temperature Ranges
  - Physical Dimensions
- Revision History
  - Hardware Revision History
  - Document Change History
- Disclaimer
  - Data Privacy
  - Document Warranty
  - Limitation of Liability
  - Copyright Notice
  - Technology Licenses
  - Environmental Protection
  - REACH, RoHS and WEEE

Overview

The Trenz Electronic TE0715 is an industrial-grade SoM (System on Module) based on Xilinx Zynq-7000 SoC (XC7Z015 or XC7Z030) with 1GByte of DDR3 SDRAM, 32MBytes of SPI Flash memory, Gigabit Ethernet PHY transceiver, a USB PHY transceiver and powerful switching-mode power supplies for all on-board voltages. A large number of configurable I/Os is provided via rugged high-speed stacking strips.

Key Features

- Industrial-grade Xilinx Zynq-7000 SoC (XC7Z015, XC7Z030)
- Rugged for shock and high vibration
- 2 × ARM Cortex-A9
- 10/100/1000 Mbps Ethernet transceiver PHY
- MAC address EEPROM
- 32-bit wide 1GB DDR3 SDRAM
- 32 MByte quad SPI Flash memory
- Programmable clock generator
    - Transceiver clock (default 125 MHz)
- Plug-on module with 2 × 100-pin and 1 × 60-pin high-speed hermaphroditic strips
- 132 FPGA I/Os (65 LVDS pairs possible) and 14 PS MIO available on B2B connectors
- 4 GTP/GTX (high-performance transceiver) lanes
    - GTP/GTX (high-performance transceiver) clock input
- USB 2.0 high-speed ULPI transceiver
- On-board high-efficiency DC-DC converters
    - 4 A x 1.0 V power rail
    - 3 A x 1.0 V power rail
    - 3 A x 1.2 V power rail
    - 3 A x 1.35 V power rail
    - 3 A x 1.8 V power rail
- System management
- eFUSE bit-stream encryption
- AES bit-stream encryption
- Temperature compensated RTC (real-time clock)
- User LED
- Evenly-spread supply pins for good signal integrity

Additional assembly options are available for cost or performance optimization upon request.

Block Diagram

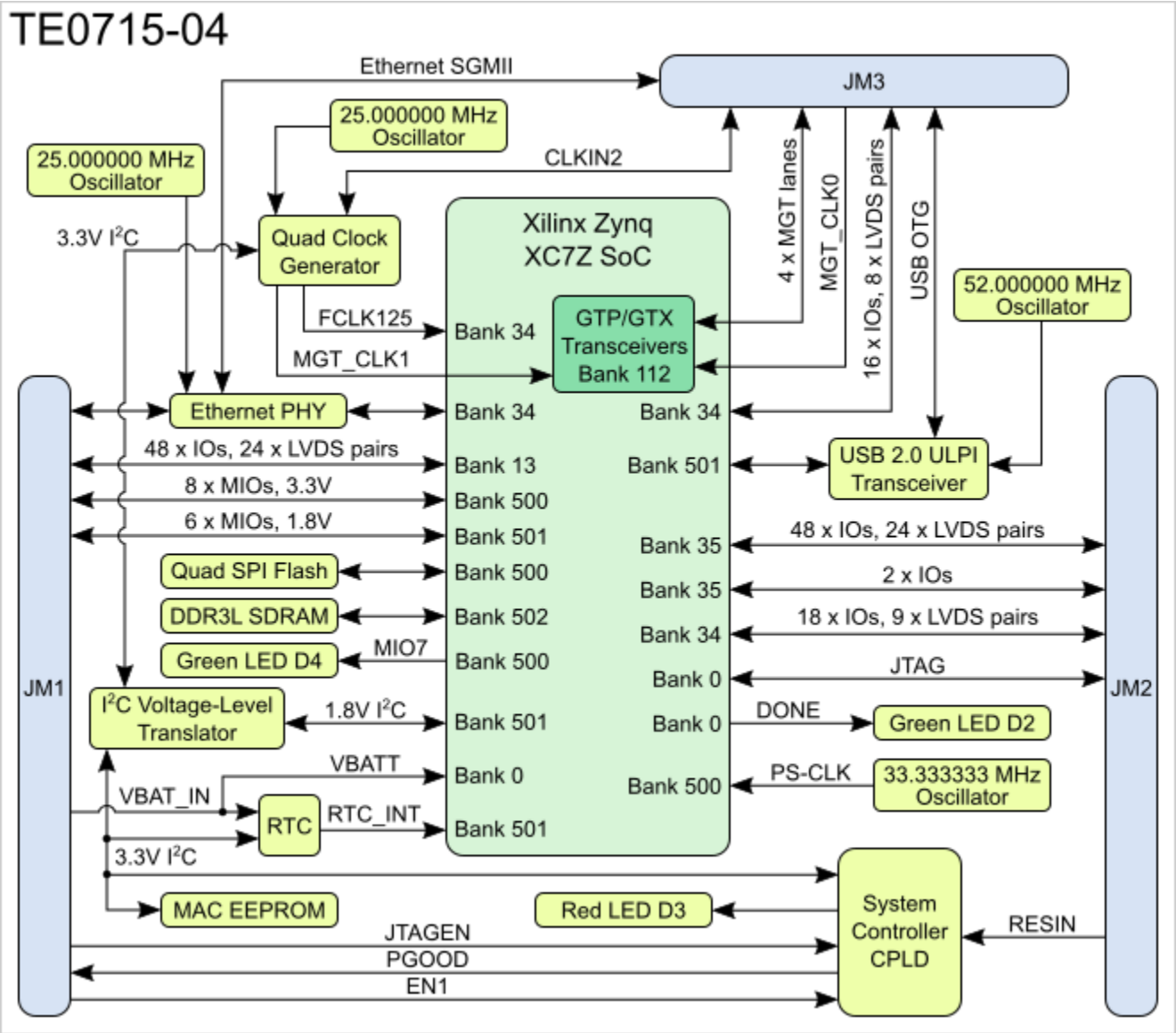


Figure 1: TE0715 block diagram.

Main Components

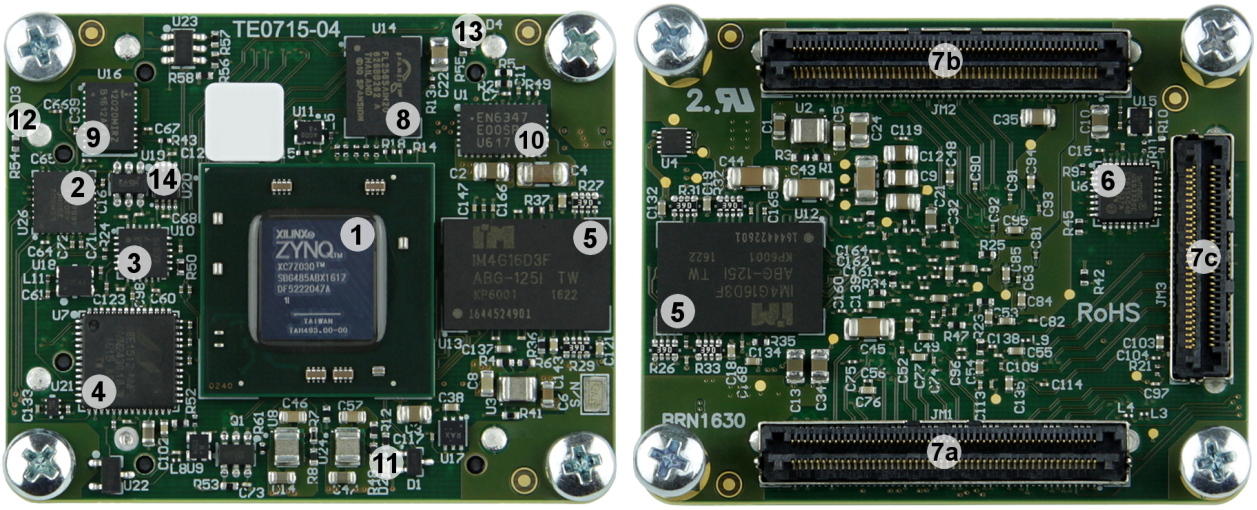


Figure 2: TE0715 main components.

- 1. Xilinx Zynq-7000 all programmable SoC, U5
- 2. System Controller CPLD, U26
- 3. Programmable quad clock generator , U10
- 4. 10/100/1000 Mbps Ethernet PHY, U7
- 5. 2 x 4-Gbit DDR3L SDRAM (1.35 V), U12 and U13
- 6. Hi-speed USB 2.0 ULPI transceiver, U6
- 7a. B2B connector Samtec Razor Beam™ LSHM-150, JM1
- 7b. B2B connector Samtec Razor Beam™ LSHM-150, JM2
- 7c. B2B connector Samtec Razor Beam™ LSHM-130, JM3
- 8. 32-MByte quad SPI Flash memory, U14
- 9. Low-power RTC with battery backed SRAM, U16
- 10. 4A PowerSoC DC-DC converter, U1
- 11. Green LED (DONE), D2
- 12. Red LED (SC), D3
- 13. Green LED (MIO7), D4
- 14. 2-bit bidirectional 1-MHz I^2C bus voltage-level translator, U20

Initial Delivery State

Storage device name	Content	Notes
24AA025E48 EEPROM	User content not programmed	Valid MAC address from manufacturer.
SPI Flash OTP Area	Empty, not programmed	Except serial number programmed by flash vendor.
SPI Flash Quad Enable bit	Programmed	-
SPI Flash main array	Demo design	-
eFUSE USER	Not programmed	-
eFUSE Security	Not programmed	-
Si5338 OTP NVM	Default settings pre-programmed	OTP not re-programmable after delivery from factory

Table 1: Initial delivery state of programmable devices on the module.

Boot Process

By default the TE-0715 supports quad SPI and SD Card boot modes which is controlled by the MODE input signal from the B2B JM1 connector.

MODE Signal State	Boot Mode
High or open	QSPI
Low or ground	SD Card

Table 2: Boot MODE signal description.

Signals, Interfaces and Pins

Board to Board (B2B) I/Os

I/O signals connected to the SoC's I/O bank and B2B connector:

Bank	Type	B2B Connector	I/O Signal Count	Voltage	Notes
13	HR	JM1	48	User	Allowed voltage level from 1.2V to 3.3V.
34	HR/HP	JM2	18	User	• On TE0715-xx-15 modules, banks 34 and 35 are HR banks, allowed voltage level from 1.2V to 3.3V. • On TE0715-xx-30 modules, banks 34 and 35 are HP banks, allowed voltage level from 1.2V to 1.8V.
35	HR/HP	JM2	50	User	As above.
34	HR/HP	JM3	16	User	As above.
500	MIO	JM1	8	3.3V	-
501	MIO	JM1	6	1.8V	-
112	GT	JM3	4 lanes	N/A	See also next section MGT Lanes.
112	GT CLK	JM3	1 differential input	N/A	NB! AC coupling capacitors required on carrier board.

Table 3: General overview of board to board I/O signals.

For detailed information about the pin-out, please refer to the Pin-out Table.

MGT Lanes

MGT (Multi Gigabit Transceiver) lane consists of one transmit and one receive (TX/RX) differential pairs, four signals total per one MGT lane. Following table lists lane number, MGT bank number, transceiver type, signal schematic name, board-to-board connector connection and Zynq SoC pin connection:

Lane	Bank	Type	Signal Name	B2B Pin	Zynq SoC Pin

0	112	GTX	• MGT_RX0_P • MGT_RX0_N • MGT_TX0_P • MGT_TX0_N	• JM3-10 • JM3-8 • JM3-9 • JM3-7	• MGTXRXP0_112, AA7 • MGTXRXN0_112, AB7 • MGTXTXP0_112, AA3 • MGTXTXN0_112, AB3
1	112	GTX	• MGT_RX1_P • MGT_RX1_N • MGT_TX1_P • MGT_TX1_N	• JM3-16 • JM3-14 • JM3-15 • JM3-13	• MGTXRXP1_112, W8 • MGTXRXN1_112, Y8 • MGTXTXP1_112, W4 • MGTXTXN1_112, Y4
2	112	GTX	• MGT_RX2_P • MGT_RX2_N • MGT_TX2_P • MGT_TX2_N	• JM3-22 • JM3-20 • JM3-21 • JM3-19	• MGTXRXP2_112, AA9 • MGTXRXN2_112, AB9 • MGTXTXP2_112, AA5 • MGTXTXN2_112, AB5
3	112	GTX	• MGT_RX3_P • MGT_RX3_N • MGT_TX3_P • MGT_TX3_N	• JM3-28 • JM3-26 • JM3-27 • JM3-25	• MGTXRXP3_112, W6 • MGTXRXN3_112, Y6 • MGTXTXP3_112, W2 • MGTXTXN3_112, Y2

Table 4: MGT lanes overview.

Below are listed MGT bank reference clock sources.

Clock signal	Bank	Source	FPGA Pin	Notes
MGT_CLK0_P	112	B2B, JM3-33	MGTREFCLK0P_112, U9	Supplied by the carrier board.
MGT_CLK0_N	112	B2B, JM3-31	MGTREFCLK0N_112, V9	Supplied by the carrier board.
MGT_CLK1_P	112	U10, CLK2A	MGTREFCLK1P_112, U5	On-board Si5338A.
MGT_CLK1_N	112	U10, CLK2B	MGTREFCLK1N_112, V5	On-board Si5338A.

Table 5: MGT reference clock sources.

JTAG Interface

JTAG access to the Xilinx Zynq SoC is provided through B2B connector JM2.

JTAG Signal	B2B Connector Pin
TMS	JM2-93
TDI	JM2-95
TDO	JM2-97
TCK	JM2-99

Table 6: JTAG interface signals.

⚠ JTAGEN pin in B2B connector JM1 should be kept low or grounded for normal operation.

System Controller CPLD I/O Pins

Special purpose pins are connected to System Controller CPLD and have following default configuration:

Pin Name	Mode	Function	Default Configuration
EN1	Input	Power Enable	No hard wired function on PCB, when forced low pulls POR_B low to emulate power on reset.
PGOOD	Output	Power Good	Active high when all on-module power supplies are working properly.
NOSEQ	-	-	No function.
RESIN	Input	Reset	Active low reset, gated to POR_B.
JTAGEN	Input	JTAG Select	Low for normal operation.

Table 7: System Controller CPLD I/O pins.

Quad SPI Interface

Quad SPI Flash (U14) is connected to the Zynq PS QSPI0 interface via PS MIO bank 500, pins MIO1 ... MIO6.

Zynq SoC's MIO	Signal Name	U5 Pin
1	SPI-CS	C2
2	SPI-DQ0/M3	D3
3	SPI-DQ1/M1	D2
4	SPI-DQ2/M2	C4
5	SPI-DQ3/M0	D4
6	SPI-SCK	B2

Table 8: Quad SPI interface signals and connections.

SD Card Interface

SD Card interface is connected form the Zynq SoC's PS MIO bank 501 to the B2B connector JM1, signals MIO40 .. MIO45.

Ethernet Interface

On-board Gigabit Ethernet PHY is provided with Marvell Alaska 88E1512 IC (U7). The Ethernet PHY RGMII interface is connected to the Zynq Ethernet0 PS GEM0. I/O voltage is fixed at 1.8V for HSTL signalling. SGMII (SFP copper or fiber) can be used directly with the Ethernet PHY, as the SGMII pins are available on the B2B connector JM3. The reference clock input of the PHY is supplied from an on-board 25.000000 MHz oscillator (U9), the 125MHz output clock signal CLK_125MHZ is connected to the IN5 pin of the PLL chip (U10).

Ethernet PHY connection

PHY Pin	Zynq PS	Zynq PL	Notes
MDC/MDIO	MIO52, MIO53	-	-
LED0	-	J3	Can be routed via PL to any free PL I/O pin in B2B connector.

LED1	-	K8	Can be routed via PL to any free PL I/O pin in B2B connector. This LED is connected to PL via level-shifter implemented in system controller CPLD.
LED2/Interrupt	MIO46	-	-
CONFIG	-	-	By default the PHY address is strapped to 0x00, alternate configuration is possible.
RESETn	MIO50	-	-
RGMII	MIO16..MIO27	-	-
SGMII	-	-	Routed to B2B connector JM3.
MDI	-	-	Routed to B2B connector JM1.

Table 9: Ethernet interface.

USB Interface

USB PHY is provided by USB3320 from Microchip. The ULPI interface is connected to the Zynq PS USB0. The I/O Voltage is fixed at 1.8V. The reference clock input of the PHY is supplied from an on-board 52.000000 MHz oscillator (U15).

USB PHY connection

PHY Pin	ZYNQ Pin	B2B Name	Notes
ULPI	MIO28..39	-	Zynq USB0 MIO pins are connected to the PHY.
REFCLK	-	-	52.000000 MHz from on board oscillator (U15).
REFSEL[0..2]	-	-	Reference clock frequency select, all set to GND selects 52.000000 MHz.
RESETB	MIO51	-	Active low reset.
CLKOUT	MIO36	-	Connected to 1.8V, selects reference clock operation mode.
DP, DM	-	OTG_D_P, OTG_D_N	USB data lines.
CPEN	-	VBUS_V_EN	External USB power switch active high enable signal.
VBUS	-	USB_VBUS	Connect to USB VBUS via a series of resistors, see reference schematics.
ID	-	OTG_ID	For an A-device connect to the ground, for a B-device leave floating.

Table 10: USB interface.

The schematics for the USB connector and required components is different depending on the USB usage. USB standard A or B connectors can be used for host or device modes. A mini-USB connector can be used for USB device mode. A micro-USB connector can be used for device mode, OTG mode or host mode.

I2C Interface

On-board I^2C devices are connected to the Zynq SoC's PS bank 501 MIO48 (SCL) and MIO49 (SDA) which is configured as I2C1 by default. As bank 501 VCC_MIO1_501 is fixed to 1.8V, there is a bi-directional voltage-level translator used to connect 3.3V I^2C slave devices to the bus. Table below lists I^2C slave device addresses and functions:

I^2C Device	IC	I^2C Slave Address	Notes
24AA025E48	U19	0x50	Serial EEPROMs with EUI-48™ node identity.
ISL12020M	U16	0x6F	Low-power RTC with battery backed SRAM.
ISL12020M	U16	0x57	Battery backed SRAM integrated into RTC.

SI5338A	U10	0x70	Programmable quad clock generator.

Table 11: Slave devices connected to the I^2C interface.

On-board Peripherals

System Controller CPLD

The System Controller CPLD (U26) is provided by Lattice Semiconductor LCMXO2-256HC (MachXO2 product family). It is the central system management unit with module specific firmware installed to monitor and control various signals of the FPGA, on-board peripherals, I/O interfaces and module as a whole.

DDR Memory

TE0715 module has up to 1 GBytes of DDR3L SDRAM arranged into 32-bit wide memory bus. Different memory sizes are available optionally.

Quad SPI Flash Memory

On-board quad SPI Flash memory S25FL256S (U14) is used to store initial FPGA configuration. Besides FPGA configuration, remaining free flash memory can be used for user application and data storage. All four SPI data lines are connected to the FPGA allowing x1, x2 or x4 data bus widths. Maximum data rate depends on the selected bus width and clock frequency used.

> ⚠ SPI Flash QE (Quad Enable) bit must be set to high or FPGA is unable to load its configuration from flash during power-on. By default this bit is set to high at the manufacturing plant.

Gigabit Ethernet PHY

On-board Gigabit Ethernet PHY (U7) is provided with Marvell Alaska 88E1512. The Ethernet PHY RGMII interface is connected to the Zynq SoC's PS bank 501 pins MIO16 .. MIO27. Reference clock input of the PHY is supplied from the on-board 25.000000 MHz oscillator (U9), the 125MHz output clock signal CLK_125MHZ is connected to the programmable clock generator (U10) pin IN5.

High-speed USB ULPI PHY

Hi-speed USB ULPI PHY (U6) is provided with USB3320 from Microchip. The ULPI interface is connected to the Zynq SoC's PS bank 501 pins MIO28 .. 39. Reference clock input is supplied from the on-board 52.000000 MHz oscillator (U15).

MAC Address EEPROM

A Microchip 24AA025E48 EEPROM (U19) is used which contains a globally unique 48-bit node address compatible with EUI-48TM specification. The device is organized as two blocks of 128 x 8-bit memory. One of the blocks stores the 48-bit node address and is write protected, the other block is available for application use. It is accessible through the I^2C slave device address 0x50.

RTC - Real Time Clock

An temperature compensated Intersil ISL12020M is used for Real Time Clock (U16). Battery voltage must be supplied to the module from the baseboard. Battery backed registers can be accessed over I^2C bus at slave address of 0x6F. General purpose RAM is at I^2C slave address 0x57. RTC IC is supported by Linux so it can be used as *hwclock* device.

Programmable Clock Generator

There is a Silicon Labs programmable clock generator Si5338A (U10) chip on the module. It's output frequencies can be programmed via the I^2C bus, slave device address is 0x70.

U10 Signal	Default Frequency	Notes
IN1/IN2	Externally supplied	Needs decoupling on carrier board.
IN3	25.000000 MHz	Reference input clock.
IN4	-	Wired to the GND.
IN5/IN6	125 MHz	Ethernet PHY output clock.
CLK0 A/B	-	Not used, disabled.
CLK1 A/B	-	Not used, disabled.
CLK2 A/B	125 MHz	MGT reference clock 1.
CLK3A	-	Bank 34 clock input, default disabled, user clock.
CLK3B	-	Not used, disabled.

Table 12: Programmable clock generator I/Os.

Oscillators

The module has following reference clock signals provided by on-board oscillators:

Source	Signal	Frequency	Destination	Pin Name	Notes
U18	CLK	25.000000 MHz	U10	IN3	
U9	CLK	25.000000 MHz	U7	XTAL_IN	
U11	PS-CLK	33.333333 MHz	U5	PS_CLK_500	Zynq SoC PS subsystem main clock.
U15	CLK	52.000000 MHz	U6	REFCLK	USB3320C PHY reference clock.

Table 13: Reference clock signals.

On-board LEDs

LED	Color	Connected to	Description and Notes
D2	Green	DONE	Reflects inverted DONE signal. ON when FPGA is not configured, OFF as soon as PL is configured. This LED will not operate if the SC can not power on the 3.3V output rail that also powers the 3.3V circuitry on the module.
D3	Red	SC	System main status LED.
D4	Green	MIO7	User controlled, default OFF (when PS7 has not been booted).

Table 14: On-board LEDs.

Power and Power-On Sequence

TE0715-xx-30 has several HP banks on B2B connectors. Those banks have maximum voltage tolerance of 1.8V. Please check special instructions for the baseboard to be used with TE0715-xx-30.

Power Consumption

Power supply with minimum current capability of 3A for system startup is recommended. Maximum power consumption of a module mainly depends on the design running on the FPGA. Xilinx provides power estimator excel sheets to calculate power consumption. It is also possible to evaluate the power consumption of the design with Vivado. See also Trenz Electronic Wiki FAQ.

Power Input Pin	Typical Current
VIN	To be determined.
3.3VIN	To be determined.

Table 15: Typical power consumption.

Power Distribution Dependencies

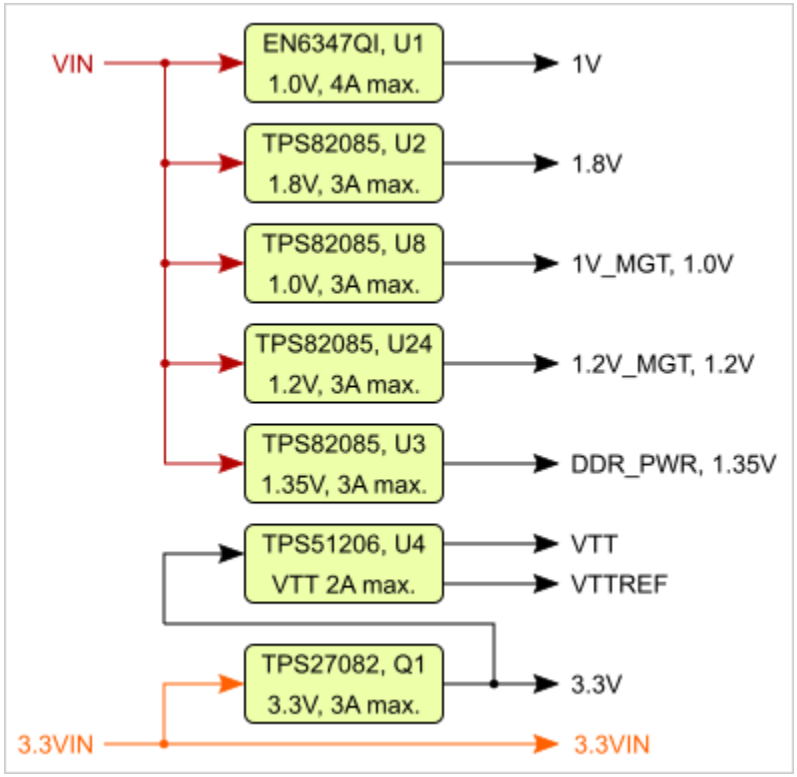


Figure 3: Module power distribution diagram.

Power-On Sequence

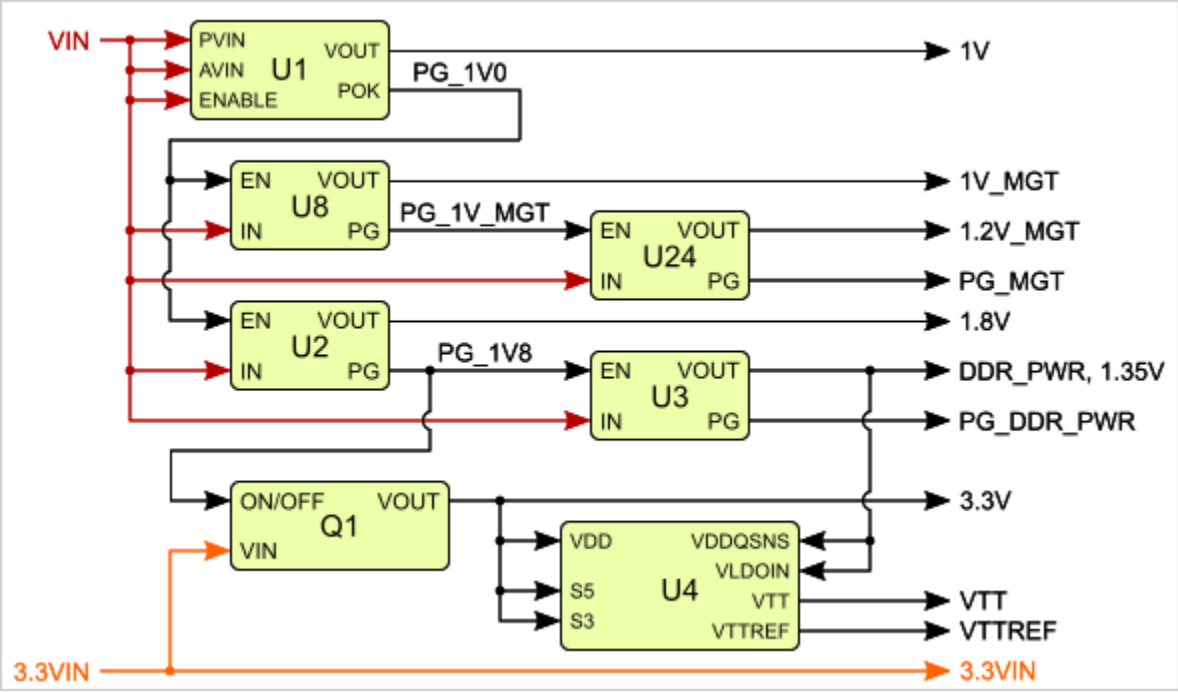


Figure 4: TE0820-02 power-on sequence diagram.

For highest efficiency of the on-board DC-DC regulators, it is recommended to use same 3.3V power source for both VIN and 3.3VIN power rails. Although VIN and 3.3VIN can be powered up in any order, it is recommended to power them up simultaneously.

> To avoid any damage to the module, check for stabilized on-board voltages should be carried out (3.3V (JM2-10, 12) or 1.8V(JM1-39) output) before powering up any FPGA's I/O bank voltages VCCO_x. All I/Os should be tri-stated during power-on sequence.

See Xilinx datasheet DS187 (for XC7Z015) or DS191 (for XC7Z030) for additional information. User should also check related baseboard documentation when choosing baseboard design for TE0715 module.

Power Rails

B2B Name	B2B JM1 Pins	B2B JM2 Pins	Direction	Note
VIN	1, 3, 5	2, 4, 6, 8	Input	Supply voltage.
3.3VIN	13, 15	-	Input	Supply voltage.
VCCIO13	9, 11	-	Input	High range bank voltage.
VCCIO34	-	5	Input	TE0715-xx-15: high range bank voltage. TE0715-xx-30: high performance bank voltage.
VCCIO35	-	7, 9	Input	TE0715-xx-15: high range bank voltage. TE0715-xx-30: high performance bank voltage.
VBAT_IN	79	-	Input	RTC battery-buffer supply voltage.
3.3V	-	10, 12	Output	Internal 3.3V voltage level.

1.8V	39	-	Output	Internal 1.8V voltage level.
DDR_PWR	-	19	Output	Internal 1.5V or 1.35V voltage level, depends on revision.
VREF_JTAG		91	Output	JTAG reference voltage (3.3V).

Table 16: TE0715 power rails.

Bank Voltages

Bank	Schematic Name	Voltage	TE0715-xx-15	TE0715-xx-30
500	VCCO_MIO0_500	3.3V	-	-
501	VCCO_MIO1_501	1.8V	-	-
502	VCCO_DDR_502	1.5V	-	-
0 Config	VCCO_0	3.3V	-	-
13 HR	VCCO_13	User	HR: 1.2V to 3.3V	HR: 1.2V to 3.3V
34 HR/HP	VCCO_34	User	HR: 1.2V to 3.3V	HP: 1.2V to 1.8V
35 HR/HP	VCCO_35	User	HR: 1.2V to 3.3V	HP: 1.2V to 1.8V

Table 17: TE0715 bank voltages.

Board to Board Connectors



These connectors are hermaphroditic. Odd pin numbers on the module are connected to even pin numbers on the baseboard and vice versa.

4 x 5 modules use two or three Samtec Razor Beam LSHM connectors on the bottom side.

- 2 x REF-189016-02 (compatible to LSHM-150-04.0-L-DV-A-S-K-TR), (100 pins, "50" per row)
- 1 x REF-189017-02 (compatible to LSHM-130-04.0-L-DV-A-S-K-TR), (60 pins, "30" per row) (depending on module)

Connector Mating height

When using the same type on baseboard, the mating height is 8mm. Other mating heights are possible by using connectors with a different height

Order number	Connector on baseboard	compatible to	Mating height
23836	REF-189016-01	LSHM-150-02.5-L-DV-A-S-K-TR	6.5 mm
	LSHM-150-03.0-L-DV-A-S-K-TR	LSHM-150-03.0-L-DV-A-S-K-TR	7.0 mm
23838	REF-189016-02	LSHM-150-04.0-L-DV-A-S-K-TR	8.0 mm
	LSHM-150-06.0-L-DV-A-S-K-TR	LSHM-150-06.0-L-DV-A-S-K-TR	10.0mm
26125	REF-189017-01	LSHM-130-02.5-L-DV-A-S-K-TR	6.5 mm
	LSHM-130-03.0-L-DV-A-S-K-TR	LSHM-130-03.0-L-DV-A-S-K-TR	7.0 mm
24903	REF-189017-02	LSHM-130-04.0-L-DV-A-S-K-TR	8.0 mm
	LSHM-130-06.0-L-DV-A-S-K-TR	LSHM-130-06.0-L-DV-A-S-K-TR	10.0mm

Connectors.

The module can be manufactured using other connectors upon request.

Connector Speed Ratings

The LSHM connector speed rating depends on the stacking height; please see the following table:

Stacking height	Speed rating
12 mm, Single-Ended	7.5 GHz / 15 Gbps
12 mm, Differential	6.5 GHz / 13 Gbps
5 mm, Single-Ended	11.5 GHz / 23 Gbps
5 mm, Differential	7.0 GHz / 14 Gbps

Speed rating.

Current Rating

Current rating of Samtec Razor Beam™ LSHM B2B connectors is 2.0A per pin (2 adjacent pins powered).

Connector Mechanical Ratings

- Shock: 100G, 6 ms Sine
- Vibration: 7.5G random, 2 hours per axis, 3 axes total

Manufacturer Documentation

File	Modified
PDF File hsc-report_lshm-lshm-05mm_web.pdf High speed test report	07 04, 2016 by Thorsten Trenz
PDF File lshm_dv.pdf LSHM catalog page	07 04, 2016 by Thorsten Trenz
PDF File LSHM-1XX-XX.X-X-DV-A-X-X-TR-FOOTPRINT(1).pdf Recommended layout and stencil drawing	07 04, 2016 by Thorsten Trenz
PDF File LSHM-1XX-XX.X-XX-DV-A-X-X-TR-MKT.pdf Technical drawing	07 04, 2016 by Thorsten Trenz
PDF File REF-189016-01.pdf Technical Drawing	07 04, 2016 by Thorsten Trenz
PDF File REF-189016-02.pdf Technical Drawing	07 04, 2016 by Thorsten Trenz
PDF File REF-189017-01.pdf Technical Drawing	07 04, 2016 by Thorsten Trenz
PDF File REF-189017-02.pdf Technical Drawing	07 04, 2016 by Thorsten Trenz
PDF File TC0923--2523_report_Rev_2_qua.pdf Design qualification test report	07 04, 2016 by Thorsten Trenz
PDF File tc0929--2611_qua(1).pdf Shock and vibration report	07 04, 2016 by Thorsten Trenz

Download All

Variants Currently in Production

Trenz shop TE0715 overview page	
English page	German page

Table 18: TE0715 variants currently in production.

Technical Specifications

Absolute Maximum Ratings

Parameter	Min	Max	Units	Notes
VIN supply voltage	-0.3	6.0	V	-
3.3VIN supply voltage	-0.4	3.6	V	-
VBAT supply voltage	-1	6.0	V	-
PL IO bank supply voltage for HR I/O banks (VCCO)	-0.5	3.6	V	-
PL IO bank supply voltage for HP I/O banks (VCCO)	-0.5	2.0	V	TE0715-xx-15 does not have HP banks.
I/O input voltage for HR I/O banks	-0.4	VCCO + 0.55	V	-
I/O input voltage for HP I/O banks	-0.55	VCCO + 0.55	V	TE0715-xx-15 does not have HP banks.
GT receiver (RXP/RXN) and transmitter (TXP/TXN)	-0.5	1.26	V	-
Voltage on module JTAG pins	-0.4	VCCO_0 + 0.55	V	VCCO_0 is 3.3V nominal.
Storage temperature	-40	+85	°C	-
Storage temperature without the ISL12020MIRZ and 88E1512	-55	+100	°C	-

Table 19: TE0715 module absolute maximum ratings.

⚠ Assembly variants for higher storage temperature range are available on request.

⚠ Please check Xilinx datasheet DS187 (for XC7Z015) or DS191 (for XC7Z030) for complete list of absolute maximum and recommended operating ratings.

Recommended Operating Conditions

Parameter	Min	Max	Units	Notes	Reference Document
VIN supply voltage	2.5	5.5	V		
3.3VIN supply voltage	3.135	3.465	V		
VBAT_IN supply voltage	2.7	5.5	V		
PL I/O bank supply voltage for HR I/O banks (VCCO)	1.14	3.465	V		Xilinx datasheet DS191
PL I/O bank supply voltage for HP I/O banks (VCCO)	1.14	1.89	V	TE0715-xx-15 does not have HP banks	Xilinx datasheet DS191

I/O input voltage for HR I/O banks	(*)	(*)	V	(*) Check datasheet	Xilinx datasheet DS191 or DS187
I/O input voltage for HP I/O banks	(*)	(*)	V	TE0715-xx-15 does not have HP banks (*) Check datasheet	Xilinx datasheet DS191
Voltage on Module JTAG pins	3.135	3.465	V	VCCO_0 is 3.3 V nominal	

Table 20: TE0715 module recommended operating conditions.

Operating Temperature Ranges

Commercial grade: 0°C to +70°C.

Industrial and extended grade: -40°C to +85°C.

The module operating temperature range depends also on customer design and cooling solution. Please contact us for options.

Physical Dimensions

- Module size: 50 mm × 40 mm. Please download the assembly diagram for exact numbers
- Mating height with standard connectors: 8mm
- PCB thickness: 1.6mm
- Highest part on PCB: approx. 2.5mm. Please download the step model for exact numbers

All dimensions are given in millimeters.

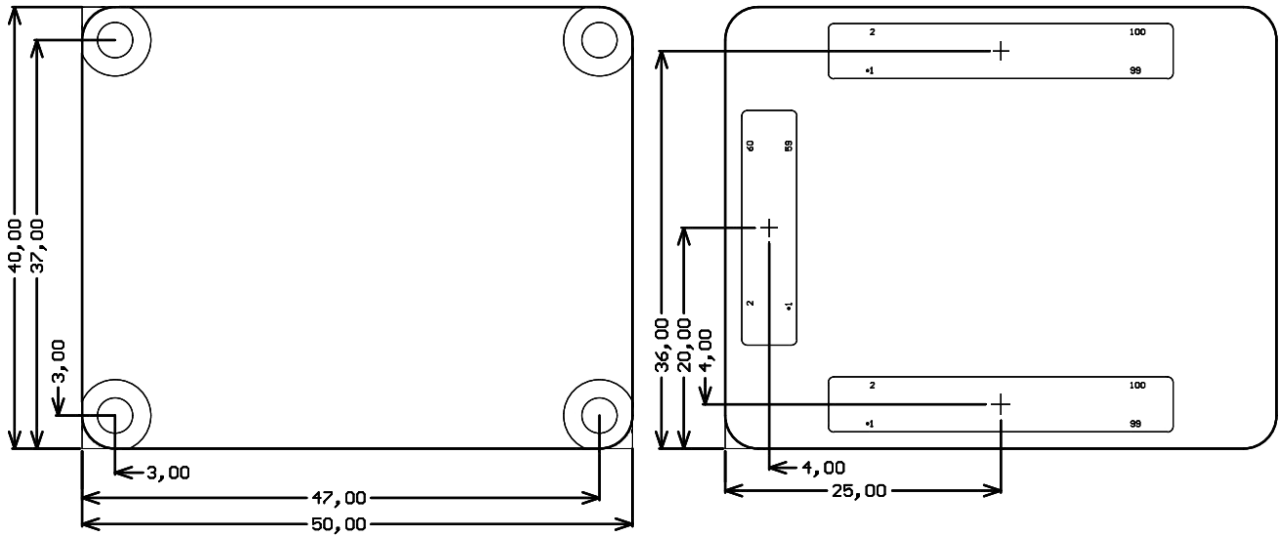


Figure 5: TE0715 physical dimensions.

Revision History

Hardware Revision History

Date	Revision	Notes	Link to PCN	Documentation Link
2022-12-21	05	Third production release	Click to see PCN	TE0715-05
2016-06-21	04	Second production release	Click to see PCN	TE0715-04
-	03	First production release		TE0715-03
-	02	Prototypes		TE0715-02
-	01	Prototypes		

Table 21: TE0715 module hardware revision history.

Hardware revision number is printed on the PCB board together with the module model number separated by the dash.

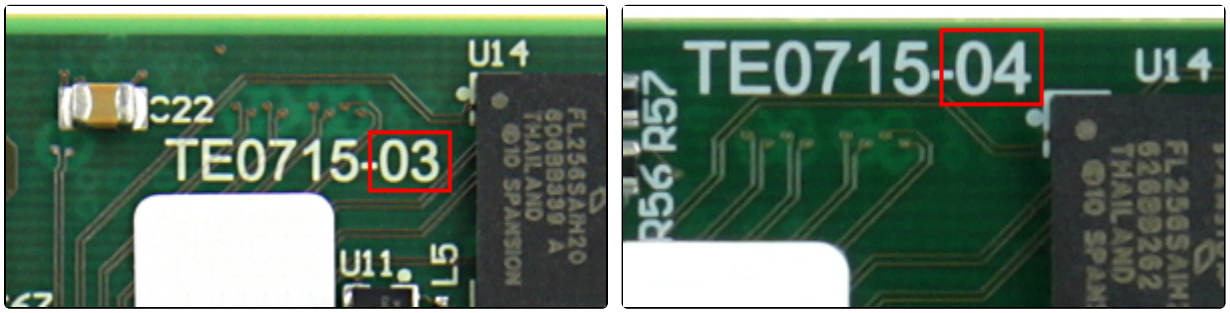


Figure 6: TE0715 hardware revision number.

Document Change History

Date	Revision	Contributors	Description

Error rendering macro 'page-info' Ambiguous method overloading for method jdk.proxy244.$Proxy3572#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy244.$Proxy3572#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy244.$Proxy3572#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	• Updated Key features: DCDC current rating • Added revision 5 in Hardware revision history
2021-06-21	v.87	John Hartfiel	• Bugfix Link to PDF download
2018-07-06	v.86	John Hartfiel	• Link to shop production list • Change normal Bank power note to important note

2017-11-14	v.85	John Hartfiel	• Replace B2B connector section
2017-09-10	v.82	Jan Kumann	• Document template revision added. • Revised block diagram with new I^2C part. • Power distribution diagram added. • Power-on sequence diagram added. • Sections rearranged, some missing ones added. • Weight section removed.
2017-06-07	v.64	Jan Kumann	• Minor formatting.
2017-03-02	v.59	Thorsten Trenz	• Corrected boot mode table.
2017-02-10	v.58	Thorsten Trenz	• Corrected PLL initial delivery state.
2017-01-25	v.55	Jan Kumann	• New block diagram.

2017-01-14	v.50	Jan Kumann	• Product revision 04 images added. • Formatting changes and small corrections.
2016-11-15	v.45	Thorsten Trenz	• Added B2B Connector section.
2016-10-18	v.40	Ali Naseri	• Added table "power rails".

2016-06-28	v.38	Thorsten Trenz, Emmanuel Vassilakis, Jan Kumann	• New overall document layout with shorter table of contents. • Revision 01 PCB pictures replaced with the revision 03 ones. • Fixed link to Master Pin-out Table. • New default MIO mapping table design. • Revised Power-on section. • Added links to related Xilinx online documents. • Physical dimensions pictures revised. • Revision number picture with explanation added.
2016-04-27	v.33	Thorsten Trenz, Emmanuel Vassilakis	• Added table "Recommended Operating Conditions". • Storage Temperature edited.
2016-03-31	v.10	Philipp Bernhardt, Antti Lukats	• Initial version.

Table 22: Document change history.

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