TEI0003 Test Board

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1.1 Key Features

Nios V/m designlexample:owithisDR/AM controller (AXI4), 3-axis Accelerometer and different LED sequences. O 1.3 Release Notes and Know Issues

• 1.4 Requirements

Refer to http://trenz.org/ct/v4.008oin/vafor the current online version of this manual and other available documentation.

1.4.2 Hardware

o 1.5 Content

■ 1.5.1 Design Sources

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 Quartus Prime Lite 22.1std
 Nios Vim Programming
 Spi 3.1 Programming

SPI = 3.1.1 Get prebuilt boot binaries

UART = 3.1.2 Configuration Flash

SDRAM controller (AXIA)

Source code: https://github.com/ultraembedded/core_sdram_axi4

3-axis Acceleronseter UART

Set by Stern Design - Quartus

User by Ittps:

Software Design - SDK

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• 6 Appx. A: Cl	nange History and Leg	al Notices		
Date 0 6.1	Doc omատմ S hange His		Authors	Description
2023-09-13	Legal Notices Do22.Ptitecy Document Warranty Limitation of Liability Copyright Notice Technology Licenses Environmental Protecti REACH, RoHS and W Intents	TEI0003- test_board_noprebui lt-quartus_22.1std.2- 20230913161158.zip TEI0003-test_board- of_uartus_22.1std.2- 20230913161214.zip	Thomas Dück	update to Quartus Prime Lite 22.1 new board variants change to Nios V/m TE scripts update
2022-04-21	21.1 Lite	TEI0003- test_board_noprebui lt-quartus_21.1.0- 20220421150041.zip TEI0003-test_board- quartus_21.1.0- 20220421150114.zip	Thomas Dück	update to Quartus Prime Lite 21.1
2021-07-09	20.1 Lite	TEI0003- test_board_noprebui It-quartus_20.1.1- 20210709110930.zip TEI0003-test_board- quartus_20.1.1- 20210709110847.zip	Thomas Dück	update to Quartus Prime Lite 20.1 TE scripts update

2020-10-19	19.1 Lite	TEI0003- test_board_noprebui It-quartus_19.1.0- 20201019101802.zip TEI0003-test_board- quartus_19.1.0- 20201019101738.zip	Thomas Dück	script updatebugfixes
2020-05-13	19.1 Lite	TEI0003- test_board_noprebui It-quartus_19.1.0- 20200513080815.zip TEI0003-test_board- quartus_19.1.0- 20200513081030.zip	Thomas Dück	• 19.1 update
2019-11-11	18.1	TEI0003- test_board_noprebui It-quartus_18.1- 20191111104152.zip TEI0003-test_board- quartus_18.1- 20191111104339.zip	Thomas Dück	add bash files for Linux OS
2019-10-29	18.1	TEI0003- test_board_noprebui It-quartus_18.1- 20191029121432.zip TEI0003-test_board- quartus_18.1- 20191029121225.zip	Thomas Dück	create project with TE scripts new board variants
2019-04-02	18.1	TEI0003-02- test_board- quartus_18.1- 20190402.zip	Thomas Dück	• initial release

Design Revision History

Release Notes and Know Issues

Issues	Description	Workaround	To be fixed version
No known issues			

Known Issues

Requirements

Software

Software	Version	Note
Quartus Prime Lite	22.1std	Nios V license is needed. For more information see: Intel Nios V Processors
RiscFree IDE for Intel FPGAs	22.1std	needed

Software

Hardware

Complete List is available on ct folder>/board_files/*_devices.csv

Design supports following modules:

Module Model	PCB Revision Support	Board Part Short Name	SDRAM	Configuration	n fl Øsh ers	Notes
TEI0003-02	REV01, REV02	QFCR1	8MByte	2MByte		
TEI0003-02A	REV2	QFCR1	8MByte	2MByte		
TEI0003-03A- S001	REV03	QFCR4_S1	8MByte	8MByte		
TEI0003-03- QFCR1A	REV03	QFCR1	8MByte	2MByte		
TEI0003-03- QFCR4A*	REV03	QFCR4	8MByte	8MByte		

^{*}used as reference

Hardware Modules

Design supports following carriers:

Carrier Model	Notes

^{*}used as reference

Hardware Carrier

Additional HW Requirements:

Additional Hardware	Notes
Micro USB cable for JTAG/UART	

^{*}used as reference

Additional Hardware

Content

For general structure and of the reference design, see Project Delivery - Intel devices

Design Sources

Туре	Location	Notes
Quartus	<pre><pre><pre><pre><pre><pre><pre>/quartus/</pre></pre></pre></pre></pre></pre></pre>	Quartus project will be generated by TE Scripts
Software	<pre><pre><pre><pre><pre><pre><pre>/software/</pre></pre></pre></pre></pre></pre></pre>	Additional software will be generated by TE Scripts

Design sources

Prebuilt

File	File-Extension	Description
SOPC Information File	*.sopcinfo	File with description of the *. qsys file to create software for the target hardware
SRAM Object File	*.sof	Ram configuration file
JTAG indirect configuration file	*.jic	Flash configuration file
Diverse Reports		Report files in different formats
Software Application File	*.elf	Software application for Nios V processor system

Prebuilt files (only in ZIP file with prebuilt content)

Download

Reference Design is only usable with the specified Quartus version. Do never use different versions of Quartus software for the same project.

Reference Design is available on:

• TEI0003 "Test Board" Reference Design

Design Flow



Reference Design is available with and without prebuilt files. It's recommended to use TE prebuilt files for first launch.

Trenz Electronic provides a tcl based built environment based on Quartus Design Flow.

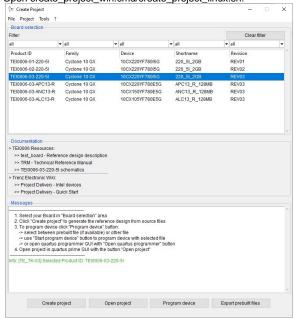
See also:

• Project Delivery - Intel devices

The Trenz Electronic FPGA Reference Designs are TCL-script based projects. To create a project, open a project or program a device execute "create_project_win.cmd" on Windows OS and "create_project_linux.sh" on Linux OS.

TE Scripts are only needed to generate the quartus project, all other additional steps are optional and can also executed by Intel Quartus/SDK GUI. For currently Scripts limitations on Win OS and Linux OS see: Project Delivery - Intel devices Currently limitations of functionality

1. Open create_project_win.cmd/create_project_linux.sh:



- 2. Select Board in "Board selection"
- 3. Click on "Create project" button to create project
 - a. (optional for manual changes) Select correct quartus installation path in "project folder>/settings/design_basic_settings.tcl"

Launch

Programming



Check Module and Carrier TRMs for proper HW configuration before you try any design.

Get prebuilt boot binaries



Reference Design is also available with prebuilt files. It's recommended to use TE prebuilt files for first launch.

- 1. Run create_project_win.cmd/create_project_linux.sh
- 2. Select Module in 'Board selection'
- 3. Click on 'Export prebuilt files' button
 - a. Folder <project folder>/_binaries_<Article Name> with subfolder programming_files will be generated and opened

Configuration Flash

- 1. Connect the Module to USB-Port
- 2. Open create_project_win.cmd/create_project_linux.sh
- 3. Select correct board in "Board selection"
- 4. Click on "Program device" button
 - a. if prebuilt files are available: select "Program prebuilt file"

- b. using own generated programming file: select "Program other file" and click on "Browse ..." to open own generated programming file
- c. (optional) click on "Open programmer GUI" to program device with Quartus programmer GUI
- 5. Click on "Start program device" button

JTAG

Not used on this example.

Usage

- 1. Prepare Hardware like described on section Programming
- 2. Connect UART USB (most cases same as JTAG)

UART

- 1. Open Serial Console (e.g. PuTTY)
 - a. select COM Port
 - **①**

Win OS: see device manager

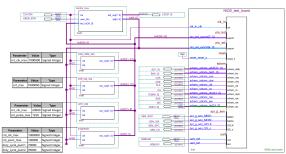
Linux OS: see Is -I dev/serial/by-id (UART is *USB1)

- b. Speed: 115200
- 2. Press reset button
- 3. Console output depends on used Software project, see Software Design SDK#Application

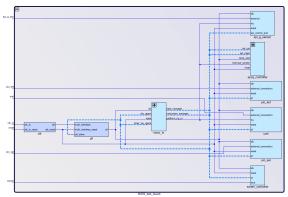
System Design - Quartus

Block Design

The block designs may differ depending on the assembly variant.



Block Design - Project



Block Design - NIOS_test_board.qsys

Block Design - Platform Designer

Software Design - SDK

Application

Used software project depends on board assembly variant. Template location: cyroject folder>/source_files/software/

test_tei0003

Software example to test TEI0003 module.

- You can select between following modes by pressing the user button:
 - 1. Spirit level
 - 2. Case statement sequence
 - 3. Shift register sequence
 - 4. Knightrider sequence
 - Pulse-width modulation sequence

hello tei0003

Software example with 'Hello TEI0003' console output in endless loop.

Appx. A: Change History and Legal Notices

Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

Date	Document Revision	Authors	Description
			 update to Quartus Prime Lite 22.1 document style update

Error	Error	Error
renderi	renderi	renderi
ng	ng	ng
macro	macro	macro
'page-	'page-	'page-
info'	info'	info'
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rmission	rmission	rmission
Cannot	Cannot	Cannot
resolve	resolve	resolve
which	which	which
method	method	method
to	to	to
invoke	invoke	invoke
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class	class	class
java.	java.	java.
lang.	lang.	lang.
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2022-04-22	v.9	Thomas Dück	update to Quartus Prime Lite 21.1
2021-07-09	v.8	Thomas Dück	update to Quartus Prime Lite 20.1 document style update script update
2020-10-09	v.7	Thomas Dück	script update bugfixes
2020-05-13	v.6	Thomas Dück	• 19.1 release
2019-11-11	v.5	Thomas Dück	add bash files for Linux OS
2019-10-29	v.3	Thomas Dück	change design to TE scripts new board variants
2019-04-03	v.2	Thomas Dück	Initial release 18.1
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overload ing for method jdk. proxy27 9.\$Proxy 4022#ha sConten tLevelPe rmission Cannot resolve which method to invoke for [null, class java. lang. String, class com. atlassian confluen ce. pages. Page] due to overlapp ing prototyp es between

[interfac e com.

atlassian confluen ce.user. Conflue nceUser , class java. lang. String, class com. atlassian confluen ce.core. Content EntityOb ject] [interfac e com. atlassian .user. User, class java. lang. String, class com. atlassian confluen ce.core. Content EntityOb ject]

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Error rendering macro 'page-info'

proxy279.\$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user. ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.

ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]