TEB2000 Getting Started

TEB2000 with TEM0007

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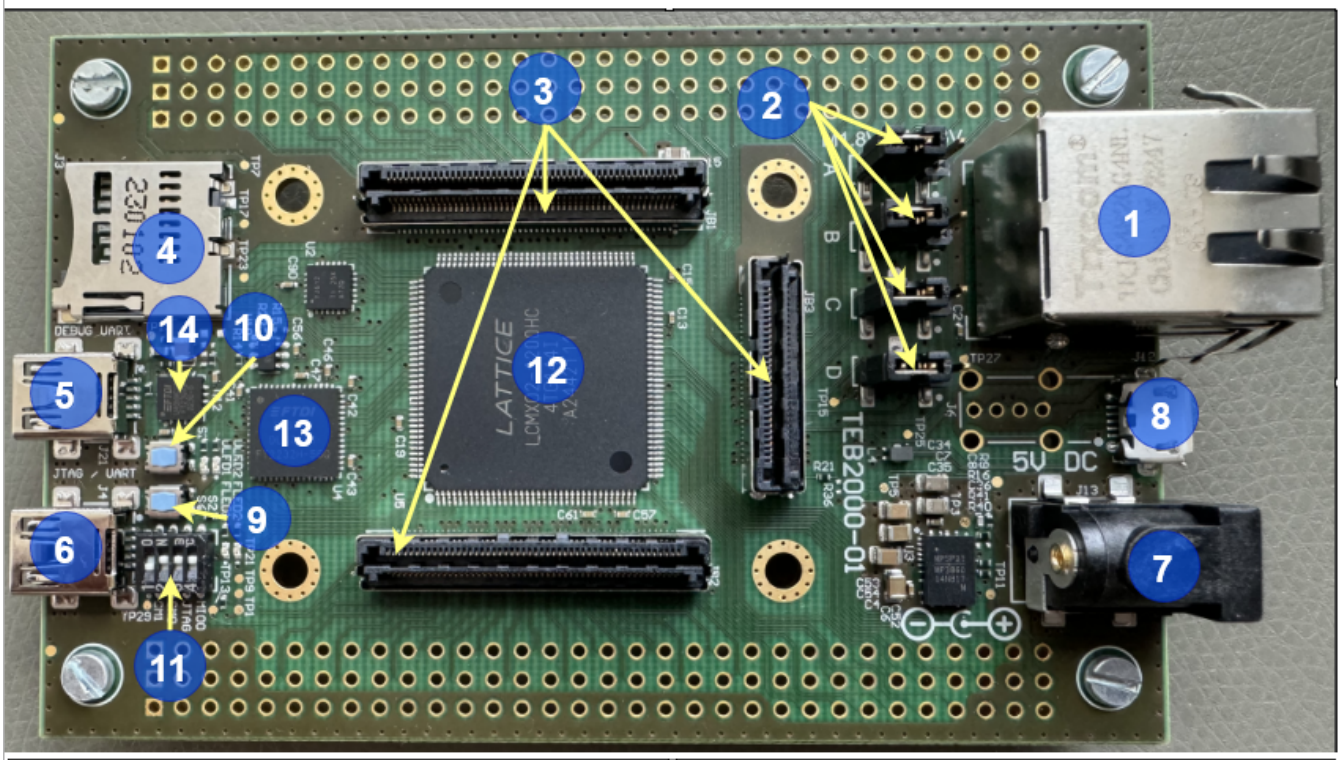
Overview

TEB2000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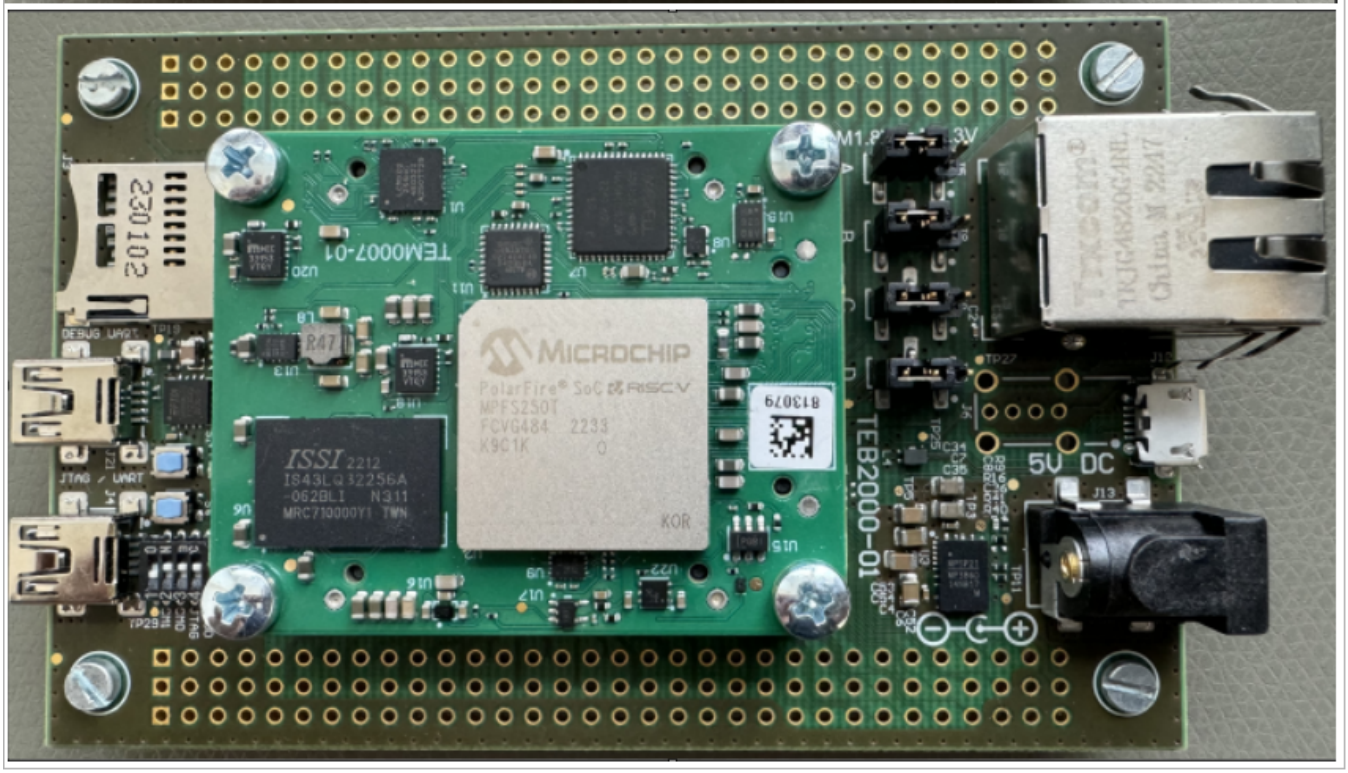
5V DC
DEBUG UART
JTAG / UART


MICROCHIP
ISSI
TEM0007-01
TEB2000-01
5V DC
DEBUG UART
JTAG / UART

Board Overview

Board Overview

Number	Note
1	J14- Ethernet interface
2	J5,J8,J9,J10- Bank voltage adjustment
3	JB1,JB2,JB3- B2B connector
4	J3- SD card socket
5	J21- UART0 socket
6	J4- UART1 socket
7	J13- 5V voltage input
8	J12- USB stick socket
9	S6- Reset button (SRST) (Soft reset)
10	S1- Reset button
11	S2- Dip Switch
12	U5- CPLD Chip
13	U4- FTDI chip for UART1 interface (Linux console)
14	U12- FTDI chip for UART0 interface (HSS console)

Power supply

Single 5V power supply with minimum current capability of 1.5A is recommended to power on the board.

DIP-Switches and Push Buttons

There is two reset switchs on the board (S1 and S6). The S6 is a soft reset button (SRST) that is not directed to CPLD chip. The S1 signal is connected to CPLD chip and is used in firmware code to create a reset signal.

Signal	Designator	Connected to	Active Level	Description
SRST	S6	B2B JB2 pin 56	Active low	
S1	S1	CPLD chip pin 114	Active low	

Dip Switch S2	Signal	Position ON	Position OFF	Connected to	Description
S2-1	MIO0	MODE pin (B2B JB1 pin 31 set to '0')	MODE pin (B2B JB1 pin 31 set to '1')	CPLD chip pin 94 / B2B JB1 pin 88	
S2-2	JTAGEN	Module FPGA JTAG access (if S2-3 ON)	Module CPLD JTAG access (if S2-3 ON)	CPLD chip pin 120	

S2-3	CM0	Module FPGA /CPLD JTAG access (depends on S2-3)	Carrier CPLD JTAG access	CPLD chip pin 76	
S2-4	CM1	PGOOD signal set to '0'	PGOOD signal set to '1'	CPLD chip pin 75	

DIP Switches /Push Buttons

There is no DIP switch on the TEM0007 module.

Jumpers

Designator	Connected to	Default set to	Note
J5	VCCIOA	M1.8VOUT	It can be set to both 1.8V or 3.3V for TEM0007 module.
J8	VCCIOB	M1.8VOUT	May be set to either 3.3V or 1.8V. If set to 1.8V --> VDDAUX1 (TP5) = 2.5V±3%
J9	VCCIOC	M1.8VOUT	It can be set to both 1.8V or 3.3V for TEM0007 module.
J10	VCCIOD	M1.8VOUT	Important note: Only set to 1.8V for TEM0007 module.

Jumpers

I2C to GPIO

Such signals same as NOSEQ can be read or written via i2c commands in linux console. For more information about it refer to TEB2000 CPLD#I2C to GPIO

LEDs

There are six LEDs which can be used for variant purposes.

LED	Designator	LED Status	Condition	Description
ULED1 (Red)	D1	Fast blink red	Access to CPLD of module (CM0 = '1') S2-2 = OFF	
		Connected to UART1_RX	Otherwise	
ULED2 (Green)	D2	Fast blink green	Access to CPLD of module (CM0 = '1') S2-2 = OFF	
		Connected to UART1_TX	Otherwise	
FLED_1 (Red)	D3	Fast blink red	PGOOD = '1' (CM1 = '0') S2-1 = ON	
		Connected to UART0_RX	Otherwise	
FLED_2 (Green)	D4	Fast blink green	PGOOD = '1' (CM1 = '0') S2-1 = ON	
		Connected to UART0_TX	Otherwise	

LED	Designator	LED Status	Condition	Description

PHY_LED1 (Green LED Anode, Yellow LED Cathode) / **PHY_LED1R (Green LED Cathode, Yellow LED Anode)**	J14B*	Fast blink yellow	NOSEQ = '0' and MIO0 = '0'	`In Linux console enter: i2cset -y 0 0x20 0x02 0x00 and S2-4 = ON*`
		Slow blink yellow	NOSEQ = '0' and MIO0 = '1'	`In Linux console enter: i2cset -y 0 0x20 0x02 0x00 and S2-4 = OFF*`
		Fast blink yellow green	NOSEQ = '1' and MIO0 = '0'	`In Linux console enter: i2cset -y 0 0x20 0x02 0x01 and S2-4 = ON*`
		Slow blink yellow gr een	NOSEQ = '1' and MIO0 = '1'	`In Linux console enter: i2cset -y 0 0x20 0x02 0x01 and S2-4 = OFF*`
PHY_LED2 (Green LED Cathode, Yellow LED Anode) / **PHY_LED2R (Green LED Anode, Yellow LED Cathode)**	J14C*	ON	SD card plugged (SD_CD = '0')	
		OFF	Otherwise	

* This LEDs exit on the ethernet socket (J14A).

Carrier LEDs

Note: The TEM0007 module has no LED.

JTAG/UART

JTAG and UART connections are available through micro USB connector. MIO14 is driven by BDBUS0 (FTDI RX). BDBUS1 (FTDI TX) is driven by MIO15 . MIO13 is driven by UART_TXD. UART_RXD is driven by MIO12.

UART 0 (HSS Console)						
Designator J21						
CPLD UART Input Pin	**CPLD Pin**	**Connected to**	**CPLD UART Output Pin**	**CPLD Pin**	**Connected to**	**Description**
MIO12	100	B2B-JB1-100	**UART_RXD**	84	U8-Pin 11	
UART_TXD	77	U8-Pin 13	**MIO13**	99	B2B-JB1-98	

UART 1 (Linux Console)
Designator J4

CPLD UART Input Pin	CPLD Pin	Connected to	CPLD UART Output Pin	CPLD Pin	Connected to	Description
FT_B_TX	139	FTDI Chip U4 Pin 32	**MIO14**	105	B2B-JB1-91	
MIO15	95	B2B-JB1-86	**FT_B_RX**	138	FTDI Chip U4 Pin 33	

UART

For more information refer to TEB2000 CPLD#UART

Reference Designs

- TEM0007 Reference Designs

Notes

- TEB2000 CPLD
- TEM0007 Resources