TE0726 TRM

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Overview

The Trenz Electronic TE0726 is an industrial/extended grade module based on AMD Zynq 7 Series. It is Raspberry Pi form factor compatible.

Refer to http://trenz.org/te0726-info for the latest online version of this manual and other available documentation.

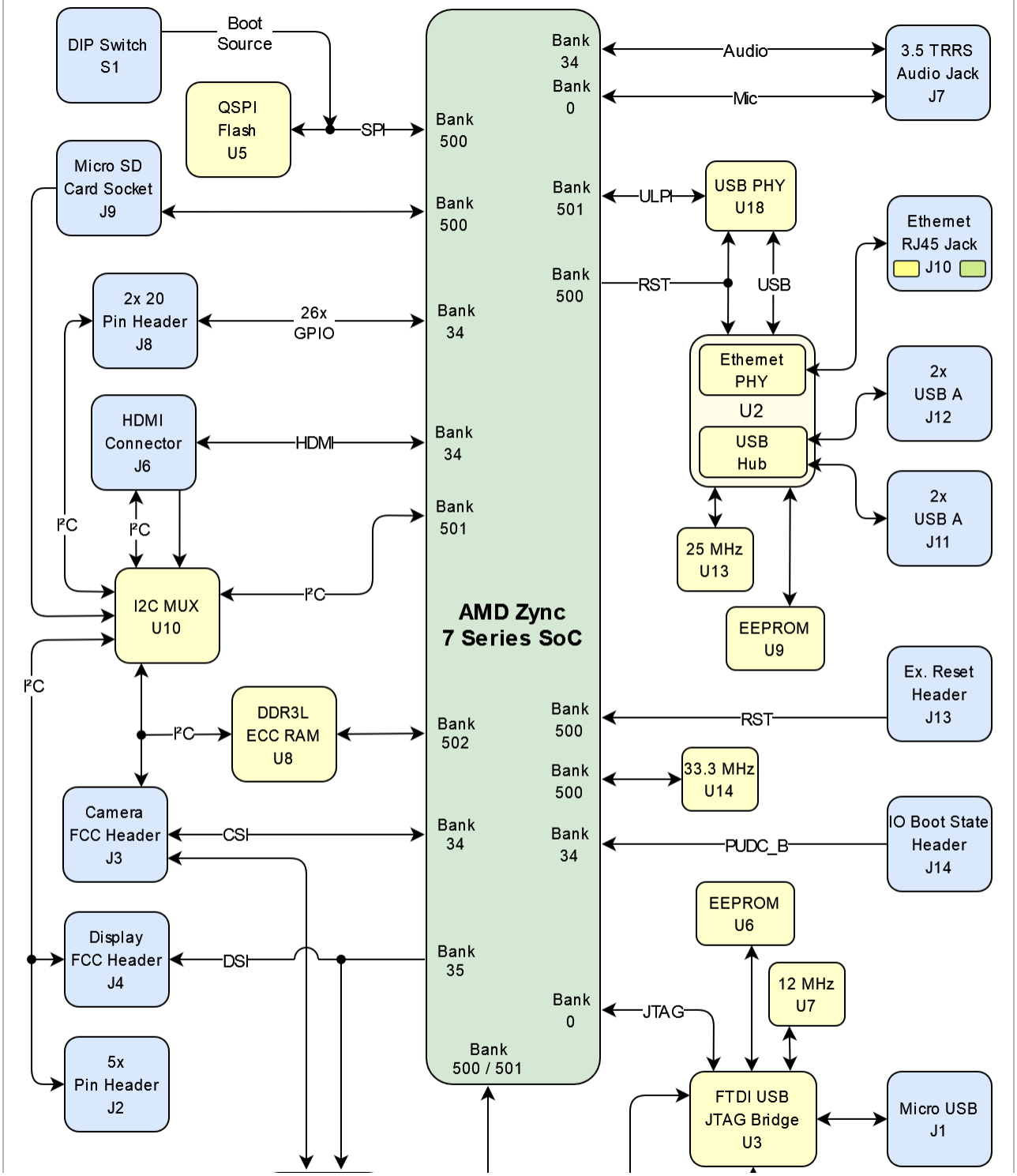
Key Features

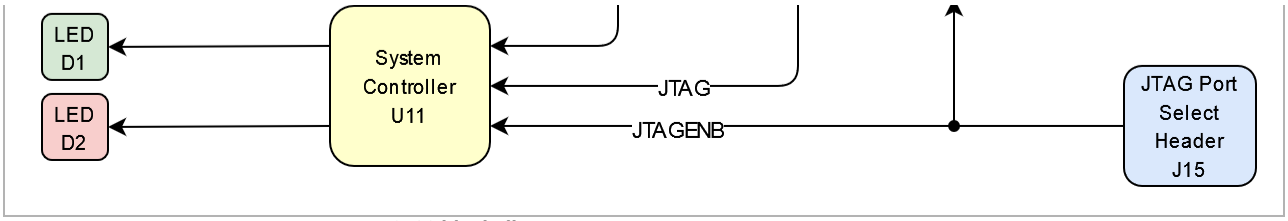
- **SoC/FPGA/Module**
  - Package: CLG225
  - Device: Z-7007S, Z-7010, [1]
  - Temperature ranges: Commercial / Extended / Industrial [1]
  - Speed grades: -3, -2, -1 [1]
- **RAM/Storage**
  - 512 MByte DDR3L ECC RAM [1]
  - 16 MByte QSPI Flash
  - 2 KBit EEPROM for FTDI
  - 2 KBit EEPROM for Ethernet & USB HUB
- **On Board**
  - System Controller CPLD
  - USB OLP Transceiver
  - 10/100 Ethernet Transceiver with USB hub
  - USB to JTAG / UART FTDI
- **Interface**
  - 1x Micro USB (UART/JTAG)
  - 4x USB 2.0
  - 1x microSD Card socket
  - 1x Boot Select DIP Switch
  - 1x Ethernet RJ45 socket
  - 1x TRRS Audio Jack 3.5mm with microphone (PWM audio only)
  - 1x HDMI Connector
  - 1x CSI-2 Connector (Camera Serial Interface)
  - 1x DSI Connector (Display Serial Interface)
  - 1x8 Pin Header for I²C
  - 2x20 Pin Header with 26 GPIO, 1x I²C , 5 and 3.3 V
  - 3 additional Pinheaders for CPLD access, Reset and PUDC (SoC Boot IO State) changes
- **Power**
  - via Micro USB
  - via 5V Pin header
- **Dimension**
  - 56 mm x 85 mm, like Raspberry Pi
- **Notes**

[1] Depends on assembly variant

Block Diagram

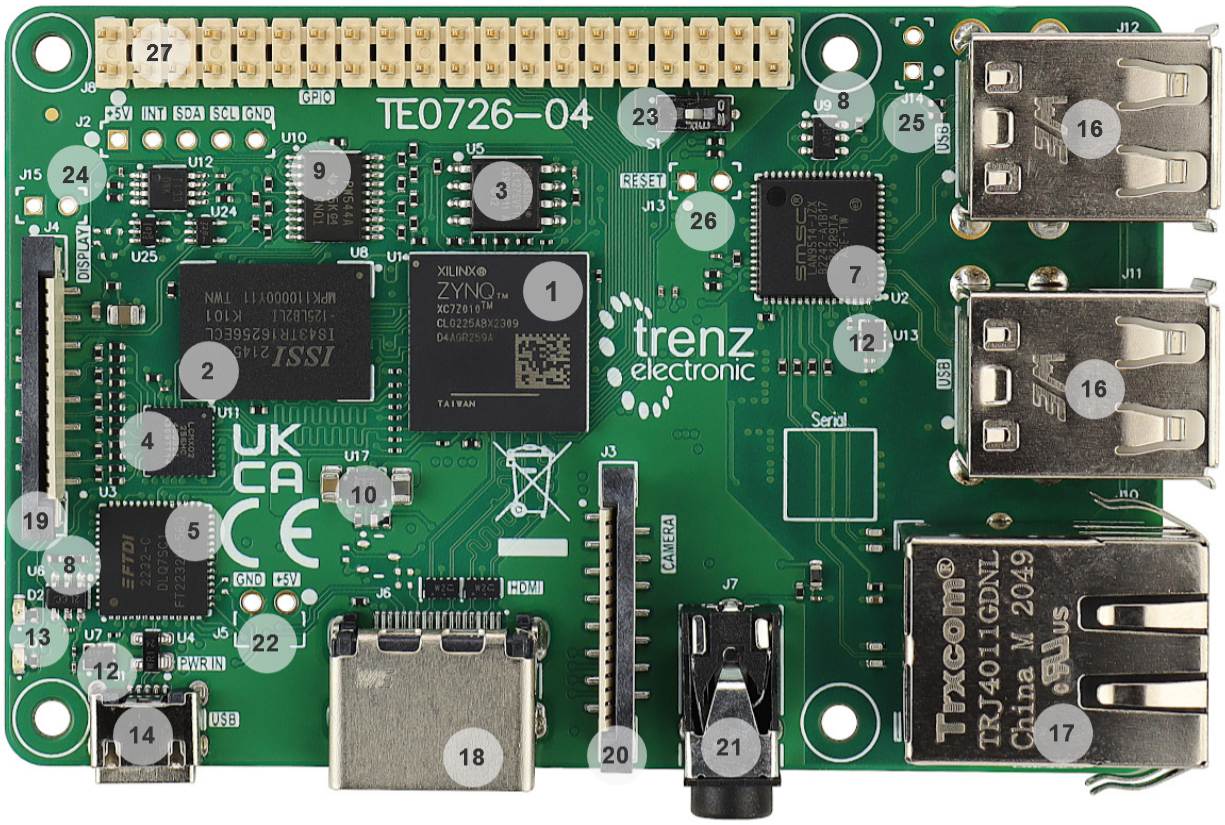
TE0726

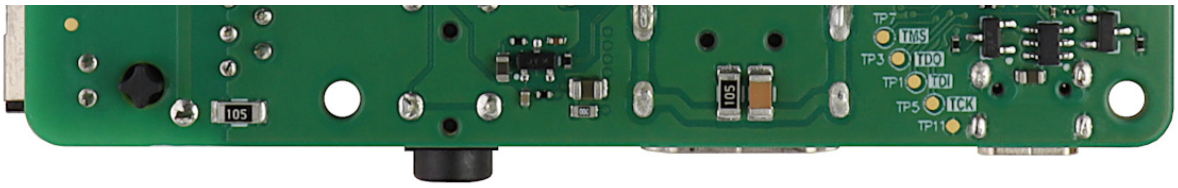

DIP Switch S1
Boot Source
QSPI Flash U5
SPI
Micro SD Card Socket J9
2x 20 Pin Header J8
26x GPIO
HDMI Connector J6
HDMI
I²C
I2C MUX U10
DDR3L ECC RAM U8
Camera FCC Header J3
CSI
Display FCC Header J4
DSI
5x Pin Header J2
AMD Zync 7 Series SoC
Bank 34
Bank 0
Bank 500
Bank 501
Bank 500
Bank 34
Bank 34
Bank 501
Bank 502
Bank 500
Bank 500
Bank 34
Bank 34
Bank 35
Bank 0
Bank 500 / 501
Audio
Mic
3.5 TRRS Audio Jack J7
ULPI
USB PHY U18
RST
USB
Ethernet RJ45 Jack J10
Ethernet PHY
U2
USB Hub
2x USB A J12
2x USB A J11
25 MHz U13
EEPROM U9
RST
Ex. Reset Header J13
33.3 MHz U14
PUDC_B
IO Boot State Header J14
EEPROM U6
12 MHz U7
JTAG
FTDI USB JTAG Bridge U3
Micro USB J1



TE0726 block diagram

Main Components


TE0726-04
trenz electronic
ZYNQ
XILINX
ISSI
Trxcom
TRJ4011GDNL
China M 2049
GPIO
DISPLAY
CAMERA
HDMI
USB
RESET
Serial
PWRIN
MICRO SD CARD
Trenz Electronic GmbH
Beendorfer Str. 23
32609 Huellhorst
Germany



TE0726 main components

1. AMD 7 Series Zynq, U1
2. DDR3L ECC RAM, U8
3. SPI Flash, U5
4. System Controller CPLD, U11
5. FTDI USB to multipurpose JTAG/FIFO, U3
6. USB Transceiver, U18
7. Ethernet Transceiver LAN9514 with 4 port USB Hub , U2
8. EEPROM, U6 , U9
9. I^2C Multiplexer, U10
10. Power Supply, U16, U17, U19, U20
11. USB power switch, U15 , U21
12. Oscillator, U14 , U13 , U7
13. LED, D1 , D2
14. Micro USB B receptacle, J1
15. microSD card, J9
16. 2x USB A, J11 , J12
17. RJ-45 Ethernet connector, J10
18. HDMI connector, J6
19. DSI LCD connector, J4
20. CSI camera connector, J3
21. 3.5mm RCA audio jack, J7
22. +5V Power Connector, J5
23. Boot DIP switch, S1
24. JTAG Port select header, J15
25. Boot IO State select header, J14
26. Externer reset header, J13
27. 2x20 pin header, J8

Initial Delivery State

Storage device name	Content	Notes
Quad SPI Flash	not programmed	
EEPROM FTDI	preprogrammed	
EEPROM ETH	not programmed	
System Controller CPLD	preprogrammed	

Initial delivery state of programmable devices on the module

Signals, Interfaces and Pins

Connectors

Connector Type	Designator	Interface	IO CNT	Notes
2x 20 2.54 mm Pin Header	J8	GPIO (HR)	26	

2x 20 2.54 mm Pin Header	J8	I²C	2	Multiplexer U10
2x 2.54 mm Pin Header	J15	JTAG select	1	SoC or SC select
2x 2.54 mm Pin Header	J14	Boot IO State select	1	
2x 2.54 mm Pin Header	J13	External reset	1	
2x USB A stacked	J11, J12	USB 2.0	12	To USB PHY (ULPI)
5x 2.54 mm Pin Header	J2	I²C	2	Multiplexer U10, I²C shared with J4
5x 2.54 mm Pin Header	J2	Interrupt	1	Multiplexer U10
DIP switch	S1	Boot select	1	Shared with SPI
FCC	J4	MIPI DSI	6 (3 pairs)	
FCC	J4	I²C	2	Multiplexer U10
FCC	J3	I²C	2	Multiplexer U10
FCC	J3	MIPI CSI-2	8 (4 pairs)	
HDMI	J6	HDMI	8 (4 pairs)	
HDMI	J6	I²C	2	Multiplexer U10
HDMI	J6	Interrupt	1	Multiplexer U10
Micro-USB 2.0 B	J1	JTAG	2 (1 pair)	SoC or SC selectable
microSD Card	J9	Interrupt	1	Multiplexer U10
microSD Card	J9	SD	5	
RJ-45 Ethernet	J10	10/100 ETH	12	To USB PHY (ULPI)
TRRS 3.5 mm	J7	RCA Audio	2	
TRRS 3.5 mm	J7	RCA Mic	1	

Board Connectors

Test Points

Test Point	Signal	Notes
TP1	TDI	
TP2	3.3V	
TP3	TDO	
TP4	1.8V	
TP5	TCK	
TP6	1.0V	
TP7	TMS	
TP8	1.35V	
TP9	5V	
TP10	GND	

TP11	GND	
TP12	GND	
TP13	GND	
TP14	POR B	Zync SoC reset signal
TP15	PG_1.35V	Power good signal
TP16	PG_1.8V	Power good signal
TP17	PG_3.3V	Power good signal
TP18	PG_1.0V	Power good signal
TP19	PUDC	Zynq SoC IO State during boot process
TP20	SPI0_DQ3/M0	Boot source select signal

Test Points Information

On-board Peripherals

Chip/Interface	Designator	Connected To	Notes
DDR3L RAM	U8	• Zynq SoC DDR Interface PS Bank 502	
System Controller CPLD	U11	• Zynq SoC MIO Bank 35 • MIDI DSI J4 • MIDI CSI J3 • FTDI U7 • LEDs	
USB-PHY	U18	• Zynq SoC MIO and Zynq SoC USB ULPI	
USB Ethernet Hub	J10	• USB PHY • USB A connectors J11 and J12 • Power switch for USB A connectors U15, U21 • ETH connector J10 • EEPROM U9	
FTDI	U3	• JTAG to System Controller and Zynq SoC • EEPROM U6	

I²C Expander	U10	• Zynq MIO (Bus master) • DDR3L via Voltage Bridge U12 shared with MIDI CSI J3 • MIDI DSI J4 and Pin Header J2 • HDMI socket J6 • Pin header J8	
I²C Interrupts	U10	• Zynq MIO (Bus master) • microSD Card socket J9 inseration detection • HDMI J6 inseration detection • Pin header J2	
Oscillator	U14	• Zynq SoC - PS	33.3 MHz
Oscillator	U9	• USB PHY	25 MHz
Oscillator	U7	• FTDI	12 MHz

On board peripherals

Configuration and System Control Signals

Connector	Signal Name	Direction[1)]	Description
S1	SPI0_DDQ3 / MO	IN	Boot source switch, SPI flash or SD Card
J13	EXTRST , POR_B , nRST	IN	Reset Zynq SoC
J14	PUDC	IN	State of Zynq SoC IO lines during boot
J15	JMODE , BDBUS7	IN	JTAG endpoint selction, System Controller or Zynq SoC

1) Direction:

- IN: Input from the point of view of this board.
- OUT: Output from the point of view of this board.

Controller signal.

Power and Power-On Sequence

Power Rails

Power Rail Name/ Schematic Name	Connector + Pin	Direction[1)]	Notes
USB_B_Vbus	J1	IN	Default power supply 5V
5V	J5.1	IN/OUT	2x Pin Header, intended for alternative powering
5V	J2.1 J8.2 , J8.4	OUT	5x Pin Header 2x 20 Pin Header
5V_HDMI	J6.18	OUT	HDMI, reverse current protection diode D11
V_BUS_A , V_BUS_B , V_BUS_C , V_BUS_D	J11.A1 , J11.B1 , J12.A1 , J12.B1	OUT	2x USB A socket
3.3V	J8.1 , J8.17 J3.15 J4.15 J9.4	OUT	2x 20 Pin Header FCC CSI FCC DSI microSD Card socket

1) Direction:

- IN: Input from the point of view of this board.
- OUT: Output from the point of view of this board.

Module power rails.

Recommended Power up Sequencing

Sequence	Net name	Recommended Voltage Range	Pull-up/down	Description	Notes
1	USB_B_Vbus	5V (± 5 %)	-	Main Power supply via Micro-USB J1.	Main module power supply. 0.5 A minimum. Power consumption depends mainly on design and cooling solution. If more current is needed use J5 for external power supply.
2	3.3V	-	-	Module generated output voltage.	
3	-	-	-	External components which are connected to J8 should be powered up with 3.3V from module.	See link: https://docs.amd.com/v/u/en-US/ds187-XC7Z010-XC7Z020-Data-Sheet , page 8 "PL PowerOn/Off Power Supply Sequencing" for PL IO usage

Baseboard Design Hints

Technical Specifications

Absolute Maximum Ratings *)

Power Rail / Schematic Name	Description	Min	Max	Unit
USB_B_Vbus	Determined through "USB 2.0 VBUS Max Limits"	4.75	5.5	V
5V	Determined through "USB 2.0 VBUS Max Limits"	4.75	5.5	V

Absolute maximum ratings

*) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Condition. Exposure to absolute-maximum rated conditions for extended periods may affect device reliability.

Recommended Operating Conditions

This TRM is generic for all variants. Temperature range can be differ depending on the assembly version. Voltage range is mostly the same during variants (exceptions are possible, depending on custom request)

Operating temperature range depends also on customer design and cooling solution. Please contact us for options.

- Variants of modules are described here: Article Number Information
- Modules with commercial temperature grade are equipped with components that cover at least the range of 0°C to 75°C
- Modules with extended temperature grade are equipped with components that cover at least the range of 0°C to 85°C
- Modules with industrial temperature grade are equipped with components that cover at least the range of -40°C to 85°C
- The actual operating temperature range will depend on the FPGA / SoC design / usage and cooling and other variables.

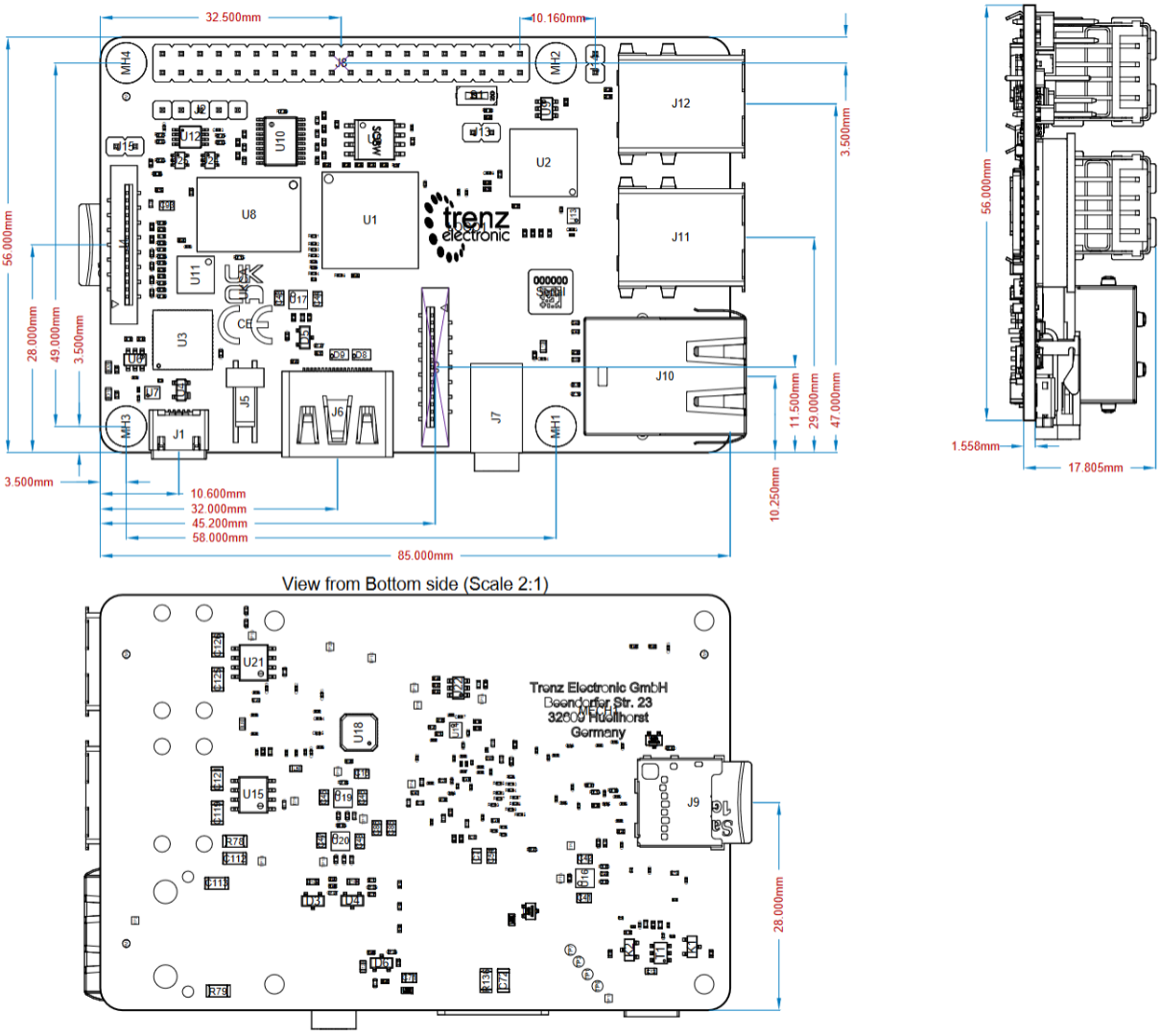
Parameter	Min	Max	Units	Reference Document
USB_B_Vbus	4.75	5.25	V	Schematic of this board. SCH-TE0726-04-41C94-A.PDF page 3, table "Supported Voltage Ranges"
5V	4.75	5.25	V	Schematic of this board. SCH-TE0726-04-41C94-A.PDF page 3, table "Supported Voltage Ranges"

Recommended operating conditions.

Physical Dimensions

- Module size: 85 mm × 56 mm. Please download the assembly diagram for exact numbers.

PCB thickness: 1.57 mm ± 10 %.



Physical Dimension

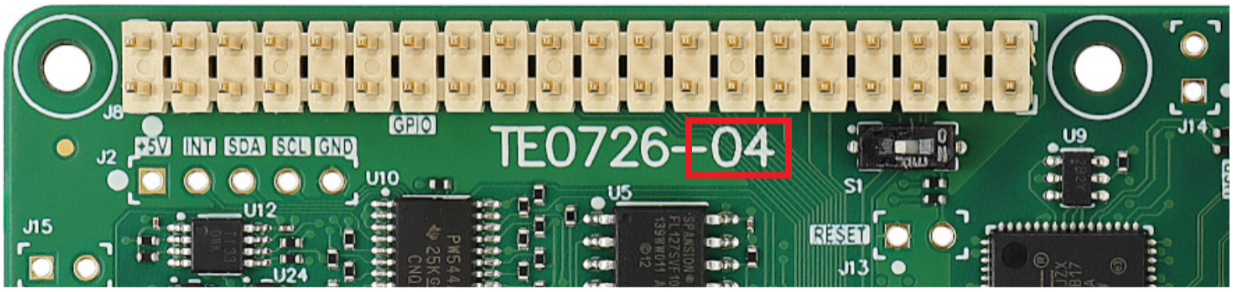
Currently Offered Variants

Trenz shop TE0726 overview page	
English page	German page

Trenz Electronic Shop Overview

Revision History

Hardware Revision History



Board hardware revision number.

Date	Revision	Changes	PCN Link	Documentation Link
2023-06-10	04	Page Numbers refer to the schematic for this revision	PCN-20230619 TE0726-03 to TE0726-04 Hardware Revision Change	TE0726-04

		• EOL components U16, U17 , U19, U20 (EN5311QI) were replaced by MPM3834CGPA
		• Added MIC bias power L12, C114 , R151 (Page 16)
		• Added Legal notices (Page 1)
		• Added power diagram (Page 4)
		• Added S1 switch and R152 for "JTAG only mode" enable (Page 8)
		• The signals were renamed:
		  ◦ SPI-DQ0 /M0 ---> SPI-DQ0 /M3
		  ◦ SPI-DQ3 /M3 ---> SPI-DQ3 /M0
		• ECC function has been added for U8 (Page 11)
		• Added I2C level shifter U12 for DDR3 ECC function (Page 11)
		• Added Buffers U24, U25 to match the level of signals (Page 6)
		• Added Diode D7, resistors R155, R160
		• EOL components L1, L2, L3, L4, L6, L7, L9, L10 BKP0603HS121-T replaced by MPZ0603S121HT000
		• EOL components D8, D9 SP5001-04TTG replaced by EMI8042MUTAG
		• Resistors R80-R82 replaced by 10 kOhm (was 1k43)
		• Added Testpoints TP15 - TP20
		• The type of testpoints TP1 - TP14 was updated. Diameter changed from 0.8 mm to 1 mm
		• CEC function is not supported. L11 was removed. C127, D5, R140, R42 are DNP
		• Power-up sequencing was updated for new DC-DC supplies
		• Capacitors C29, C32, C33 replaced by 470 nF (was 100 nF)		

2021-01-21	03	• Change DDR3 RAM (U8) from IM4G16D3FABG-125I to IS43TR16256BL-125KBLI • Clock Revision Change (U7, U14) from SiT8008AI-... to SiT8008BI-... • Clock Revision Change (U13) from SiT8008AI-... to SiT8008BI-... • LEDs D1 and D2 changed to 19-213/G6C-BM1N2/DT and 19-213/R6C-AL1M2VY/3T • Set S/N to not fitted	PCN-20210121 TE0726-03 DDR3 Change and Product Update	TE0726-03
2019-04-08	03	• VBUS Resistor R94 replaced by 10 kOhm (was 12k1)	-	TE0726-03

2016-05-06	03	• Introduced new variants:
		  ◦ Default with DDR3L 128 Mb
		  ◦ TE0726-03M with DDR3L 512 Mb
		  ◦ TE0726-03L with DDR3L 128 Mb, without usb's, eth_phy, RJ-45, CSI, DSI, HDMI and 3.5mm jack connectors
		• Changed FTDI to 56 pins package
		• Moved LED's into Raspberry Pi 3 layout
		• Replaced POWER connector on right angle connector
		• Corected conection PUDC pin
		• Replace HDMI, DSI/CSI connector, USB stacked connectors, RJ-45, power connector)
			-	TE0726-03

2016-01-26	02	• CSI CLK line moved to MRCC pin, CSI lanes swap • CSI camera GPIO moved to MIO GPIO • RPi GPIO 14,15 moved from MIO to PL • Added 47 µF capacitor for SD Card VCC (required by SD spec) • Added 47 µF capacitor for RPi camera - prevent voltage drop at camera init • Fixed MODE pin strapping • LED change 0603 • Added POWER connector 2 pin • Change HDMI ESD to ESD+EMI • Fixed HDMI HPD and backpower • DSI find solution for LS mode • Fixed XADC power caps • Changed LPDRR2 to DDR3L	-	TE0726-02
-	01	• Inital board release	-	-

Hardware Revision History

Hardware revision number can be found on the PCB board together with the module model number separated by the dash.

Document Change History

Date	Revision	Contributor	Description
Error rendering macro 'page-info' Ambiguous	**Error rendering macro 'page-info'** Ambiguous	**Error rendering macro 'page-info'** Ambiguous	• Removed editing bar from 2 pictures

method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interfac

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e com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	e com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	e com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	

2024-04-16	v.54	John Hartfiel	• Updated to new TRM style. • Updated to board REV04.
2017-11-10	v.52	John Hartfiel	• rework J8 header
2017-11-10	v.51	Ali Naseri	• Updated Power section • added Power-Distribution diagram
2017-05-30	v.40	Jan Kumann	• Absolute maximum ratings • Layout redesign • Wiki link fixed • SoC model removed from BD
2017-05-24	v.1	Jan Kumann	• Initial version
--	all	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot	• --

resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.

		atlassian . confluence.core. ContentEntityObject] [interface com. atlassian.user. User, class java. lang. String, class com. atlassian . confluence.core. ContentEntityObject]	

Document change history.

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Data Privacy

Please also note our data protection declaration at https://www.trenz-electronic.de/en/Data-protection-Privacy

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Error rendering macro 'page-info'

Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]