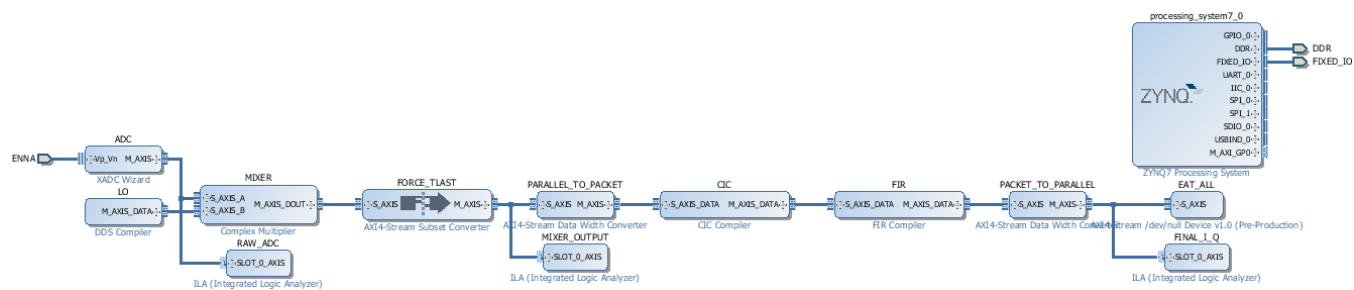
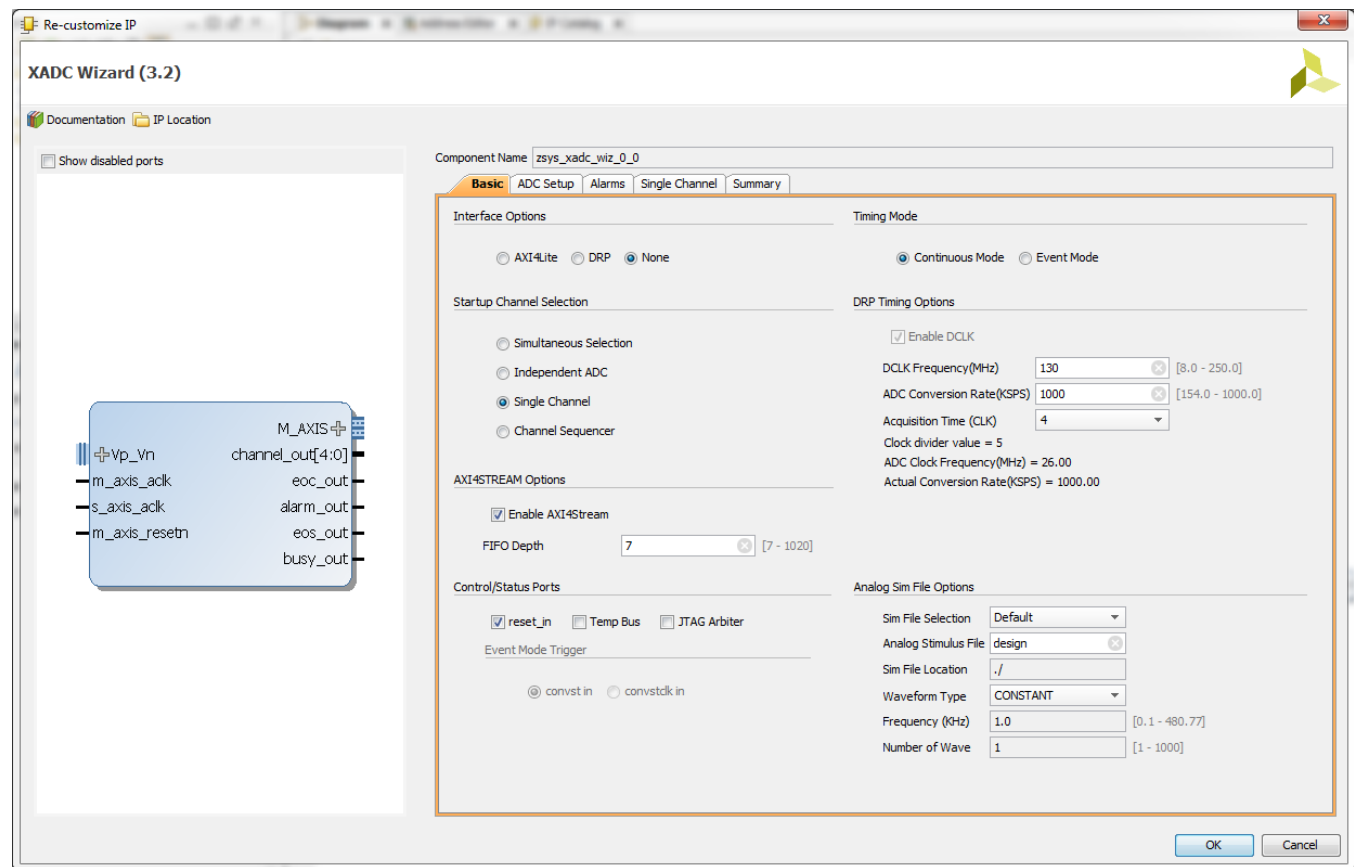


# SDR Demo

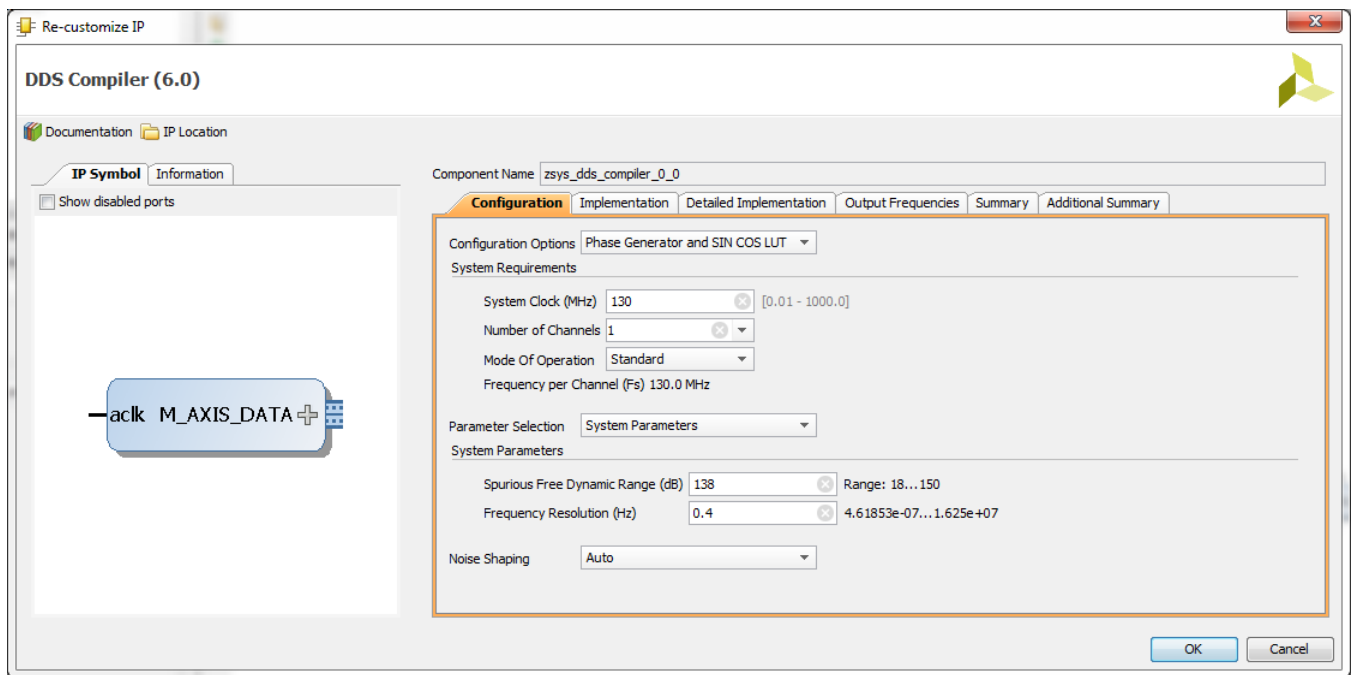
This is simple demo for DC (Direction Conversion) SDR function use in FPGA, for analog input XADC is used (Zynqberry mic input).



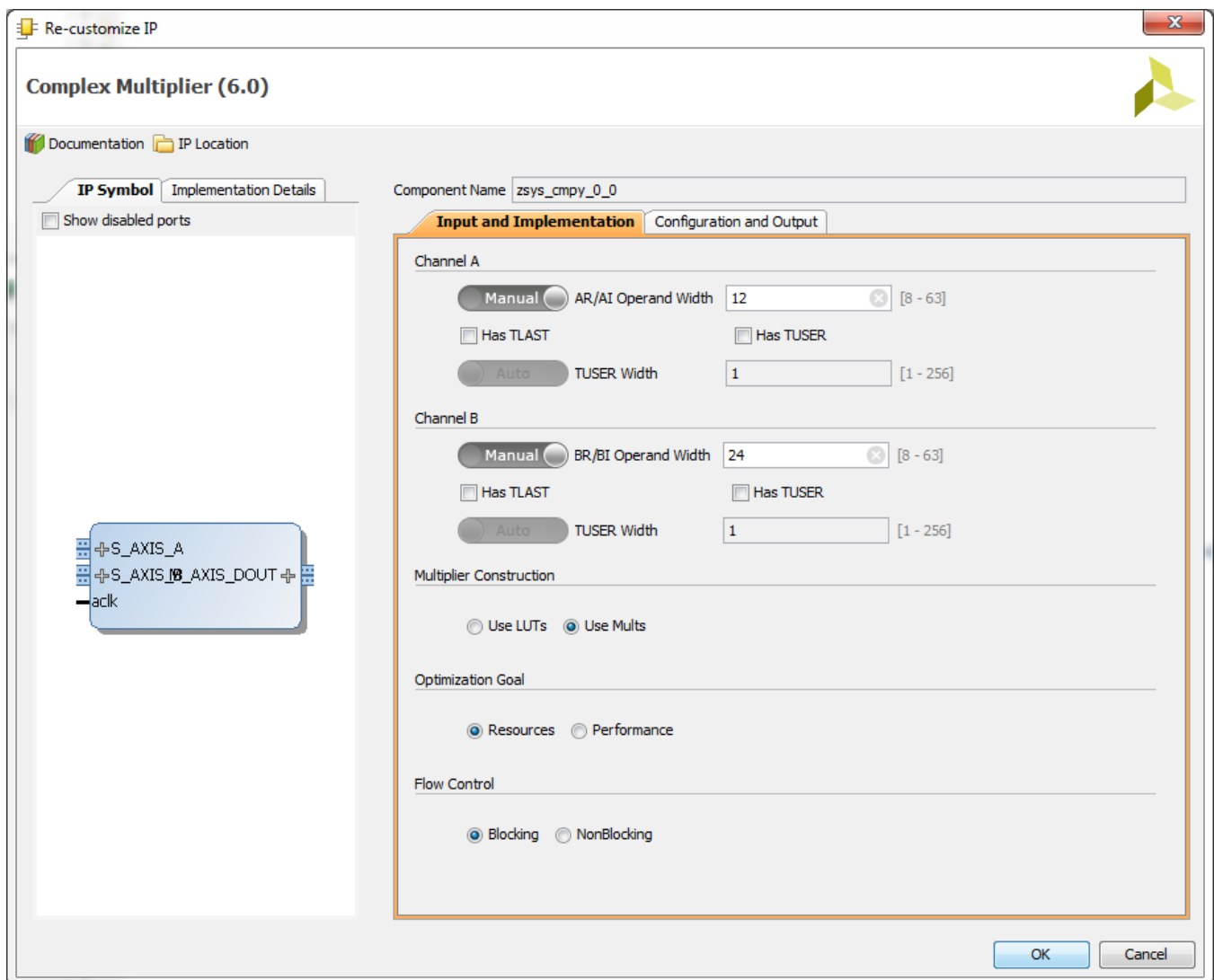
IPI BD for the SDR demo.



XADC is configured with streaming interface. Clock is set to 130MHz (generated with Clock Wizard) XADC sample rate exactly 1MSPS.



DDS Compiler Wizard is used to generate LO (local oscillator) Sinus and Cosinus outputs. LO output is multiplied with the input from XADC. All AXI4-Streaming components run from single system clock (130MHz). XADC asserts TVALID with the rate of ADC sampling, that is 1 MHz. To make DDS to work at 130MHz TREADY input of the DDS Output stream must be tied to 1.



After complex multiplier AXI stream subset converter is used to force TLAST to 1, then AXI stream datawidth converter is used to convert single samples with I and Q values into stream of interleaved I and Q values. This stream is going into CIC block that converts the sampling frequency down.

Re-customize IP

# CIC Compiler (4.0)

Documentation
IP Location

**IP Symbol**
Freq Response
Im

☐ Show disabled ports

S\_AXIS\_DATA
M\_AXIS\_DATA
ack
event\_last\_unexpected
event\_last\_missing

Component Name
zsys\_cic\_compiler\_0\_0

**Filter Options**
Implementation Options
Summary

Filter Specification

Filter Type
Decimation

Number Of Stages
6

Differential Delay
2

Number Of Channels
2

Sample Rate Change Specification

Sample Rate

☒ Fixed
☐ Programmable

Fixed Or Initial Rate
20
[4 - 8192]

Minimum Rate
20
[4 - 20]

Maximum Rate
20
[20 - 8192]

Hardware Oversampling Specification

Rate Specification
Frequency Specification

Input Sample Frequency (MHz)
1
[1.0E-6 - 300.0]

Clock Frequency (MHz)
130.0
[2.0 - 600.0]

Sample Period (Clock Cycles)
1
[1 - 10000000]

Selects the type of rate change

OK
Cancel

Configuration of the CIC

IP Symbol

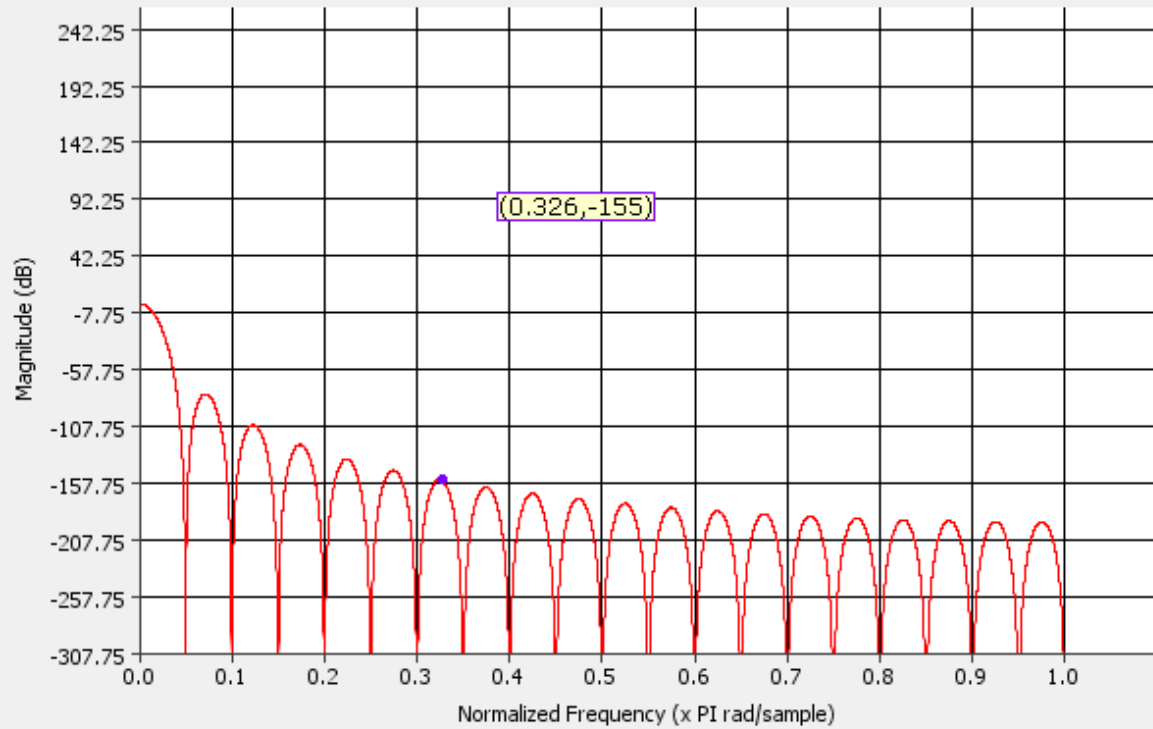
Freq Response

Implementation Details

Sample

— Data1

Frequency Response (Magnitude)



Response Magnitude Normalized

Filter Analysis

Pass Band

Range : 0.0 - 0.5

|        |                 |
|--------|-----------------|
| Min    | -1948.367932 dB |
| Max    | 0.000000 dB     |
| Ripple | 1948.367932 dB  |

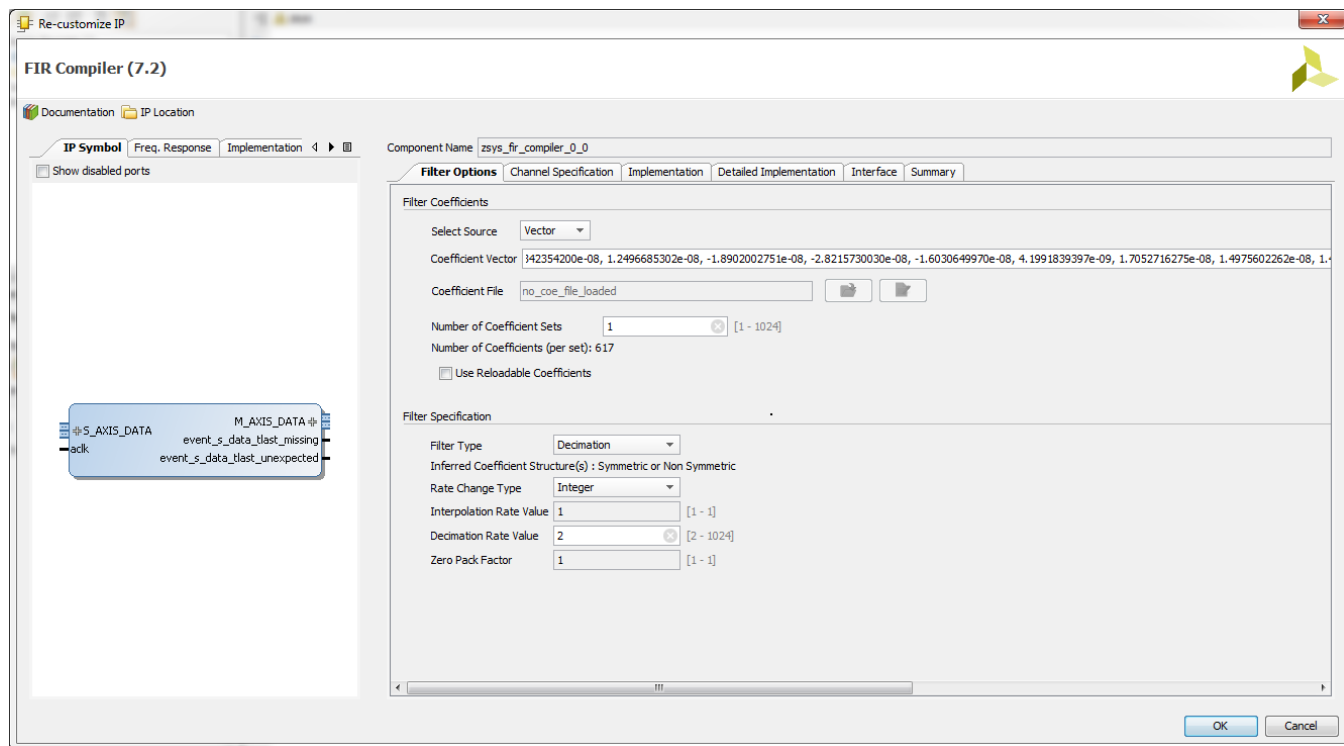
Stop Band

Range : 0.5 - 1.0

|        |                 |
|--------|-----------------|
| Min    | -1994.301014 dB |
| Max    | -176.139760 dB  |
| Ripple | 1818.161254 dB  |

CIC Frequency response.

Downconverted I and Q stream enters a FIR block that also reduces sample rate by 2.



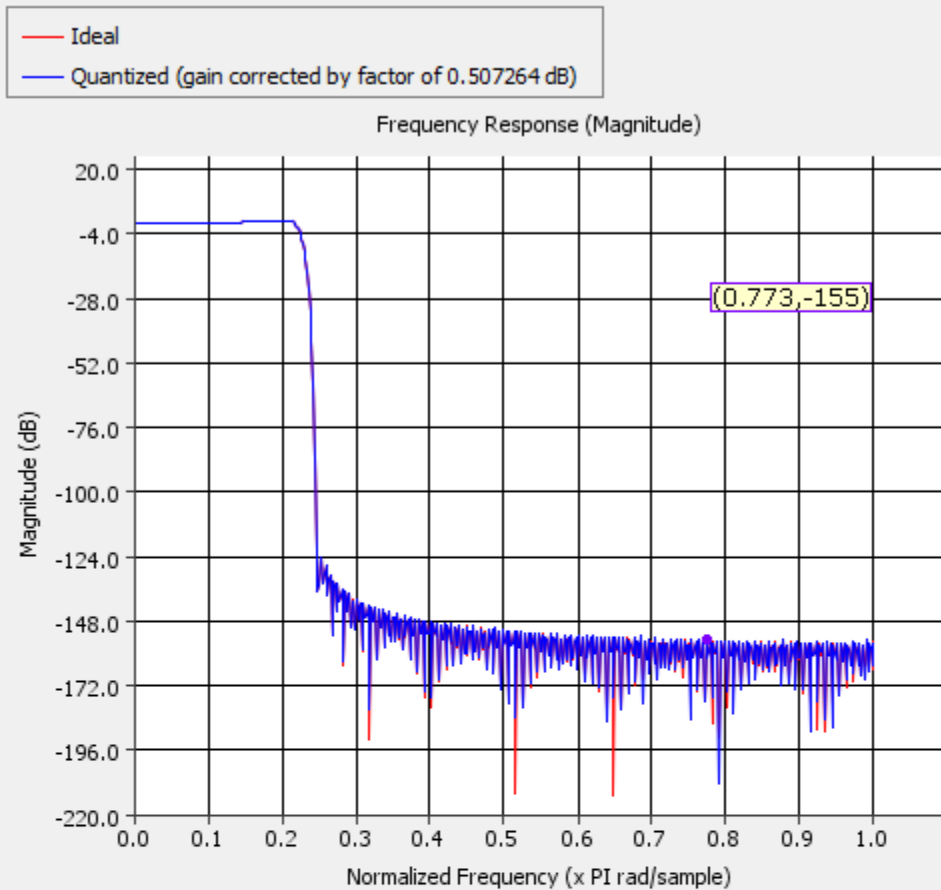
Configuration of the FIR.

IP Symbol

**Freq. Response**

Implementation Details

Coefficient Reload



Set to Display 1 [1 - 1]

Filter Analysis

Pass Band

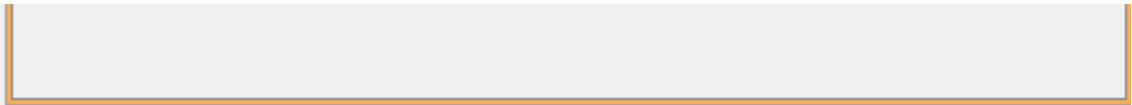
Range : 0.0 - 0.5

|        |                |
|--------|----------------|
| Min    | -180.795726 dB |
| Max    | 0.935472 dB    |
| Ripple | 181.731198 dB  |

Stop Band

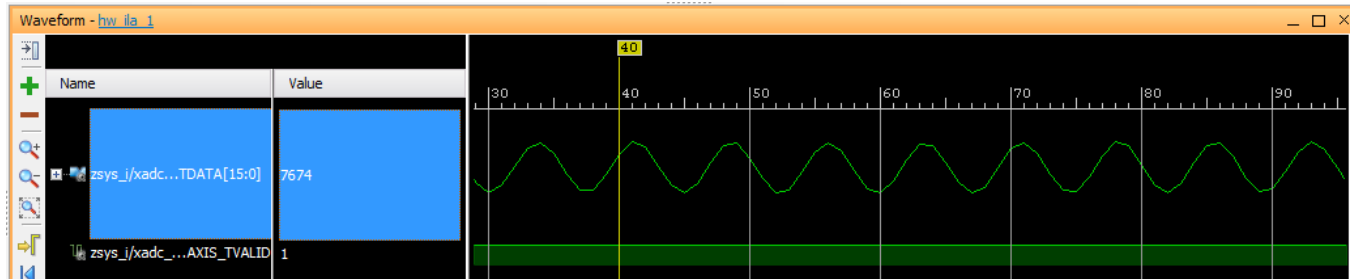
Range : 0.5 - 1.0

|        |                |
|--------|----------------|
| Min    |                |
| Max    | -151.634289 dB |
| Ripple |                |

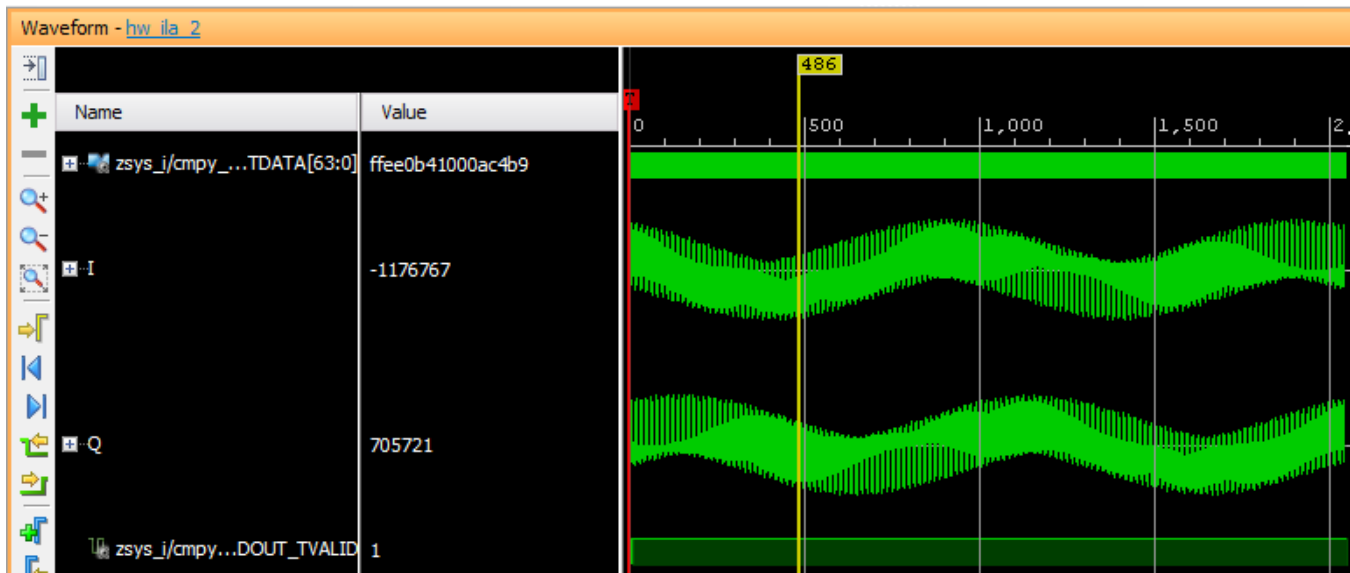


Frequency response of the FIR Filter.

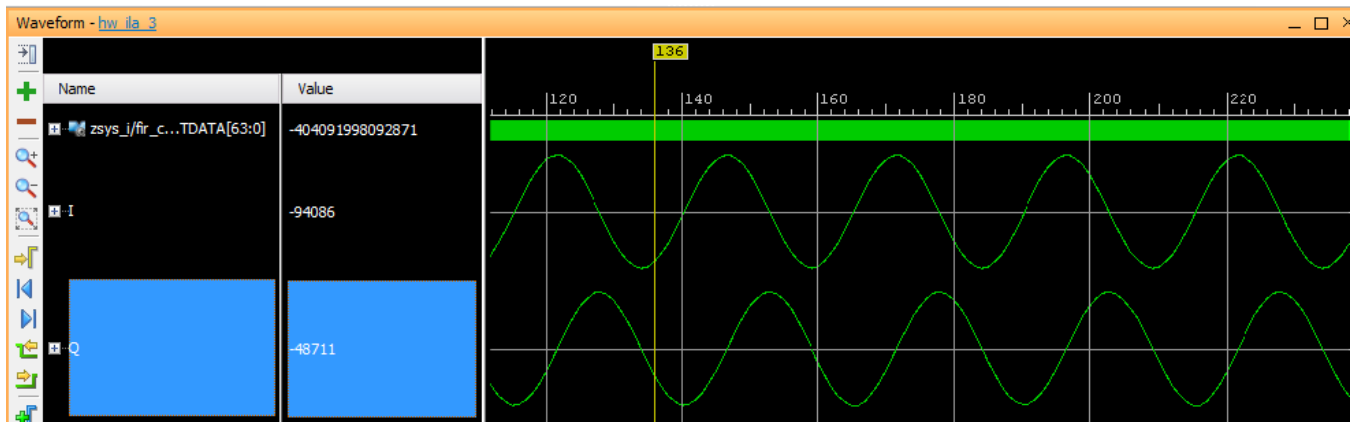
After FIR filter AXI stream datawidtht converter is used again to get convert the interleaved samples of I and Q as single AXIS stream TDATA word. The processing is terminated by AXI stream DEVNULL that eats all. For visualization and data capture ILA Logic Analyzer IP cores are inserted. For test purposes the LO frequency was set to 134KHz (this is close to WSPR band where beacons are expected to be present in frequency band).



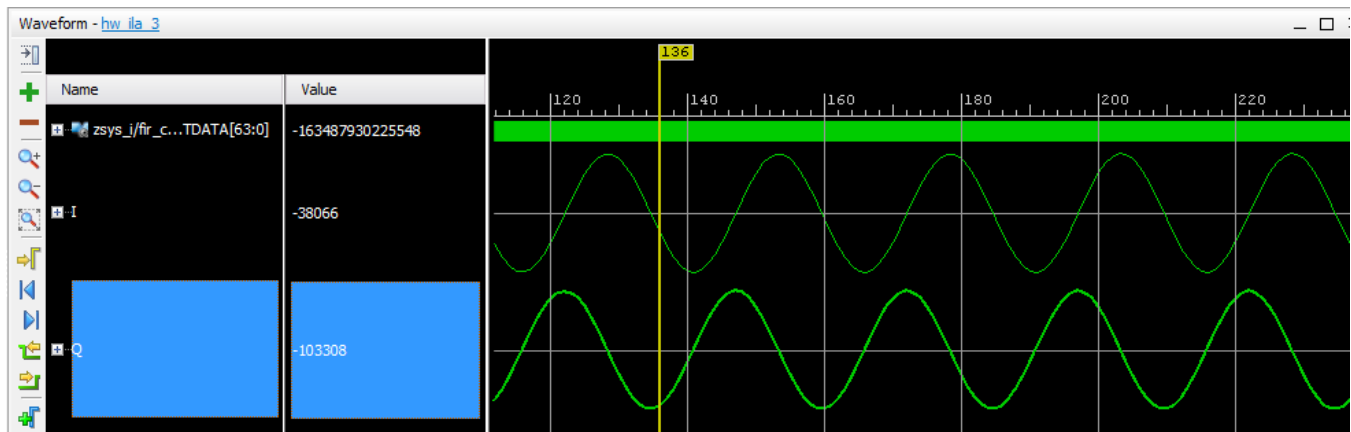
XADC Raw data, capturing 135KHz signal from Zynqberry mic input.



I and Q immediatly after the complex multiplier



I and Q data after DDC and FIR with input signal at 135KHz, 1 KHz signal is seen  $135\text{KHz} - 134\text{MHz} = 1\text{KHz}$ .



Output with 133KHz input signal, 1KHz signal is seen  $133\text{KHz} - 134\text{KHz} = -1\text{KHz}$ , the phase of I and Q is now different.