Zynq USB

Xilinx Zynq-7000 PS has two USB IP Cores that can be used over dedicated MIO pins only (EMIO multiplexing is not supported). If both USB IP Cores is used then SD Card boot is no longer supported.

PHY Reset requirements

Xilinx default standard FSBL can perform USB ULPI PHY Reset only if the reset is directly connected to MIO GPIO, if not then fsbl_hooks.c has to include custom code to reset the USB PHY.

SoM	USB PHY Reset	Notes
TE0715	MIO51	PS7 Config must include MIO51 as USB Reset, polarity active low
TE0720	System Controller	Reset must be implemented in fsbl_hooks.c
TE0723		
TE0726		
TE0745		
TE0782	MIO0	Common for both USB PHY's

USB VBUS Control

If USB Host VBUS is controlled by the USB ULPI PHY, then power will not be present until software stack enables it. If the USB drivers or USB ULPI PHY drivers do not load correctly, and if the USB mode is not set to Host, then VBUS remains off.

Linux Kernel

Petalinux default Kernel configuration does not enable all needed drivers for the USB to operate properly, menuconfig has to be used to select or enable required drivers.

Linux Devicetree

Petalinux automatically generated devicetree is not sufficient, devicetree top file has to be edited manually for proper USB operation, the changes required depend on the Petalinux version used.