

Multiboot

SREC Loader with U-Boot

This is one of the easiest solutions to implement full multiboot application for any Xilinx 7 Series or Ultrascale FPGA.

A Microblaze based system should be made with following IP Core from Xilinx free Vivado IP Catalog:

- AXI_QSPI
- AXI_HWICAP
- AXI_UARTLITE
- AXI_GPIO
- MIG (for External Memory access)

Offset	Size	Content	Notes
		Application bitstream #2	
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	Sizeof(u-boot.SREC) + padding	u-boot converted to SREC format	
0 + Sizeof(golden.bit) + padding	0x2000	u-boot flash environment	Offset must be larger than size of FPGA bitstream
0x000000		GOLDEN bitstream	First bootloader (like SREC SPI Loader) is embedded in BRAM and loaded with the bitstream

Xilinx SREC SPI loader is used to bootstrap u-boot into external memory, then u-boot is used for all flash operations as required. The image to be written can be loaded to external RAM and then written to SPI Flash as needed.

Step by Step

1. FPGA loads from address 0, Microblaze starts from BRAM with SREC Loader
2. SREC Loader (customized part of it) checks some I/O pin to choose between update mode or normal mode
3. In case of Update mode, SREC loader loads u-boot into external RAM and executes u-boot
4. In case of Normal Application mode, warm boot is executed by writes to HWICAP to start Application Bitstream

This process involves least amount of custom coding, the only custom code is small function that talks to HWICAP, and the "check" of update mode in the SREC Loader. All functions related to SPI Flash erasing and writing are done with u-boot.

References

List of references source for additional information

1. UG470 7-Series FPGAs Configuration
2. UG908 Vivado Design Suite User Guide: Programming and Debugging
3. PG134 AXI HWICAP v3.0
4. PG153 AXI Quad SPI v3.2
5. XAPP1247 MultiBoot with 7 Series FPGAs and SPI
6. XAP586 Using SPI with 7 Series FPGAs

