

4 x 5 SoM Integration Guide

Table of Content

- 1 Table of Content
 - 1.1 Power and Signal Pin Assignment
 - 1.1.1 How to Use This Guide
 - 1.1.2 Module Power Connection Table
 - 1.1.3 Module Pinout Overview
 - 1.1.4 Carrier Board Power Connection Table
 - 1.1.5 Carrier Pinout Overview
 - 1.2 4x5 Module Controller I/Os
 - 1.3 Remove 4x5 module
 - 1.4 Compatibility Guide
 - 1.4.1 Ethernet LED'S
 - 1.4.2 JM2 pins 1, 3 (TE0720 Bank 34 Voltage)
 - 1.5 Carrier Board Checklist
 - 1.5.1 Schematic Checklist
 - 1.5.2 PCB Checklist
 - 1.5.3 Visual Check of Module placement

Power and Signal Pin Assignment

How to Use This Guide

- This guide is split into two tables:
 - Module Power Connection Table** section shows the power source of the different FPGA banks and components of the different module boards as well as the power and group location on the B2B connectors of the module site.
 - Carrier Board Power Connection Table** section shows the power source of the B2B connectors with pins, schematic names and available options of the different carrier boards as well as the power location on the B2B connectors of the carrier site.
 - The PCBs have fixed and variable user supplied I/O voltage pins. Variable power supply pins are colored in four groups (VCCIOA, VCCIOB, VCCIOC and VCCIOD).
- Find your module model on the **Module Power Connection Table** and check the power supply of the different FPGA banks.
 - If the power supply is variable(colored), go to the **Carrier Board Power Connection Table** and see how it's connected on your carrier board. Often the power source can be selected by jumper, resistor or variable used from other connector pin of the carrier board. So use the schematic name or the component designator from the table to search for the available options in the PCB schematics or TRM.
 - Additional Master Pinout Viewer/XDC-Generator is available on [Trenz Electronic Download - Pinout](#)

Module Power Connection Table

Group	1				2				3				4				5				6				7				8	9	special
Module Model	Bank	I/Os	Type	Voltage	Bank	I/Os	Type	Voltage	Bank	I/Os	Type	Voltage	Bank	I/Os	Type	Voltage	Bank	I/Os	Type	Voltage	Bank	I/Os	Type	Voltage	Bank	I/Os	Type	Voltage			
TE0710	B15	48	HR	VC CIOA	-	-	-	-	-	-	-	-	B34	50	HR	VC CIOD	B16	6	HR	3.3 V	B14	8	HR	3.3 V	2x 100Mb it ETH						
TE0711	B15	48	HR	VC CIOA	B34	36	HR	VC CIOB	B14	18	HR	3.3 V	B35	50	HR	VC CIOD	B16	6	HR	1.8 V	B14	8	HR	3.3 V	B34	8	HR	VC CIOB	B34(4)	USB	
TE0712	B16	48	HR	VC CIOA	B13	20	HR	VC CIOB	B14	18	HR	3.3 V	B15	50	HR	VC CIOD	B13	6	HR	VC CIOB	B14	8	HR	3.3 V	1x 100Mb it ETH / B13	4	HR	VC CIOB		B14	4x GTP on G2
TE0713																															4x GTP on G2
TE0715 with Z-7015 Z-7012S	B13	48	HR	VC CIOA	B34	16	HR	VC CIOC	B34	18	HR	VC CIOC	B35	50	HR	VC CIOD	B5 01	6	MIO	1.8 V	B500	8	MIO	3.3 V	1x Gbit ETH				SGMII	USB	4x GTP on G2

TE0715 with Z-7030	B13	48	HR	VC CIOA	B34	16	HP	VC CIOC	B34	18	HP	VC CIOC	B35	50	HP	VC CIOD	B5 01	6	MIO	1.8 V	B500	8	MIO	3.3 V	1x Gbit ETH				SGMII	USB	4x GTP on G2
TE0720	B35	48	HR	VC CIOA	B34	36	HR	VC CIOB	B33	18	HR	VC CIOC	B13	50	HR	VC CIOD	B5 01	6	MIO	1.8 V	B500	8	MIO	3.3 V	1x Gbit ETH				SGMII	USB	
TE0820*	B66	48	HP	VC CIOA	B65	16	HP	VC CIOC	B65	18	HP	VC CIOC	B64	50	HP	VC CIOD	B5 01	6	MIO	3.3 V	B5 01	8	MIO	3.3 V	1x Gbit ETH				SGMII	USB	4x GTR on G2
TE0821*	B26	48	HD	VC CIOA	B65	16	HP	VC CIOC	B65	18	HP	VC CIOC	B24	48	HD	VC CIOD	B5 01	6	MIO	3.3 V	B5 01	8	MIO	3.3 V	1x Gbit ETH				SGMII	USB	4x GTR on G2
TE0823*	B66	48	HP	VC CIOA	B65	16	HP	VC CIOC	B65	18	HP	VC CIOC	B64	50	HP	VC CIOD	B5 01	6	MIO	3.3 V	B5 01	8	MIO	3.3 V	1x Gbit ETH				SGMII	USB	4x GTR on G2
TE0741	B13	48	HR	VC CIOA	B16	16	HR	VC CIOB	B15	18	HR	VC CIOC	B12	50	HR	VC CIOD	1x GTX	1 Lane			B14	8	HR	3.3 V	2x GTX	2 Lan es		1x GTX		4x GTX on G2	
TE0742*																															
TE0841	B64	48	HR	VC CIOA	B66	16	HP	VC CIOB	B68	18	HP	VC CIOC	B67	50	HP	VC CIOD	1x GTH	1 Lane			B65	8	HR	3.3 V	2x GTH	2 Lan es		1x GTH		4x GTH on G2	
TE0842*																															

I/O resource comparison for all 4x5 modules. There are maximum 4 user supplied I/O voltages (VCCIOA, VCCIOB, VCCIOC and VCCIOD).

*Attention: Maximum supply voltage for HP banks is 1.8V.
Module B2B FPGA-Banks and Voltages

Module Pinout Overview

JMS				JMS			
Direction	Name	Pin	Direction	Name	Pin	Direction	
io/tx/tx	MST TX	1	io/tx/tx	MST TX	1	io/tx/tx	
io/tx/tx	MST TX	2	io/tx/tx	MST TX	2	io/tx/tx	
io/tx/tx	MST TX	3	io/tx/tx	MST TX	3	io/tx/tx	
io/tx/tx	MST TX	4	io/tx/tx	MST TX	4	io/tx/tx	
io/tx/tx	MST TX	5	io/tx/tx	MST TX	5	io/tx/tx	
io/tx/tx	MST TX	6	io/tx/tx	MST TX	6	io/tx/tx	
io/tx/tx	MST TX	7	io/tx/tx	MST TX	7	io/tx/tx	
io/tx/tx	MST TX	8	io/tx/tx	MST TX	8	io/tx/tx	
io/tx/tx	MST TX	9	io/tx/tx	MST TX	9	io/tx/tx	
io/tx/tx	MST TX	10	io/tx/tx	MST TX	10	io/tx/tx	
io/tx/tx	MST TX	11	io/tx/tx	MST TX	11	io/tx/tx	
io/tx/tx	MST TX	12	io/tx/tx	MST TX	12	io/tx/tx	
io/tx/tx	MST TX	13	io/tx/tx	MST TX	13	io/tx/tx	
io/tx/tx	MST TX	14	io/tx/tx	MST TX	14	io/tx/tx	
io/tx/tx	MST TX	15	io/tx/tx	MST TX	15	io/tx/tx	
io/tx/tx	MST TX	16	io/tx/tx	MST TX	16	io/tx/tx	
io/tx/tx	MST TX	17	io/tx/tx	MST TX	17	io/tx/tx	
io/tx/tx	MST TX	18	io/tx/tx	MST TX	18	io/tx/tx	
io/tx/tx	MST TX	19	io/tx/tx	MST TX	19	io/tx/tx	
io/tx/tx	MST TX	20	io/tx/tx	MST TX	20	io/tx/tx	
io/tx/tx	MST TX	21	io/tx/tx	MST TX	21	io/tx/tx	
io/tx/tx	MST TX	22	io/tx/tx	MST TX	22	io/tx/tx	
io/tx/tx	MST TX	23	io/tx/tx	MST TX	23	io/tx/tx	
io/tx/tx	MST TX	24	io/tx/tx	MST TX	24	io/tx/tx	
io/tx/tx	MST TX	25	io/tx/tx	MST TX	25	io/tx/tx	
io/tx/tx	MST TX	26	io/tx/tx	MST TX	26	io/tx/tx	
io/tx/tx	MST TX	27	io/tx/tx	MST TX	27	io/tx/tx	
io/tx/tx	MST TX	28	io/tx/tx	MST TX	28	io/tx/tx	
io/tx/tx	MST TX	29	io/tx/tx	MST TX	29	io/tx/tx	
io/tx/tx	MST TX	30	io/tx/tx	MST TX	30	io/tx/tx	
io/tx/tx	MST TX	31	io/tx/tx	MST TX	31	io/tx/tx	
io/tx/tx	MST TX	32	io/tx/tx	MST TX	32	io/tx/tx	
io/tx/tx	MST TX	33	io/tx/tx	MST TX	33	io/tx/tx	
io/tx/tx	MST TX	34	io/tx/tx	MST TX	34	io/tx/tx	
io/tx/tx	MST TX	35	io/tx/tx	MST TX	35	io/tx/tx	
io/tx/tx	MST TX	36	io/tx/tx	MST TX	36	io/tx/tx	
io/tx/tx	MST TX	37	io/tx/tx	MST TX	37	io/tx/tx	
io/tx/tx	MST TX	38	io/tx/tx	MST TX	38	io/tx/tx	
io/tx/tx	MST TX	39	io/tx/tx	MST TX	39	io/tx/tx	
io/tx/tx	MST TX	40	io/tx/tx	MST TX	40	io/tx/tx	
io/tx/tx	MST TX	41	io/tx/tx	MST TX	41	io/tx/tx	
io/tx/tx	MST TX	42	io/tx/tx	MST TX	42	io/tx/tx	
io/tx/tx	MST TX	43	io/tx/tx	MST TX	43	io/tx/tx	
io/tx/tx	MST TX	44	io/tx/tx	MST TX	44	io/tx/tx	
io/tx/tx	MST TX	45	io/tx/tx	MST TX	45	io/tx/tx	
io/tx/tx	MST TX	46	io/tx/tx	MST TX	46	io/tx/tx	
io/tx/tx	MST TX	47	io/tx/tx	MST TX	47	io/tx/tx	
io/tx/tx	MST TX	48	io/tx/tx	MST TX	48	io/tx/tx	
io/tx/tx	MST TX	49	io/tx/tx	MST TX	49	io/tx/tx	
io/tx/tx	MST TX	50	io/tx/tx	MST TX	50	io/tx/tx	
io/tx/tx	MST TX	51	io/tx/tx	MST TX	51	io/tx/tx	
io/tx/tx	MST TX	52	io/tx/tx	MST TX	52	io/tx/tx	
io/tx/tx	MST TX	53	io/tx/tx	MST TX	53	io/tx/tx	
io/tx/tx	MST TX	54	io/tx/tx	MST TX	54	io/tx/tx	
io/tx/tx	MST TX	55	io/tx/tx	MST TX	55	io/tx/tx	
io/tx/tx	MST TX	56	io/tx/tx	MST TX	56	io/tx/tx	
io/tx/tx	MST TX	57	io/tx/tx	MST TX	57	io/tx/tx	
io/tx/tx	MST TX	58	io/tx/tx	MST TX	58	io/tx/tx	
io/tx/tx	MST TX	59	io/tx/tx	MST TX	59	io/tx/tx	
io/tx/tx	MST TX	60	io/tx/tx	MST TX	60	io/tx/tx	

Positions are displayed as Top View

Legend
Power-VCC
Power-GND
GROUP1
GROUP2
GROUP3
GROUP4
GROUP5
GROUP6
GROUP7
GROUP8
GROUP9
GROUP10
GROUP11
GROUP12
GROUP13
GROUP14
GROUP15
GROUP16
GROUP17
GROUP18
GROUP19
GROUP20
GROUP21
GROUP22
GROUP23
GROUP24
GROUP25
GROUP26
GROUP27
GROUP28
GROUP29
GROUP30
GROUP31
GROUP32
GROUP33
GROUP34
GROUP35
GROUP36
GROUP37
GROUP38
GROUP39
GROUP40
GROUP41
GROUP42
GROUP43
GROUP44
GROUP45
GROUP46
GROUP47
GROUP48
GROUP49
GROUP50
GROUP51
GROUP52
GROUP53
GROUP54
GROUP55
GROUP56
GROUP57
GROUP58
GROUP59
GROUP60
GROUP61
GROUP62
GROUP63
GROUP64
GROUP65
GROUP66
GROUP67
GROUP68
GROUP69
GROUP70
GROUP71
GROUP72
GROUP73
GROUP74
GROUP75
GROUP76
GROUP77
GROUP78
GROUP79
GROUP80
GROUP81
GROUP82
GROUP83
GROUP84
GROUP85
GROUP86
GROUP87
GROUP88
GROUP89
GROUP90
GROUP91
GROUP92
GROUP93
GROUP94
GROUP95
GROUP96
GROUP97
GROUP98
GROUP99
GROUP100

Direction	Name	Pin	Direction	Name	Pin	Direction
in	VCCIOA	1	in	PWR_1	1	in
in	VCCIOA	2	in	PWR_1	2	in
in	VCCIOA	3	in	PWR_1	3	in
in	VCCIOA	4	in	PWR_1	4	in
in	VCCIOA	5	in	PWR_1	5	in
in	VCCIOA	6	in	PWR_1	6	in
in	VCCIOA	7	in	PWR_1	7	in
in	VCCIOA	8	in	PWR_1	8	in
in	VCCIOA	9	in	PWR_1	9	in
in	VCCIOA	10	in	PWR_1	10	in
in	VCCIOA	11	in	PWR_1	11	in
in	VCCIOA	12	in	PWR_1	12	in
in	VCCIOA	13	in	PWR_1	13	in
in	VCCIOA	14	in	PWR_1	14	in
in	VCCIOA	15	in	PWR_1	15	in
in	VCCIOA	16	in	PWR_1	16	in
in	VCCIOA	17	in	PWR_1	17	in
in	VCCIOA	18	in	PWR_1	18	in
in	VCCIOA	19	in	PWR_1	19	in
in	VCCIOA	20	in	PWR_1	20	in
in	VCCIOA	21	in	PWR_1	21	in
in	VCCIOA	22	in	PWR_1	22	in
in	VCCIOA	23	in	PWR_1	23	in
in	VCCIOA	24	in	PWR_1	24	in
in	VCCIOA	25	in	PWR_1	25	in
in	VCCIOA	26	in	PWR_1	26	in
in	VCCIOA	27	in	PWR_1	27	in
in	VCCIOA	28	in	PWR_1	28	in
in	VCCIOA	29	in	PWR_1	29	in
in	VCCIOA	30	in	PWR_1	30	in
in	VCCIOA	31	in	PWR_1	31	in
in	VCCIOA	32	in	PWR_1	32	in
in	VCCIOA	33	in	PWR_1	33	in
in	VCCIOA	34	in	PWR_1	34	in
in	VCCIOA	35	in	PWR_1	35	in
in	VCCIOA	36	in	PWR_1	36	in
in	VCCIOA	37	in	PWR_1	37	in
in	VCCIOA	38	in	PWR_1	38	in
in	VCCIOA	39	in	PWR_1	39	in
in	VCCIOA	40	in	PWR_1	40	in
in	VCCIOA	41	in	PWR_1	41	in
in	VCCIOA	42	in	PWR_1	42	in
in	VCCIOA	43	in	PWR_1	43	in
in	VCCIOA	44	in	PWR_1	44	in
in	VCCIOA	45	in	PWR_1	45	in
in	VCCIOA	46	in	PWR_1	46	in
in	VCCIOA	47	in	PWR_1	47	in
in	VCCIOA	48	in	PWR_1	48	in
in	VCCIOA	49	in	PWR_1	49	in
in	VCCIOA	50	in	PWR_1	50	in
in	VCCIOA	51	in	PWR_1	51	in
in	VCCIOA	52	in	PWR_1	52	in
in	VCCIOA	53	in	PWR_1	53	in
in	VCCIOA	54	in	PWR_1	54	in
in	VCCIOA	55	in	PWR_1	55	in
in	VCCIOA	56	in	PWR_1	56	in
in	VCCIOA	57	in	PWR_1	57	in
in	VCCIOA	58	in	PWR_1	58	in
in	VCCIOA	59	in	PWR_1	59	in
in	VCCIOA	60	in	PWR_1	60	in
in	VCCIOA	61	in	PWR_1	61	in
in	VCCIOA	62	in	PWR_1	62	in
in	VCCIOA	63	in	PWR_1	63	in
in	VCCIOA	64	in	PWR_1	64	in
in	VCCIOA	65	in	PWR_1	65	in
in	VCCIOA	66	in	PWR_1	66	in
in	VCCIOA	67	in	PWR_1	67	in
in	VCCIOA	68	in	PWR_1	68	in
in	VCCIOA	69	in	PWR_1	69	in
in	VCCIOA	70	in	PWR_1	70	in
in	VCCIOA	71	in	PWR_1	71	in
in	VCCIOA	72	in	PWR_1	72	in
in	VCCIOA	73	in	PWR_1	73	in
in	VCCIOA	74	in	PWR_1	74	in
in	VCCIOA	75	in	PWR_1	75	in
in	VCCIOA	76	in	PWR_1	76	in
in	VCCIOA	77	in	PWR_1	77	in
in	VCCIOA	78	in	PWR_1	78	in
in	VCCIOA	79	in	PWR_1	79	in
in	VCCIOA	80	in	PWR_1	80	in
in	VCCIOA	81	in	PWR_1	81	in
in	VCCIOA	82	in	PWR_1	82	in
in	VCCIOA	83	in	PWR_1	83	in
in	VCCIOA	84	in	PWR_1	84	in
in	VCCIOA	85	in	PWR_1	85	in
in	VCCIOA	86	in	PWR_1	86	in
in	VCCIOA	87	in	PWR_1	87	in
in	VCCIOA	88	in	PWR_1	88	in
in	VCCIOA	89	in	PWR_1	89	in
in	VCCIOA	90	in	PWR_1	90	in
in	VCCIOA	91	in	PWR_1	91	in
in	VCCIOA	92	in	PWR_1	92	in
in	VCCIOA	93	in	PWR_1	93	in
in	VCCIOA	94	in	PWR_1	94	in
in	VCCIOA	95	in	PWR_1	95	in
in	VCCIOA	96	in	PWR_1	96	in
in	VCCIOA	97	in	PWR_1	97	in
in	VCCIOA	98	in	PWR_1	98	in
in	VCCIOA	99	in	PWR_1	99	in
in	VCCIOA	100	in	PWR_1	100	in

Module basic power and group pin assignment, recommended to verify with Schematics

Carrier Board Power Connection Table

IO Voltage		B2B Connector		Carrier Boards													
Name	Direction*	JB1	JB2	TE0701		TE0703 Rev01 - Rev04		TE0703 Rev 05		TE0705		TE0706		TEBA0841		TEBA0841 REV01	
		Pin	Pin	Schematic Name	Value, Option, Comp.	Schematic Name	Value, Option, Comp.	Schematic Name	Value,Option, Comp.	Schematic Name	Value, Option, Comp.	Schematic Name	Value,Option, Comp.	Schematic Name	Value,Option, Comp.	Schematic Name	Value,Option, Comp.
PWR_1	out	2,4,6	1,3,5,7	5V0	5V	3.3V	3.3V	3.3V	3.3V	5V0	5V	3.3V	3.3V	3.3V	use ext. 3.3V power supply	3.3V	use ext. 3.3V power supply
VCCIOA	out	10,12		VIOTB	FMC_VA DJ 2V5 3.3VOUT	VCCIO35	R23M3.3VOUT J1B-B1	VCCIOA	J5M3.3VOUT, M1.8VOUT R23M3.3VOUT J1-B1	VIOTB	FMC_VA DJ 2V5 3.3VOUT	VCCIO35	R20->M3.3VOUT/J6B-B32	VCCIOA	J26 M1.8VOUT, 2.5V, 3.3V_OUT J20-6,J20-45	VCCIOA	J26 M1.8VOUT, 2.5V, 3.3V_OUT J20-6,J20-45

VCCIOD	out		8,10	VIOTB	FMC_VA DJ 2V5 3.3VOUT	VCCIO13	R26M3. 3VOUT J2B-B1	VCCIOD	J10M3. 3VOUT, M1. 8VOUT R26M3. 3VOUT J2B-B1	VIOTB	FMC_VA DJ 2V5 3.3VOUT	VCCIO13	R22->M3. 3VOUT/J6B- B1	VCCIOD	J27 M1.8VOUT, 2.5V, 3.3V_OUT J17-6,J17-45	VCCIOD	J27 M1.8VOUT, 2.5V, 3.3V_OUT J17-6,J17-45
PWR_2	out	14,16		3V3IN	3.3V	3.3V	3.3V	3.3V	3.3V	3V3IN	3.3V	3.3V	3.3V	3.3V	use ext. 3.3V power supply	3.3V	use ext. 3.3V power supply
VCCIOB	out		2,4	no name / VIOTA	FMC_VA DJ 2V5 3.3VOUT	VCCIO34	J5M3. 3VOUT J1B-B32	VCCIOB	J8M3.3VOUT, M1.8VOUT J2B-B32	VIOTB	FMC_VA DJ 2V5 3.3VOUT	1.8V	1.8V	VCCIOB	J5 M1.8VOUT, 2.5V, 3.3V_OUT	VCCIOB	NC
VCCIOC	out		6	no name / VIOTA	FMC_VA DJ 2V5 3.3VOUT	VCCIO33	R25M3. 3VOUT J2B-B32	VCCIOC	J9M3. 3VOUT, M1. 8VOUT R25M3. 3VOUT J2B-B32	VIOTB	FMC_VA DJ 2V5 3.3VOUT	VCCIO33	R21->M3. 3VOUT	VCCIOC	J6 M1.8VOUT, 2.5V, 3.3V_OUT	VCCIOC	NC
PWR_M1	in		9,11	3.3 VOUT	3.3V	3.3 VOUT	3.3V	M3. 3VOUT	3.3V	3.3 VOUT	3.3V	M3. 3VOUT	3.3V	3.3 V_OUT	3.3V	3.3 V_OUT	3.3V
PWR_M2	in	40		VIOB	1.8V	M1. 8VOUT	1.8V	M1. 8VOUT	1.8V	VIOB	1.8V	M1. 8VOUT	1.8V	M1. 8VOUT	1.8V	M1. 8VOUT	1.8V
PWR_M3	in		20	NC		NC		NC		NC		NC			NC		NC
PWR_VBAT	out	80		VBAT	B1	VBAT	J7	VBAT	J7	NC		VBAT	J9	VBAT	NC	VBAT	NC
PWR_JTAG	in		92	VCCJTAG		VCCJTAG		VCCJTAG		VCCJTAG		VCCJTAG		VCCJTAG		VCCJTAG	NC

Power comparison of all 4x5 carrier boards. ***Power direction based on carrier boards view.** There are 4 variable user supplied I/O voltages (VCCIOA, VCCIOB, VCCIOC and VCCIOD). PWR_1 and PWR_2 are fixed from carrier boards. PWR_M1 and PWR_M2 normally use default value from module. NC=Not Connected

Attention: On some carrier boards the user supplied I/O voltages are connected together (red colored schematic names).

Power Pin Connection on different Carrierboards

Carrier Pinout Overview

J1					J2				
Direction	Name	Pin	Pin	Direction	Direction	Name	Pin	Pin	Direction
out	PWR_1	2	1	IO	out	PWR_1	2	1	IO
out	PWR_1	4	4	IO	out	PWR_1	4	4	IO
out	PWR_1	6	5	IO	out	PWR_1	6	5	IO
to	NOISEL	8	7	IO	to	NOISEL	8	7	IO
out	PWR_2	10	9	IO	out	PWR_2	10	9	IO
out	VCCIOA	12	11	IO	out	VCCIOA	12	11	IO
out	PWR_3	14	13	IO	out	PWR_3	14	13	IO
out	PWR_3	15	15	IO	out	PWR_3	15	15	IO
		18	17	IO			18	17	IO
		20	19	IO			20	19	IO
		22	21	IO			22	21	IO
		24	23	IO			24	23	IO
		26	25	IO			26	25	IO
		28	27	IO			28	27	IO
		30	29	IO			30	29	IO
		32	31	IO			32	31	IO
		34	33	IO			34	33	IO
		36	35	IO			36	35	IO
		38	37	IO			38	37	IO
in	PWR_M1	40	39	IO	in	PWR_M1	40	39	IO
		42	41	IO			42	41	IO
		44	43	IO			44	43	IO
		46	45	IO			46	45	IO
		48	47	IO			48	47	IO
		50	49	IO			50	49	IO
		52	51	IO			52	51	IO
		54	53	IO			54	53	IO
		56	55	IO			56	55	IO
		58	57	IO			58	57	IO
		60	59	IO			60	59	IO
		62	61	IO			62	61	IO
		64	63	IO			64	63	IO
		66	65	IO			66	65	IO
		68	67	IO			68	67	IO
		70	69	IO			70	69	IO
		72	71	IO			72	71	IO
		74	73	IO			74	73	IO
		76	75	IO			76	75	IO
		78	77	IO			78	77	IO
out	PWR_M2	80	79	IO	out	PWR_M2	80	79	IO
		82	81	IO			82	81	IO
		84	83	IO			84	83	IO
in	I2UART_TX	86	85	IO	in	I2UART_TX	86	85	IO
		88	87	IO			88	87	IO
out	ITAGSEL	90	89	IO	out	ITAGSEL	90	89	IO
		92	91	IO			92	91	IO
		94	93	IO			94	93	IO
		96	95	IO			96	95	IO
		98	97	IO			98	97	IO
		100	99	IO			100	99	IO

Legend

Power-VCC

Power-GND

Special

IO / Special

VCCIOA

VCCIOB

VCCIOD

Positions are displayed as
Top View

J1					J2				
Direction	Name	Pin	Pin	Direction	Direction	Name	Pin	Pin	Direction
out	PWR_1	2	1	IO	out	PWR_1	2	1	IO
out	PWR_1	4	4	IO	out	PWR_1	4	4	IO
out	PWR_1	6	5	IO	out	PWR_1	6	5	IO
to	NOISEL	8	7	IO	to	NOISEL	8	7	IO
out	PWR_2	10	9	IO	out	PWR_2	10	9	IO
out	VCCIOA	12	11	IO	out	VCCIOA	12	11	IO
out	PWR_3	14	13	IO	out	PWR_3	14	13	IO
out	PWR_3	15	15	IO	out	PWR_3	15	15	IO
		18	17	IO			18	17	IO
		20	19	IO			20	19	IO
		22	21	IO			22	21	IO
		24	23	IO			24	23	IO
		26	25	IO			26	25	IO
		28	27	IO			28	27	IO
		30	29	IO			30	29	IO
		32	31	IO			32	31	IO
		34	33	IO			34	33	IO
		36	35	IO			36	35	IO
		38	37	IO			38	37	IO
in	PWR_M1	40	39	IO	in	PWR_M1	40	39	IO
		42	41	IO			42	41	IO
		44	43	IO			44	43	IO
		46	45	IO			46	45	IO
		48	47	IO			48	47	IO
		50	49	IO			50	49	IO
		52	51	IO			52	51	IO
		54	53	IO			54	53	IO
		56	55	IO			56	55	IO
		58	57	IO			58	57	IO
		60	59	IO			60	59	IO
		62	61	IO			62	61	IO
		64	63	IO			64	63	IO
		66	65	IO			66	65	IO
		68	67	IO			68	67	IO
		70	69	IO			70	69	IO
		72	71	IO			72	71	IO
		74	73	IO			74	73	IO
		76	75	IO			76	75	IO
		78	77	IO			78	77	IO
out	PWR_M2	80	79	IO	out	PWR_M2	80	79	IO
		82	81	IO			82	81	IO
		84	83	IO			84	83	IO
in	I2UART_TX	86	85	IO	in	I2UART_TX	86	85	IO
		88	87	IO			88	87	IO
out	ITAGSEL	90	89	IO	out	ITAGSEL	90	89	IO
		92	91	IO			92	91	IO
		94	93	IO			94	93	IO
		96	95	IO			96	95	IO
		98	97	IO			98	97	IO
		100	99	IO			100	99	IO

Legend

Power-VCC

Power-GND

Special

IO / Special

VCCIOA

VCCIOB

VCCIOD

Positions are displayed as
Top View

J1					J2				
Direction	Name	Pin	Pin	Direction	Direction	Name	Pin	Pin	Direction
out	PWR_1	2	1	IO	out	PWR_1	2	1	IO
out	PWR_1	4	4	IO	out	PWR_1	4	4	IO
out	PWR_1	6	5	IO	out	PWR_1	6	5	IO
to	NOISEL	8	7	IO	to	NOISEL	8	7	IO
out	PWR_2	10	9	IO	out	PWR_2	10	9	IO
out	VCCIOA	12	11	IO	out	VCCIOA	12	11	IO
out	PWR_3	14	13	IO	out	PWR_3	14	13	IO
out	PWR_3	15	15	IO	out	PWR_3	15	15	IO
		18	17	IO			18	17	IO
		20	19	IO			20	19	IO
		22	21	IO			22	21	IO
		24	23	IO			24	23	IO
		26	25	IO			26	25	IO
		28	27	IO			28	27	IO
		30	29	IO			30	29	IO
		32	31	IO			32	31	IO
		34	33	IO			34	33	IO
		36	35	IO			36	35	IO
		38	37	IO			38	37	IO
in	PWR_M1	40	39	IO	in	PWR_M1	40	39	IO
		42	41	IO			42	41	IO
		44	43	IO			44	43	IO
		46	45	IO			46	45	IO
		48	47	IO			48	47	IO
		50	49	IO			50	49	IO
		52	51	IO			52	51	IO
		54	53	IO			54	53	IO
		56	55	IO			56	55	IO
		58	57	IO			58	57	IO
		60	59	IO			60	59	IO
		62	61	IO			62	61	IO
		64	63	IO			64	63	IO
		66	65	IO			66	65	IO
		68	67	IO			68	67	IO
		70	69	IO			70	69	IO
		72	71	IO			72	71	IO
		74	73	IO			74	73	IO
		76	75	IO			76	75	IO
		78	77	IO			78	77	IO
out	PWR_M2	80	79	IO	out	PWR_M2	80	79	IO
		82	81	IO			82	81	IO
		84	83	IO			84	83	IO
in	I2UART_TX	86	85	IO	in	I2UART_TX	86	85	IO
		88	87	IO			88	87	IO
out	ITAGSEL	90	89	IO	out	ITAGSEL	90	89	IO
		92	91	IO			92	91	IO
		94	93	IO			94	93	IO
		96	95	IO			96	95	IO
		98	97	IO			98	97	IO
		100	99	IO			100	99	IO

Legend

Power-VCC

Power-GND

Special

IO / Special

VCCIOA

VCCIOB

VCCIOD

Positions are displayed as
Top View

J1					J2				
Direction	Name	Pin	Pin	Direction	Direction	Name	Pin	Pin	Direction
out	PWR_1	2	1	IO	out	PWR_1	2	1	IO
out	PWR_1	4	4	IO	out	PWR_1	4	4	IO
out	PWR_1	6	5	IO	out	PWR_1	6	5	IO
to	NOISEL	8	7	IO	to	NOISEL	8	7	IO
out	PWR_2	10	9	IO	out	PWR_2	10	9	IO
out	VCCIOA	12	11	IO	out	VCCIOA	12	11	IO
out	PWR_3	14	13	IO	out	PWR_3	14	13	IO
out	PWR_3	15	15	IO	out	PWR_3	15	15	IO
		18	17	IO			18	17	IO
		20	19	IO			20	19	IO
		22	21	IO			22	21	IO
		24	23	IO			24	23	IO
		26	25	IO			26	25	IO
		28	27	IO			28	27	IO
		30	29	IO			30	29	IO
		32	31	IO			32	31	IO
		34	33	IO			34	33	IO
		36	35	IO			36	35	IO
		38	37	IO			38	37	IO
in	PWR_M1	40	39	IO	in	PWR_M1	40	39	IO
		42	41	IO			42	41	IO
		44	43	IO			44	43	IO
		46	45	IO			46	45	IO
		48	47	IO			48	47	IO
		50	49	IO			50	49	IO
		52	51	IO			52	51	IO
		54	53	IO			54	53	IO
		56	55	IO			56	55	IO
		58	57	IO			58	57	IO
		60	59	IO			60	59	IO
		62	61	IO			62	61	IO
		64	63	IO			64	63	IO
		66	65	IO			66	65	IO
		68	67	IO			68	67	IO
		70	69	IO			70	69	IO
		72	71	IO			72	71	IO
		74	73	IO			74	73	IO
		76	75	IO			76	75	IO

Carrierboard basic power and group pin assignment (Top View), recommended to verify with Schematics

4x5 Module Controller IOs

Name	Module B2B Pin	Carrier B2B Pin	Direction (Module view)	Description	Recommendation
JTAGSEL	JM1-89	JB1-90	in	JTAG Chain multiplexer. Low FPGA, High CPLD. For module with CPLD only.	Connect Pulldown on carrier. DIP switch possible.
SC_EN1	JM1-28	JB1-27	in	Module power. Set high to enable module power. Note: Power management depends on module. Sometimes this is a only used as Power ON Reset like SC_nRST	Connect Pullup on carrier. DIP switch possible
SC_NO SEQ	JM1-7	JB1-8	in / inout	Module Power management. Set high to disable CPLD power management. Note: Power management depends on module and not all modules support extended power management with CPLD.	Connect Pullup or force to GND over zero ohm resistor on carrier. DIP switch possible.
SC_PG OOD	JM1-30	JB1-29	out / inout	Power Good signal. Is Low, if SC_EN1 is set to zero or if power is not ready, otherwise high impedance output. Note: Power management depends on module. On newer Firmware SC_PGOOD will be used as Additionally Boot Mode Pin.	Connect Pullup on carrier. Do not use this signal to enable FPGA Bank voltages. It's only for monitoring. To Enable FPGA Banks, use 3.3V(PWR_M1) or 1.8V(PWR_M2) module output.

SC_BO OTMODE	JM1-32	JB1-31	in	Boot Mode selection Pin for Zynq module only. Default low for primary SD boot and high for primary QSPI boot. Note: Depends also on module CPLD firmware	Connect Pullup on carrier. DIP switch possible.
SC_nRST	JM2-18	JB2-17	in	Low active module reset. Pin force Power one reset on FPGA /SoC. Note: Depending from module CPLD or voltage supervisor is used.	Connect Pullup on carrier. DIP switch possible.

- Controller IOs are 3.3V IOs

 It's planned to use SC_PGOOD also as additional Boot Mode Pin (Pin is bidirectional, pull up or force to zero), to additionally set JTAG only boot mode (to avoid programming problems with some vivado versions, see: [AR#00002 - QSPI Programming issues](#)). Current state of CPLD Redesigns: [AVN-20220506 4 x 5 modules controller IOs redefinition and CPLD updates](#)

4x5 Module Controller IOs

Remove 4x5 module

[4 x 5 SoMs Handling and Usage Precautions](#)

Compatibility Guide

Ethernet LED'S

TE07xx 4x5 modules do not have dedicated pins for the Ethernet PHY LED's, also there are no fix pins on the baseboards for the PHY LED's or any other LED's.

If Ethernet JACKs on Baseboard have LED's then those should be connected to some free PL I/O pins, and then routed in the FPGA logic from the PHY to the I/O Pin in the B2B Connector.

Recommended connections would be to use JM2.89 and JM2.100 for the PHY LED's, those positions support baseboard ETH LED's for TE0701 and TE0703 and TE0706.

JM2 pins 1, 3 (TE0720 Bank 34 Voltage)

- To be compatible with TE0720 JM2 pins 1,3 must be connected to some valid VCCIO voltage.
- When JM2 pins 1, 3 are not powered TE0720 would not boot, and may not be recognized in JTAG chain as well.
- When those pins are not used on the module (TE0710) then to be compatible with TE0720:
- Solution A: connect to 3.3V out from the module, option compatible to all modules except those with HP banks
- Solution B: connect to 1.8V out from the module, option compatible with all modules.

Carrier Board Checklist

Schematic Checklist

--	--	--

1	Are B2B pin numbers on the connectors mirrored compared to the module pin numbers?	As B2B connectors are "unisex" type they do mirror pin numbers when connecting. That is pin1 connects to pin2, and pin2 to pin1, etc.
2	Are B2B connectors named JB1, JB2, JB3?	This is not a hard requirement, but it helps to use the same identifiers.
3	Are all GND pins connected to a common ground net?	
4	Are all VIN pins connected together?	
5	Is JB2 pin 92 pin used as VREF for the JTAG interface?	for future compatibility only, currently all modules have 3.3V JTAG
6	For 7 Series Zynq module only: Are external circuits/buffers connecting to MIO bank 1 pins powered from JB1 pin 40?	JB1 pins 18, 20, 22, 24, 26, 28 use voltage at pin 40 as VCCIO. Currently it is 1.8V for 4x5 Zynq Modules. Note: Different Power supply on TE0820(3.3V MIO Bank) and normal FPGA modules(check schematics)

PCB Checklist

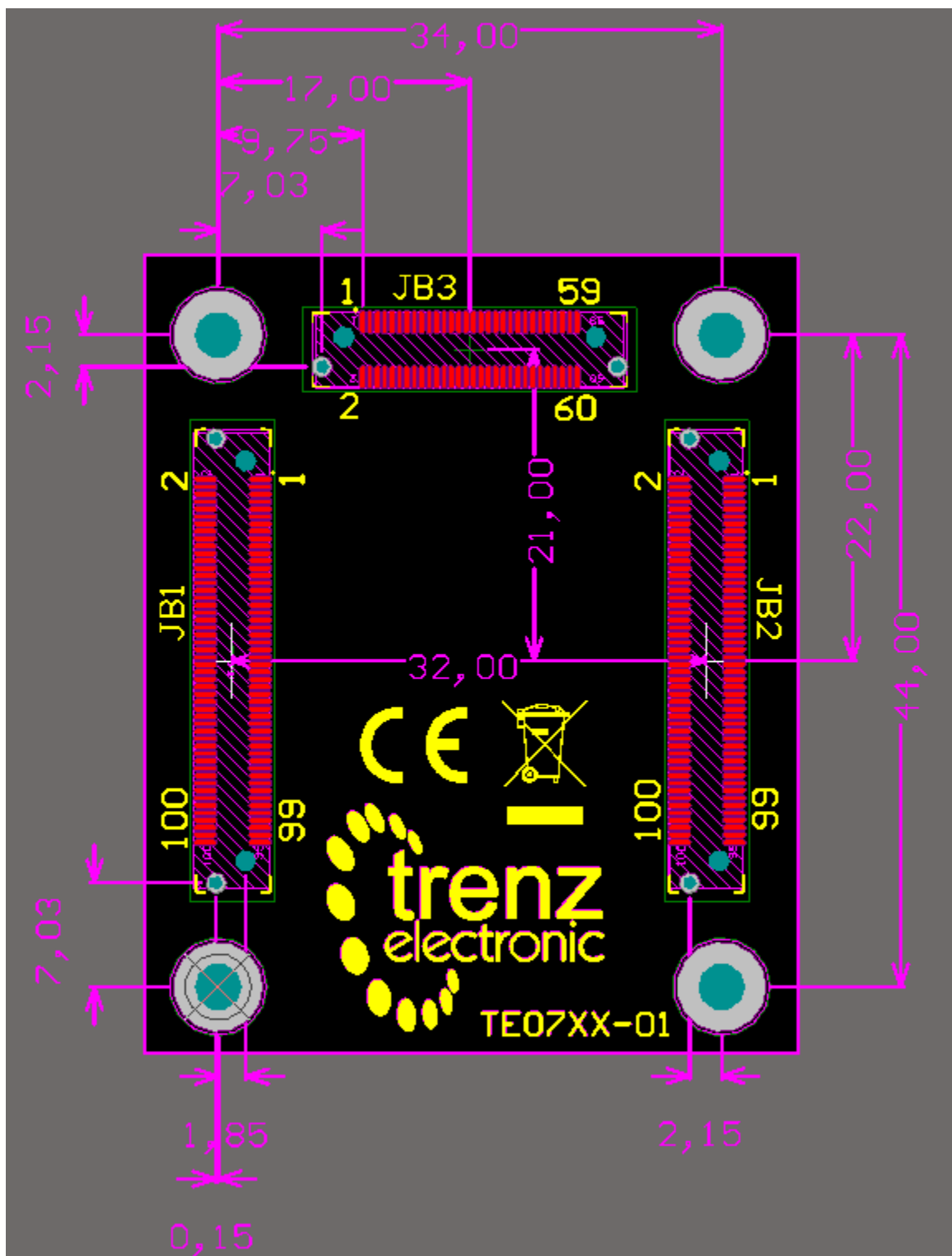
1	Are mounting holes placed properly?	Four Mounting holes should always be used. They are required for mounting screws and for module extraction. The mounting holes will also help in dissipating some heat from the module to the carrier board PCB. Four holes with a 3.2mm diameter should be placed exactly at the corners of a 34mm by 44mm rectangle.
2	Are B2B headers properly placed?	B2B headers must be placed and aligned very precisely or the module will not align correctly (in the worst case module insertion could destroy the connectors or the PCB). The B2B headers should be locked on the PCB, and it is recommended that the position and placement be checked against placement dimensions before submitting the PCB files.
3	Are B2B headers rotated properly?	As B2B header pin numbers differ from module to the carrier (swap of odd and even numbers), it is recommended that the rotation is checked in the PCB design.
4	Height clearance below module	Components can be placed below the module but height clearance rules must be obeyed.
5	Power dissipation of components below module	It is not recommended to place any components with high power dissipation below the module, as there will be almost no airflow below the module.

Visual Check of Module placement

It is highly recommended to use the Base board Template designs as a starting point for new PCB designs. If that is not possible, then adding linear dimensions in the design helps to check that all connectors and mounting holes are properly placed.



This placement is same for all 4x5 Modules!



Top view of the Carrier Board.

Connector numbers as on base! (pin JB1.1 on base would mate to pin JM1.2 on module).